MOSFET – N-Channel, SUPERFET® II

800 V, 6 A, 1.3 Ω

FCPF1300N80Z

V_{DSS}	$R_{DS(on)}$ MAX	I_D MAX
800 V	1.3 Ω @ 10 V	6 A

Description

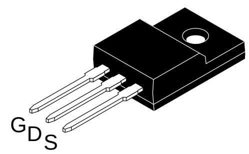
SUPERFET II MOSFET is **onsemi**'s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. In addition, internal gate−source ESD diode allows to withstand over 2 kV HBM surge stress. Consequently, SUPERFET II MOSFET is very suitable for the switching power applications such as Audio, Laptop adapter, Lighting, ATX power and industrial power applications.

Features

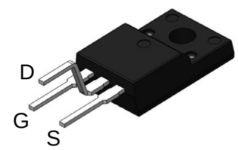
- $R_{DS(on)}$ = 1.05 Ω (Typ.)
- Ultra Low Gate Charge (Typ. Q_g = 16.2 nC)
- Low E_{oss} (Typ. 1.57 μJ @ 400 V)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)}$ = 48.7 pF)
- 100% Avalanche Tested
- RoHS Compliant
- ESD Improved Capability

Applications

- AC−DC Power Supply
- LED Lighting

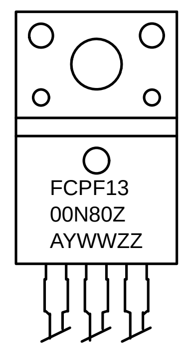


TO−220 Fullpack,
3−Lead / TO−220F−3SG
CASE 221AT



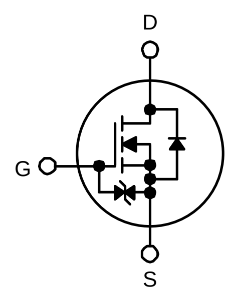
TO−220−3LD LF
CASE 340BJ

MARKING DIAGRAM



FCPF1300N80Z = Specific Device Code
A = Assembly Location
YWW = Date Code (Year & Week)
ZZ = Assembly Lot

N−CHANNEL MOSFET



ORDERING INFORMATION

Part Number	Package	Shipping
FCPF1300N80Z	TO−220	1000 Units / Tube
FCPF1300N80ZYD	TO−220F Y−formed	800 Units / Tube

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, unless otherwise noted)

Symbol	Parameter		FCPF1300N80Z FCPF1300N80ZYD	Unit
V_{DSS}	Drain to Source Voltage		800	V
V_{GSS}	Gate to Source Voltage	− DC	±20	V
		− AC (f > 1 Hz)	±30	
I_D	Drain Current	− Continuous (T_C = 25°C)	6.0*	A
		− Continuous (T_C = 100°C)	3.8*	
I_{DM}	Drain Current	− Pulsed (Note 1)	12*	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		48	mJ
I_{AR}	Avalanche Current (Note 1)		0.8	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		0.26	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
P_D	Power Dissipation	(T_C = 25°C)	24	W
		− Derate Above 25°C	0.19	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering, 1/8” from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature, with heatsink.
1. Repetitive rating: pulse width limited by maximum junction temperature.
2. I_{AS} = 0.8 A, R_G = 25 Ω, starting T_J = 25°C.
3. $I_{SD} \leq 6$ A, di/dt ≤ 200 A/μs, $V_{DD} \leq BV_{DSS}$, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FCPF1300N80Z FCPF1300N80ZYD	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	5.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	800	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	–	0.85	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 800 V, V_{GS} = 0 V	–	–	25	μA
		V_{DS} = 640 V, V_{GS} = 0 V, T_C = 125°C	–	–	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 0.4 mA	2.5	–	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 2 A	–	1.05	1.3	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20 V, I_D = 2 A	–	4.5	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	–	661	880	pF
C_{oss}	Output Capacitance		–	22.3	30	pF
C_{rss}	Reverse Transfer Capacitance		–	0.74	–	pF
C_{oss}	Output Capacitance	V_{DS} = 480 V, V_{GS} = 0 V, f = 1 MHz	–	11.4	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 480 V, V_{GS} = 0 V	–	48.7	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 640 V, I_D = 4 A, V_{GS} = 10 V (Note 4)	–	16.2	21	nC
Q_{gs}	Gate to Source Gate Charge		–	3.5	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	6.8	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	4	–	Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 400 V, I_D = 4 A, V_{GS} = 10 V, R_g = 4.7 Ω (Note 4)	–	14	38	ns
t_r	Turn−On Rise Time		–	8.3	27	ns
$t_{d(off)}$	Turn−Off Delay Time		–	33	76	ns
t_f	Turn−Off Fall Time		–	6	22	ns
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	6	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	12	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 4 A	–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 4 A, dI_F/dt = 100 A/μs	–	275	–	ns
Q_{rr}	Reverse Recovery Charge		–	2.9	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

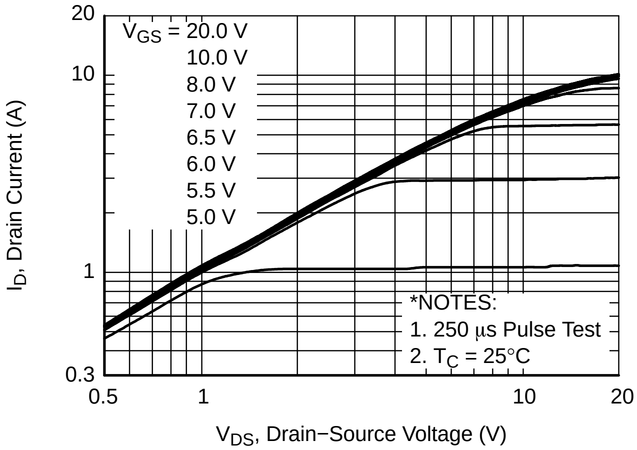


Figure 1. On−Region Characteristics

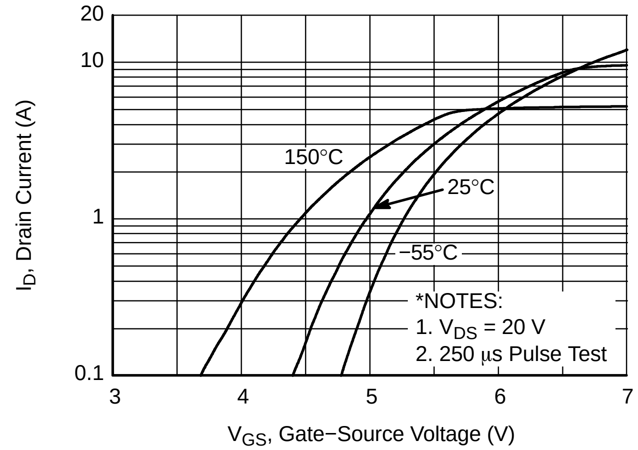


Figure 2. Transfer Characteristics

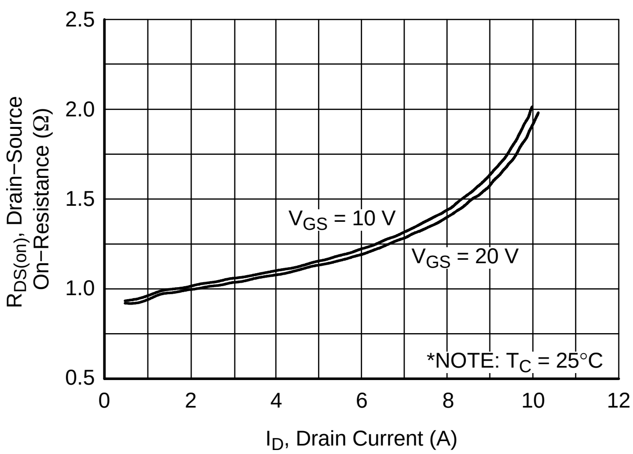


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

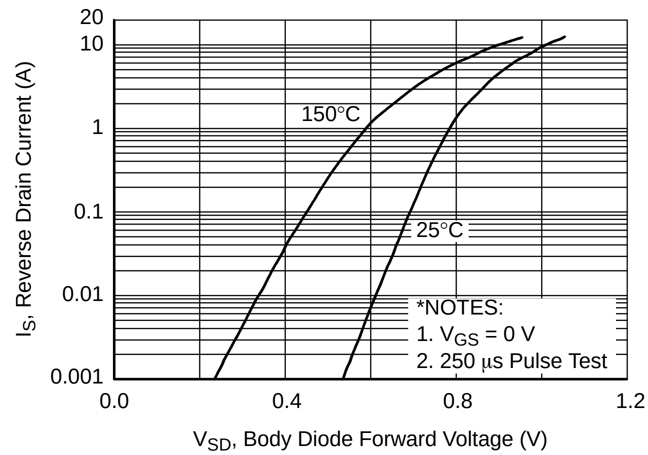


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

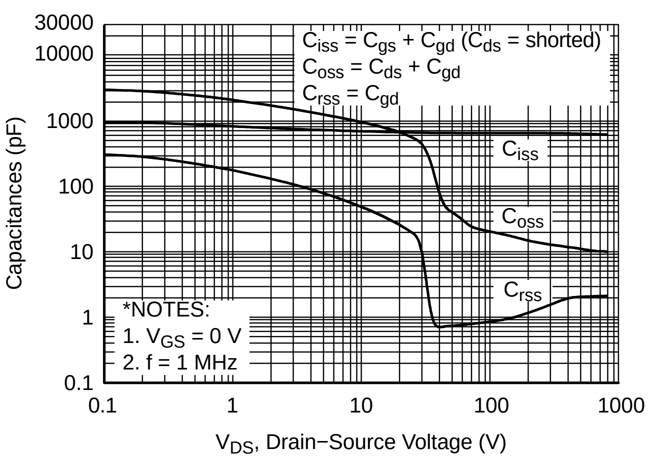


Figure 5. Capacitance Characteristics

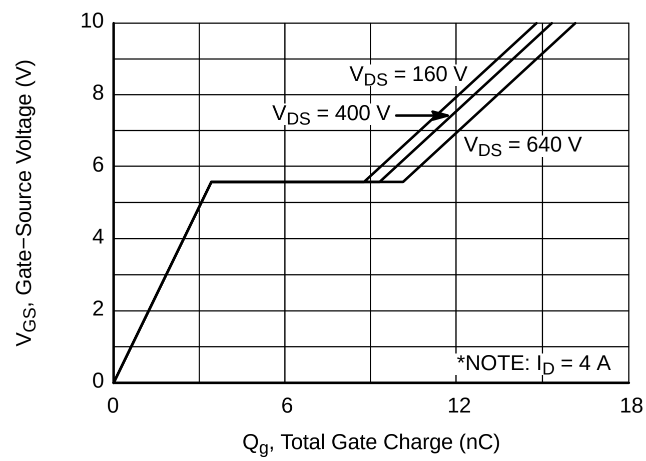


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

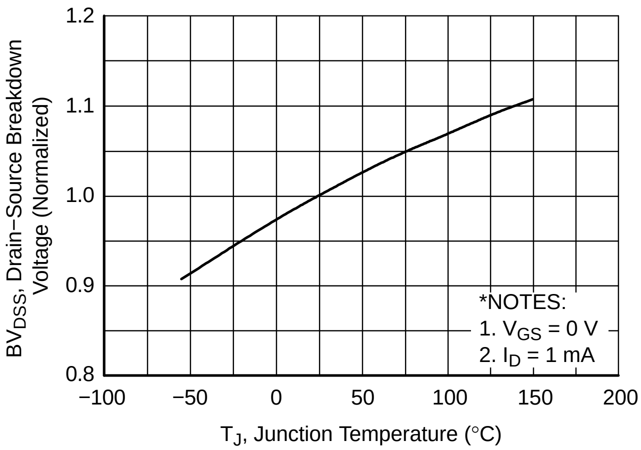


Figure 7. Breakdown Voltage Variation vs. Temperature

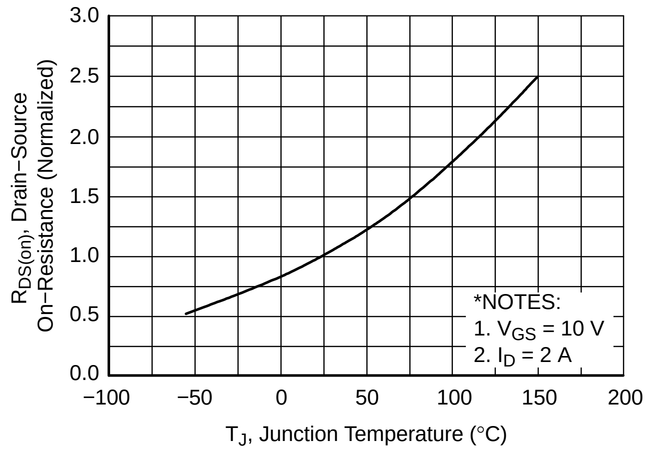


Figure 8. On−Resistance Variation vs. Temperature

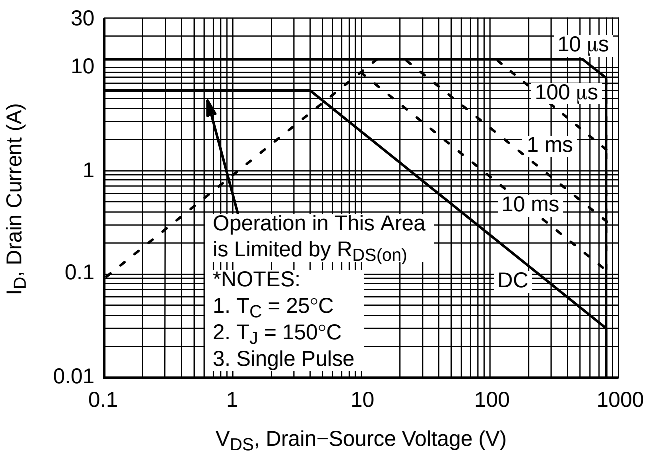


Figure 9. Maximum Safe Operating Area

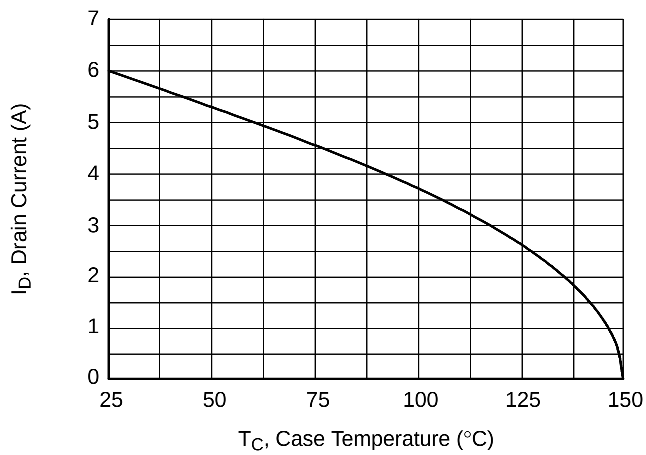


Figure 10. Maximum Drain Current vs. Case Temperature

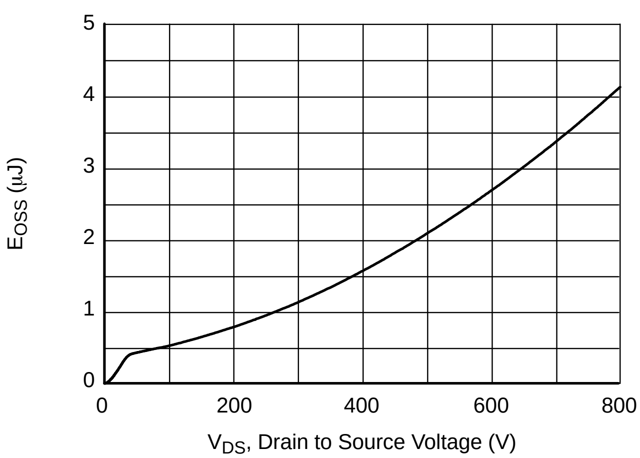


Figure 11. E_{OSS} vs. Drain to Source Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

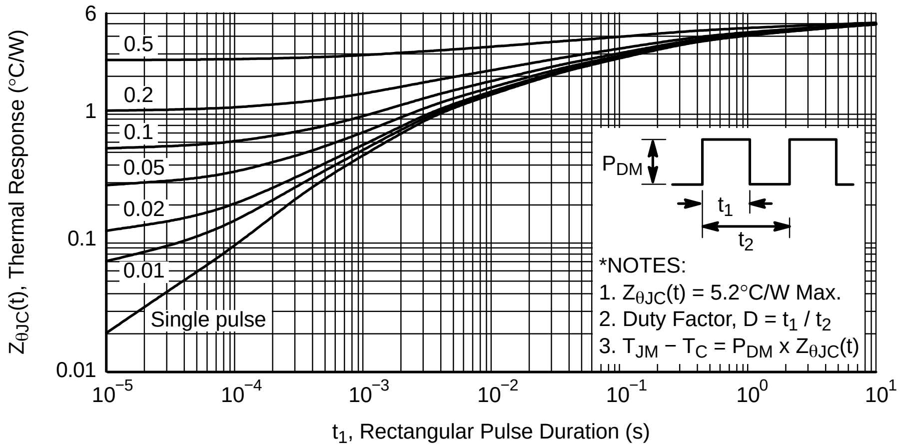


Figure 12. Transient Thermal Response Curve

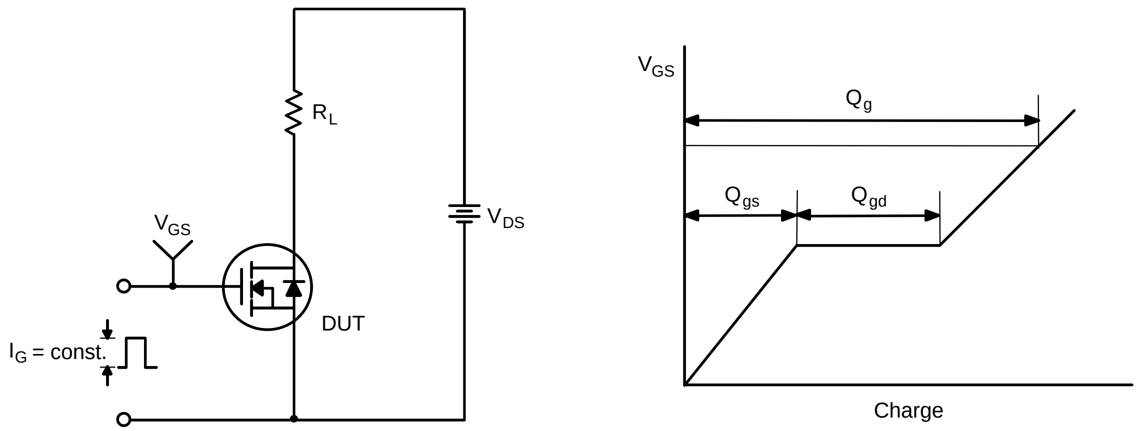


Figure 13. Gate Charge Test Circuit & Waveform

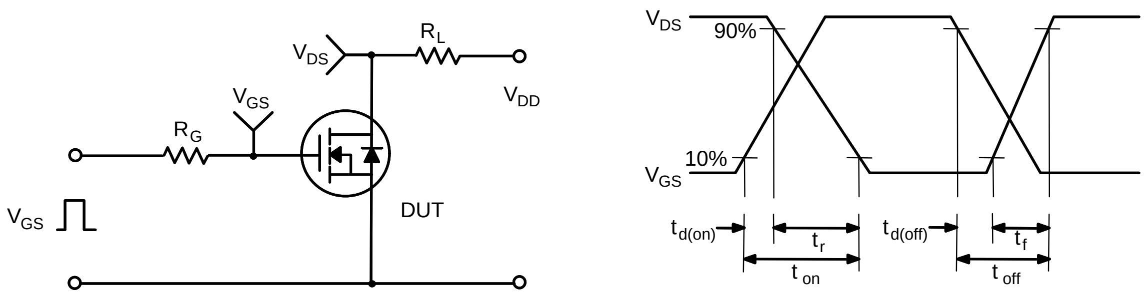


Figure 14. Resistive Switching Test Circuit & Waveforms

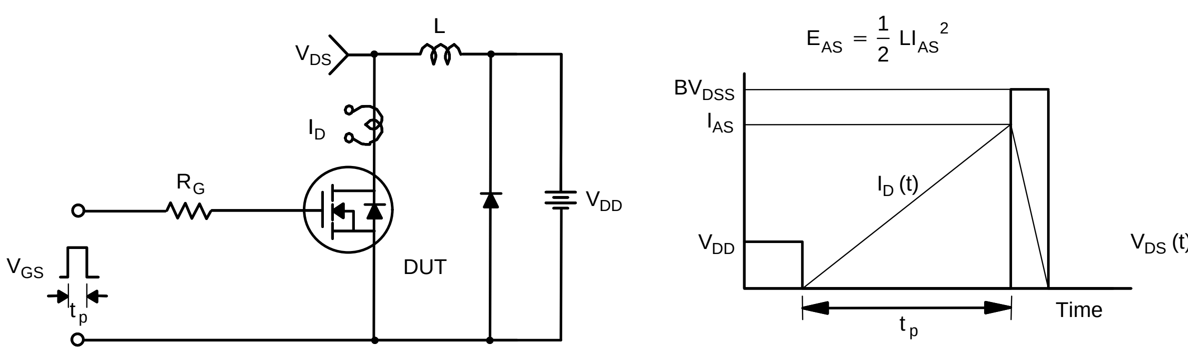


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

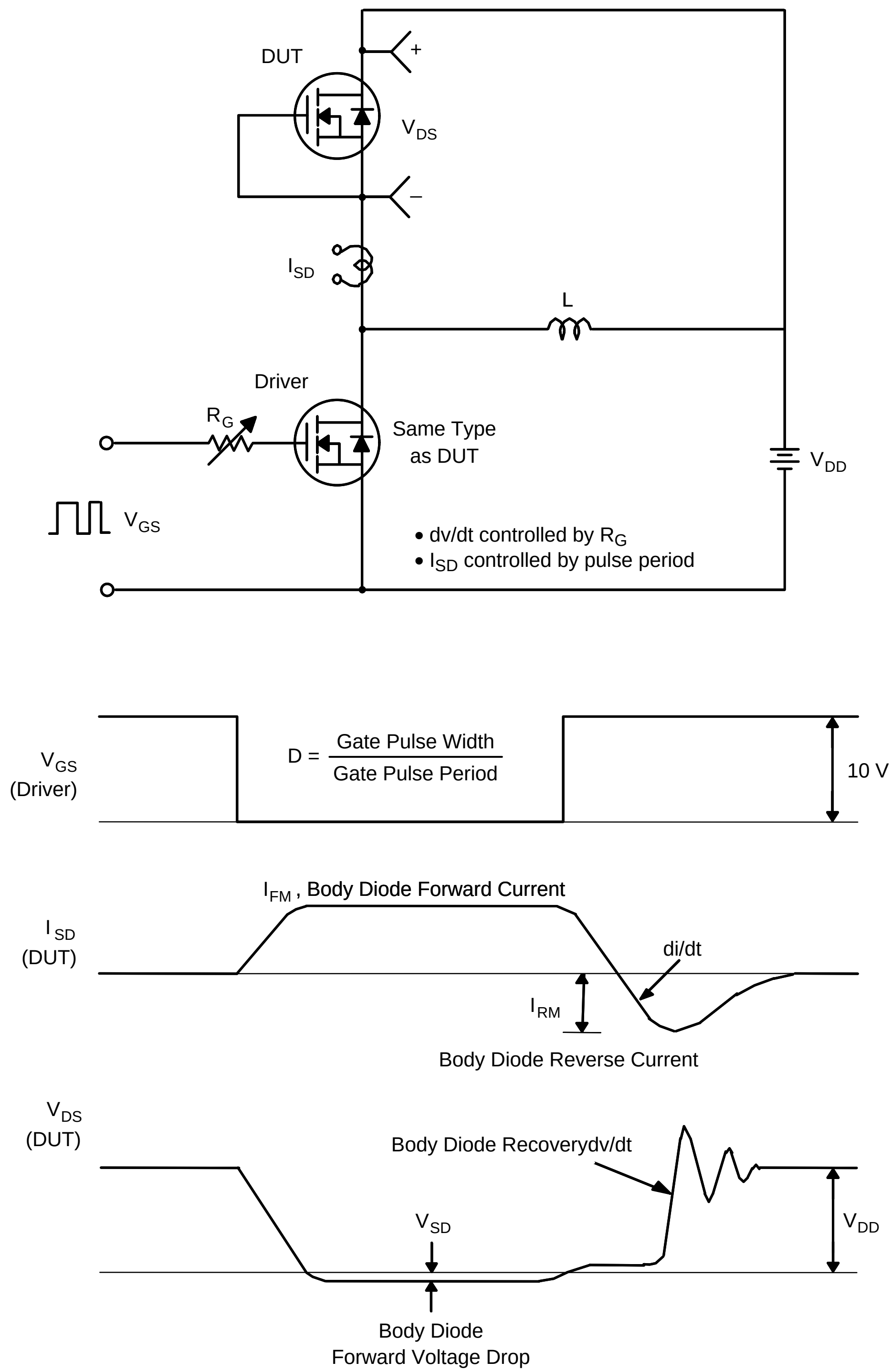
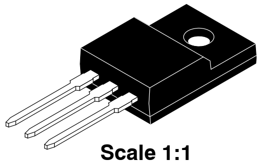


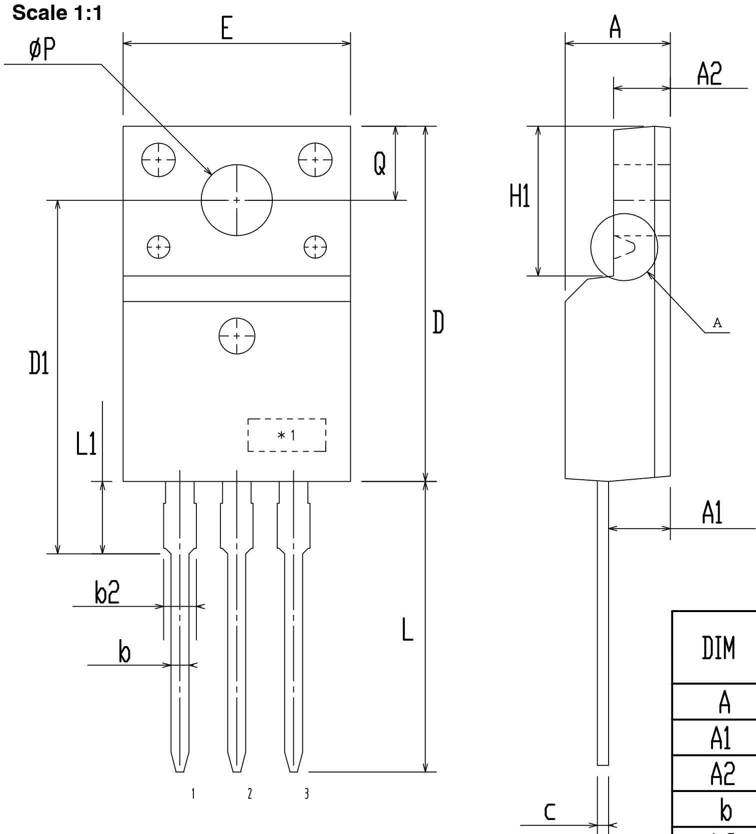
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

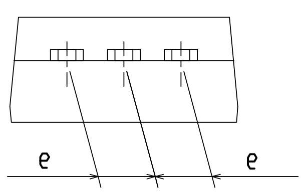


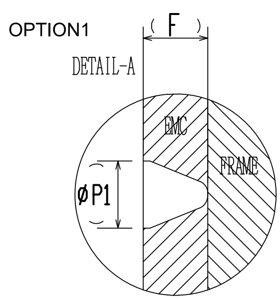
Scale 1:1

TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT
ISSUE B

DATE 19 JAN 2021







DIM	MILLIMITERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
ø P	2.98	3.18	3.38
ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:
A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.
C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

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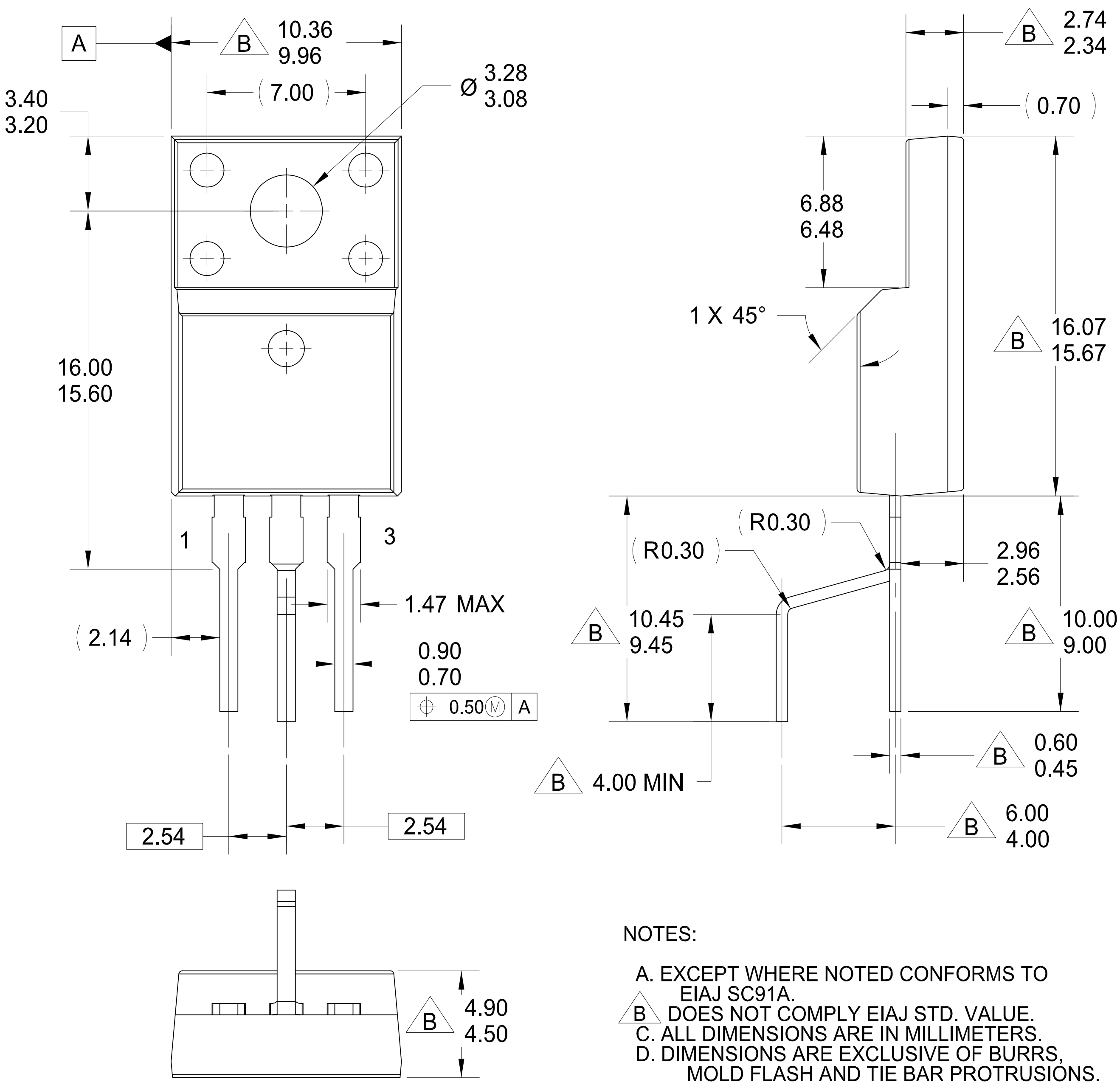
DESCRIPTION:	TO−220 FULLPACK, 3−LEAD / TO−220F−3SG	PAGE 1 OF 1

TO−220−3LD LF
CASE 340BJ
ISSUE O

DATE 31 AUG 2016



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B. DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.

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