MOSFET – N-Channel

600 V, 47 A, 79 mΩ

FCH47N60-F085

Description

SUPERFET[®] is ON Semiconductor's proprietary new generation of high voltage MOSFETs utilizing an advanced charge balance mechanism for outstanding low on–resistance and lower gate charge performance.

This advanced technology has been tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate and higher avalanche energy.

Consequently, SUPERFET is suitable for various automotive DC/DC power conversion.

Features

- Typical $r_{DS(on)} = 64 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 47 \text{ A}$
- Typical $Q_{g(tot)} = 187 \text{ nC}$ at $V_{GS} = 10 \text{ V}$, $I_D = 47 \text{ A}$
- UIS Capability
- Qualified to AEC Q101 and PPAP Capable
- This Device is Pb-Free and is RoHS Compliant

Applications

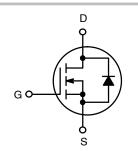
- Automotive On Board Charger
- Automotive DC/DC Converter for HEV



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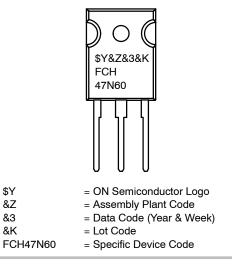
V _{DSS}	R _{DS(ON)} MAX	I _D MAX
600 V	79 m Ω	47 A



N-Channel MOSFET



MARKING DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

MAXIMUM RATINGS (T_C = 25°C, unless otherwise specified)

Symbol	Parameter	Ratings	Unit	
V _{DSS}	Drain to Source Voltage		600	V
V _{GS}	Gate to Source Voltage		±30	V
Ι _D	Drain Current – Continuous (V _{GS} = 10) (Note 1)	$T_{C} = 25^{\circ}C$	47	А
	Pulsed Drain Current	T _C = 25°C	See Fig. 4	
E _{AS}	Single Pulsed Avalanche Rating (Note 2)		810	mJ
PD	Power Dissipation		417	W
	Derate above 25°C		3.3	W/°C
T _J , T _{STG}	Operating and Storage Temperature		–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Current is limited by bondwire configuration.

2. Starting $T_J = 25^{\circ}$ C, L = 5 mH, $I_{AS} = 18$ A, $V_{DD} = 100$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche. 3. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Unit
$R_{ ext{ heta}JC}$	Thermal Resistance Junction to Case	0.3	°C/W
$R_{ hetaJA}$	Maximum Thermal Resistance Junction to Ambient (Note 3)	50	

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Reel Size	Tape Width	Quantity
FCH47N60-F085	FCH47N60	TO-247-3LD	-	-	30 Units

ELECTRICAL CHARACTERISTICS (T. = 25°C unless otherwise noted)

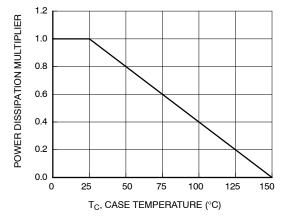
Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARAC	CTERISTICS	·				
B _{VDSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I _D = 250 μ A	600	-	_	V
I _{DSS}	Drain to Source Leakage Current	V_{DS} = 600 V, V_{GS} = 0 V, T_{J} = 25 $^{\circ}\text{C}$	-	-	1	μA
		V_{DS} = 600 V, V_{GS} = 0 V, T_{J} = 150°C (Note 4)	-	-	1	mA
I _{GSS}	Gate to Source Leakage Current	V _{GS} = ±30 V	_	-	±100	nA
ON CHARACT	TERISTICS					
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS}=V_{DS},\ I_{D}=250\ \mu A$	3	4	5	V
r _{DS(on)}	Drain to Source On Resistance	V_{GS} = 10 V, I _D = 47 A, T _J = 25°C	-	64	79	mΩ
		V_{GS} = 10 V, I _D = 47 A, T _J = 150°C (Note 4)	-	180	223	mΩ
OYNAMIC CH	ARACTERISTICS	·				
C _{iss}	Input Capacitance	$V_{\rm DS}$ = 25 V, $V_{\rm GS}$ = 0 V, f = 1 MHz	-	5900	8000	pF
C _{oss}	Output Capacitance		-	3200	4200	pF
C _{rss}	Reverse Transfer Capacitance		-	177	-	pF
Rg	Gate Resistance	f = 1 MHz	-	1	-	Ω
Q _{g(TOT)}	Total Gate Charge at 10 V	V_{GS} = 0 to 10 V, V_{DD} = 300 V, I_{D} = 47 A	-	187	250	nC
Q _{g(th)}	Threshold Gate Charge	V_{GS} = 0 to 2 V, V_{DD} = 300 V, I_{D} = 47 A	-	12	18	nC
Q _{gs}	Gate to Source Gate Charge	V _{DD} = 300 V, I _D = 47 A	-	40	-	nC
Q _{gd}	Gate to Drain "Miller" Charge		I	81	-	nC
SWITCHING C	CHARACTERISTICS					
t _{on}	Turn-On Time	$V_{DD} = 380 \text{ V}, \text{ I}_{D} = 47 \text{ A},$	-	-	410	ns
t _{d(on)}	Turn-On Delay Time	V _{GS} = 10 V, R _G = 25 Ω -	-	110	-	ns
t _r	Rise Time		-	160	-	ns
t _{d(off)}	Turn-Off Delay Time		-	540	-	ns
t _f	Fall Time		-	125	-	ns
t _{off}	Turn-Off Time		-	-	1000	ns

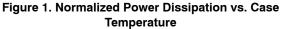
DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Source to Drain Diode Voltage	I_{SD} = 47 A, V_{GS} = 0 V	-	-	1.4	V
		I_{SD} = 23.5 A, V_{GS} = 0 V	-	-	1.25	V
T _{rr}	Reverse Recovery Time	$I_{F} = 47 \text{ A}, \text{ dI}_{SD}/\text{dt} = 100 \text{ A}/\mu\text{s},$	-	683	800	ns
Q _{rr}	Reverse Recovery Charge	V _{DD} = 480 V	-	21	28	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions. 4. The maximum value is specified by design at $T_J = 150^{\circ}$ C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS





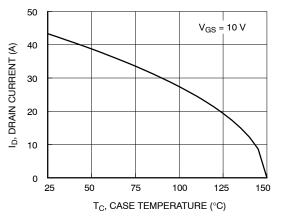


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

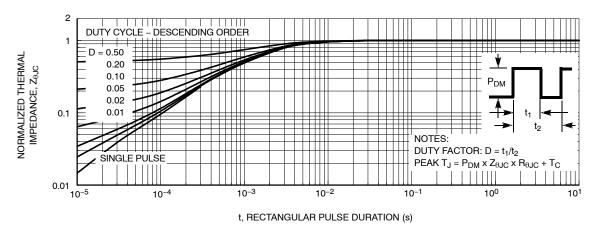


Figure 3. Normalized Maximum Transient Thermal Impedance

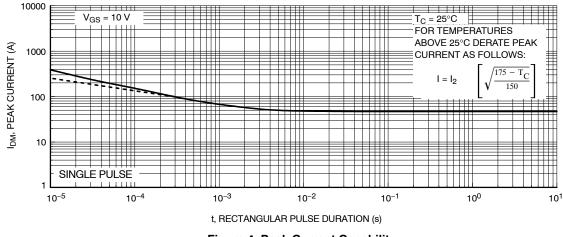


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (continued)

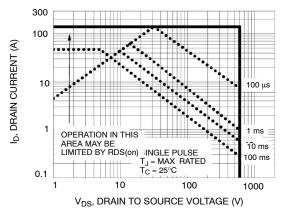


Figure 5. Forward Bias Safe Operating Area

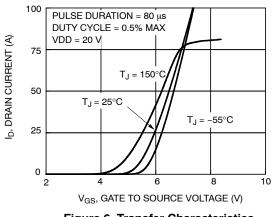


Figure 6. Transfer Characteristics

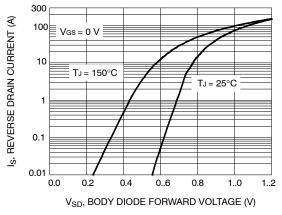
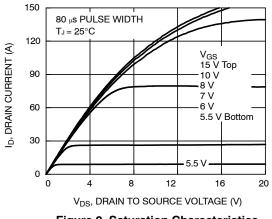


Figure 7. Forward Diode Characteristics





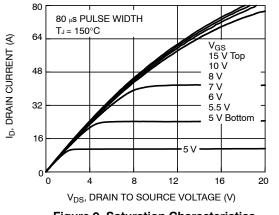
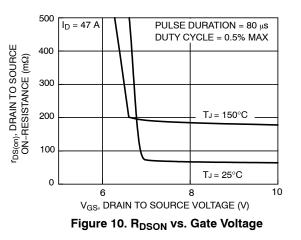
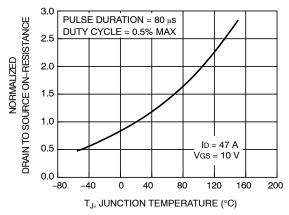


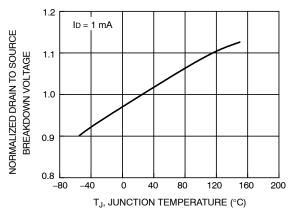
Figure 9. Saturation Characteristics

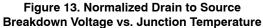


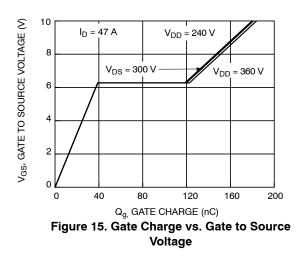
TYPICAL CHARACTERISTICS (continued)











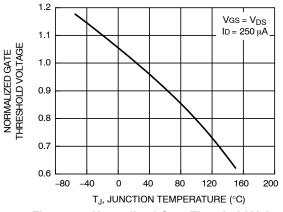


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

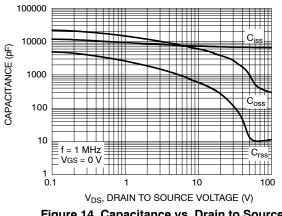


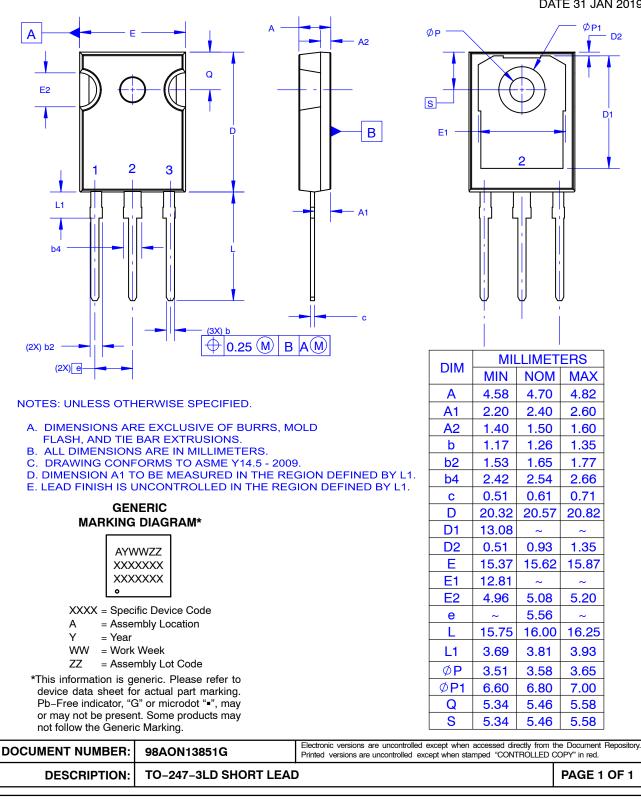
Figure 14. Capacitance vs. Drain to Source Voltage

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TO-247-3LD SHORT LEAD CASE 340CK **ISSUE A**

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