

# MOSFET – N-Channel, SUPERFET II, FRFET

650 V, 35 A, 110 mΩ

## FCH110N65F

### Description

SUPERFET<sup>®</sup> II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SUPERFET II MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications. SUPERFET II FRFET<sup>®</sup> MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

### Features

- 700 V @ T<sub>J</sub> = 150°C
- Typ. R<sub>DS(on)</sub> = 96 mΩ (Typ.)
- Ultra Low Gate Charge (Typ. Q<sub>g</sub> = 98 nC)
- Low Effective Output Capacitance (Typ. C<sub>oss(eff.)</sub> = 464 pF)
- 100% Avalanche Tested
- This Device is Pb-Free and is RoHS Compliant

### Applications

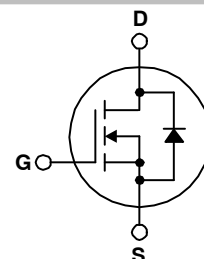
- LCD / LED / PDP TV
- Solar Inverter
- Telecom, Server Power Supplies
- AC-DC Power Supply



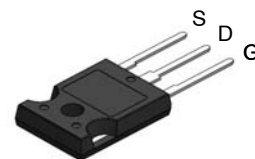
ON Semiconductor<sup>®</sup>

[www.onsemi.com](http://www.onsemi.com)

V <sub>DS</sub>	R <sub>DS(ON)</sub> MAX	I <sub>D</sub> MAX
650 V	110 mΩ @ 10 V	35 A

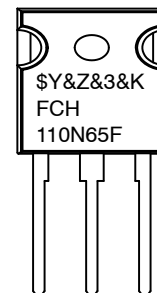


N-CHANNEL MOSFET



TO-247-3LD  
CASE 340CH

### MARKING DIAGRAM



\$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FCH110N65F	= Specific Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FCH110N65F

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	FCH110N65F-F155	Unit
V <sub>DSS</sub>	Drain to Source Voltage	650	V
V <sub>GSS</sub>	Gate to Source Voltage	-DC	±20
		-AC (f > 1 Hz)	±30
I <sub>D</sub>	Drain Current	-Continuous (T <sub>C</sub> = 25°C)	35
		-Continuous (T <sub>C</sub> = 100°C)	24
I <sub>DM</sub>	Drain Current	-Pulsed (Note 1)	105
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	809	mJ
I <sub>AR</sub>	Avalanche Current (Note 1)	8	A
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	3.57	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C)	357
		-Derate Above 25°C	2.86
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to + 150	°C
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8 from Case for 5 Seconds	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. I<sub>AS</sub> = 8 A, R<sub>G</sub> = 25 Ω, Starting T<sub>J</sub> = 25°C
3. I<sub>SD</sub> ≤ 17.5 A, di/dt ≤ 200 A/μs, V<sub>DD</sub> ≤ 380 V, Starting T<sub>J</sub> = 25 °C.

## THERMAL CHARACTERISTICS

Symbol	Parameter	FCH110N65F-F155	Unit
R <sub>θJC</sub>	Thermal Resistance, Junction to Case, Max.	0.35	°C/W
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient, Max.	40	

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH110N65F-F155	FCH110N65F	TO-247-3LD	Tube	N/A	N/A	30 Units

# FCH110N65F

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 25°C	650	-	-	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 150°C	700	-	-	
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C	-	0.72	-	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 650 V, V <sub>GS</sub> = 0 V	-	-	10	μA
		V <sub>DS</sub> = 520 V, T <sub>C</sub> = 125°C	-	110	-	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	-	-	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 3.5 mA	3	-	5	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 17.5 A	-	96	110	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 17.5 A	-	30	-	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	3680	4895	pF
C <sub>oss</sub>	Output Capacitance		-	110	145	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		-	0.65	-	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 380 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	65	-	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 400 V, V <sub>GS</sub> = 0 V	-	464	-	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10 V	V <sub>DD</sub> = 380 V, I <sub>D</sub> = 17.5 A, V <sub>GS</sub> = 10 V (Note 4)	-	98	145	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		-	20	-	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		-	43	-	nC
ESR	Equivalent Series Resistance	f = 1 MHz	-	0.7	-	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 380 V, I <sub>D</sub> = 17.5 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 4.7 Ω (Note 4)	-	31	72	ns
t <sub>r</sub>	Turn-On Rise Time		-	21	52	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		-	89	188	ns
t <sub>f</sub>	Turn-Off Fall Time		-	5.7	21	ns

### DRAIN-SOURCE DIODE CHARACTERISTICS

I <sub>S</sub>	Maximum Continuous Drain to Source Diode Forward Current		-	-	35	A
I <sub>SM</sub>	Maximum Pulsed Drain to Source Diode Forward Current		-	-	105	A
V <sub>SD</sub>	Drain to Source Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 17.5 A	-	-	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 17.5 A, dI <sub>F</sub> /dt = 100 A/μs	-	133	-	ns
Q <sub>rr</sub>	Reverse Recovery Charge		-	0.67	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

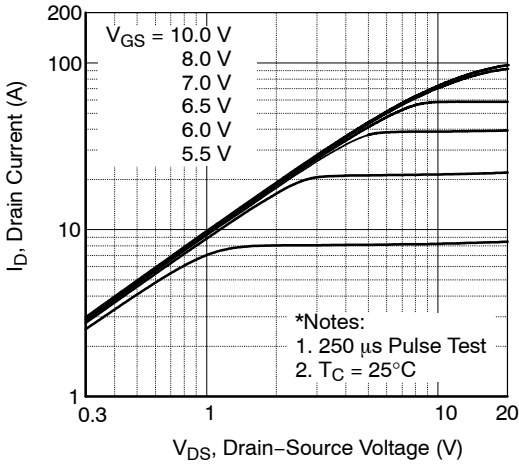


Figure 1. On-Region Characteristics

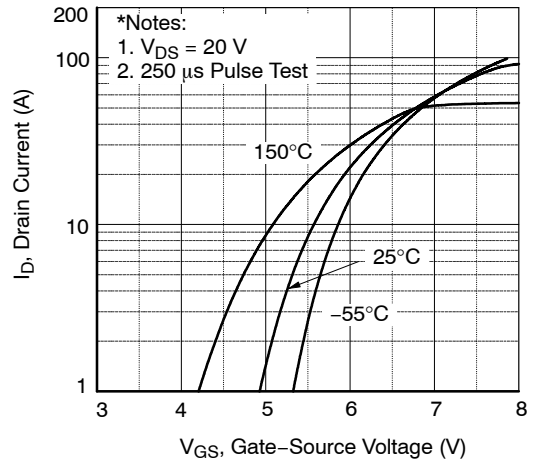


Figure 2. Transfer Characteristics

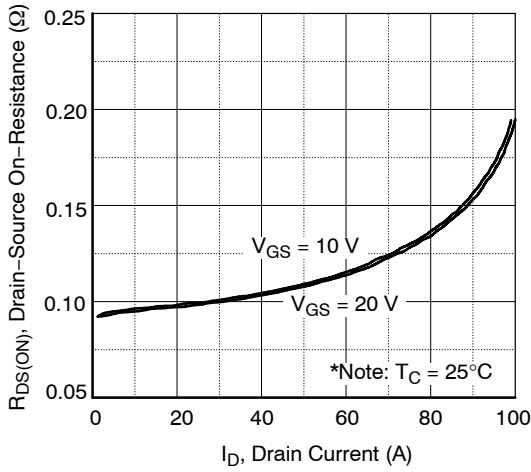


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

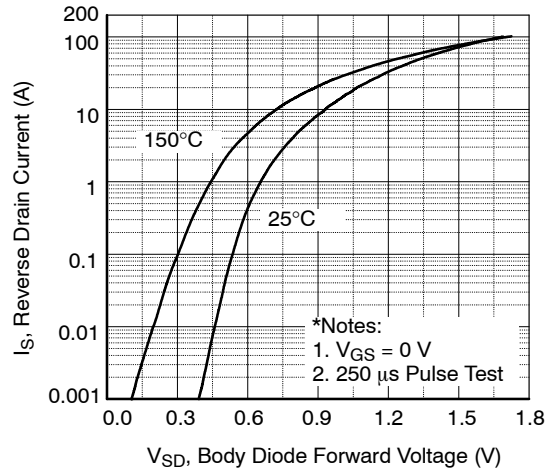


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

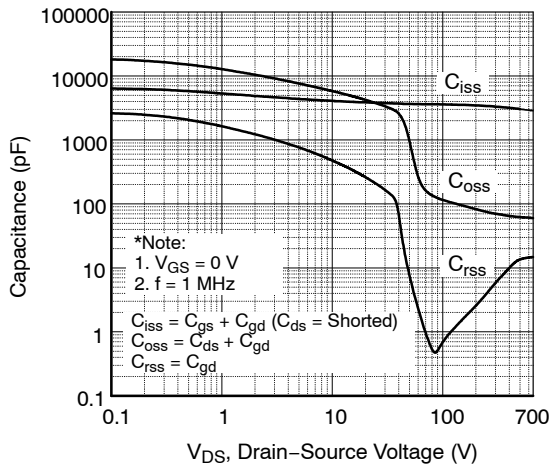


Figure 5. Capacitance Characteristics

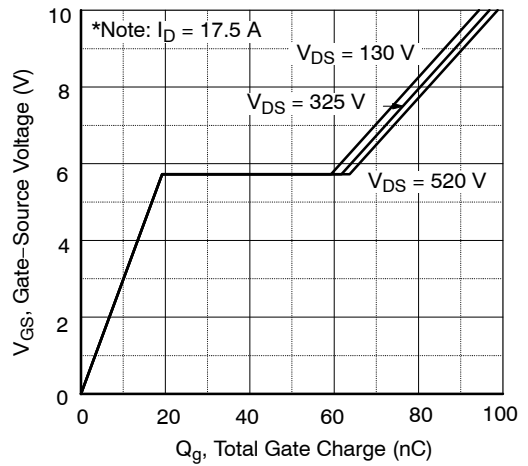
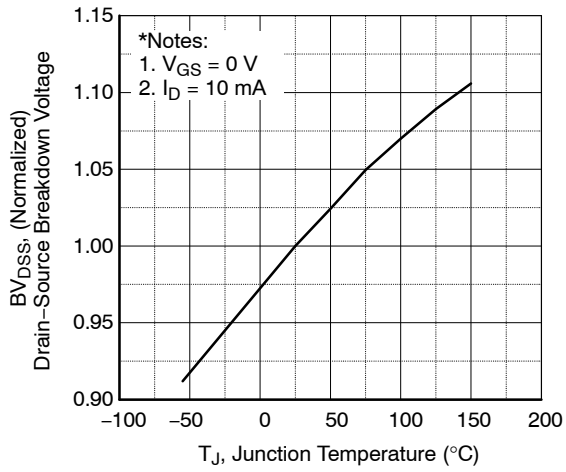


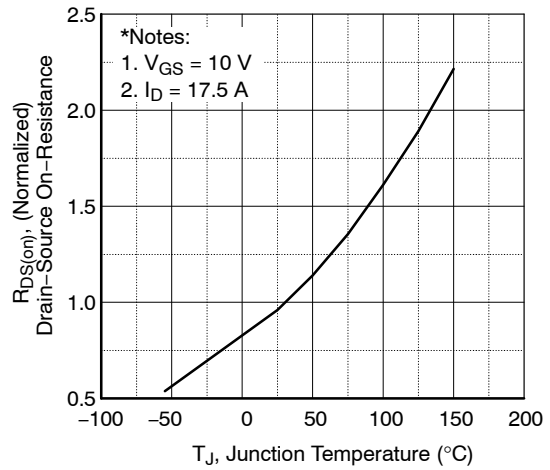
Figure 6. Gate Charge Characteristics

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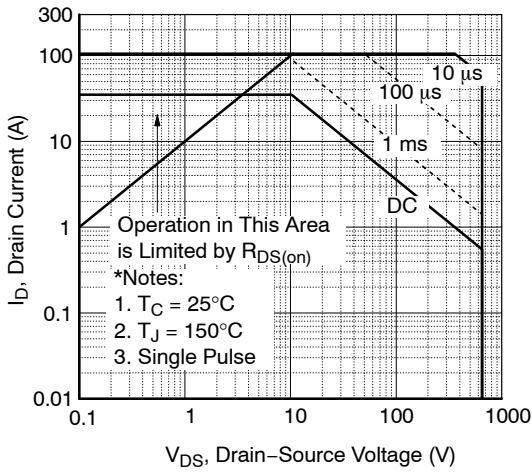
## TYPICAL PERFORMANCE CHARACTERISTICS (continued)



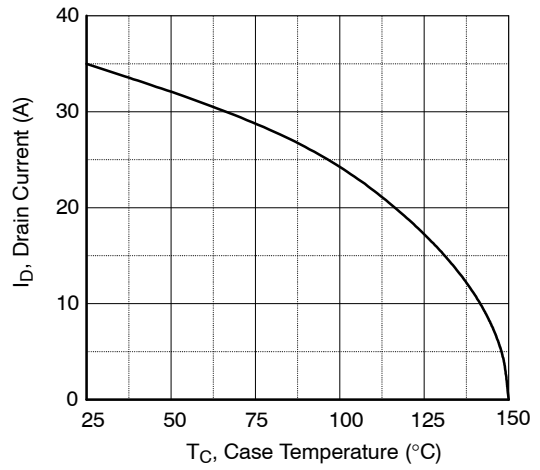
**Figure 7. Breakdown Voltage Variation vs. Temperature**



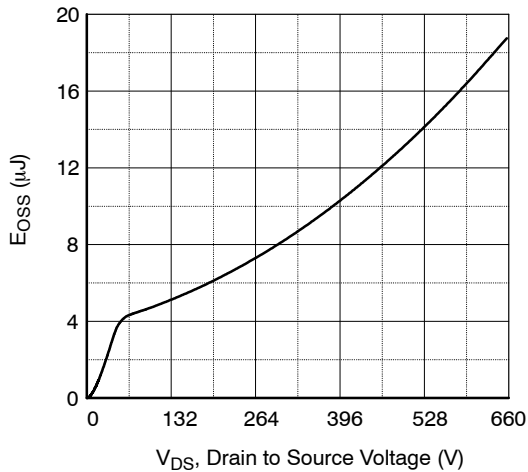
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11.  $E_{OSS}$  vs. Drain to Source Voltage**

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## TYPICAL PERFORMANCE CHARACTERISTICS (continued)

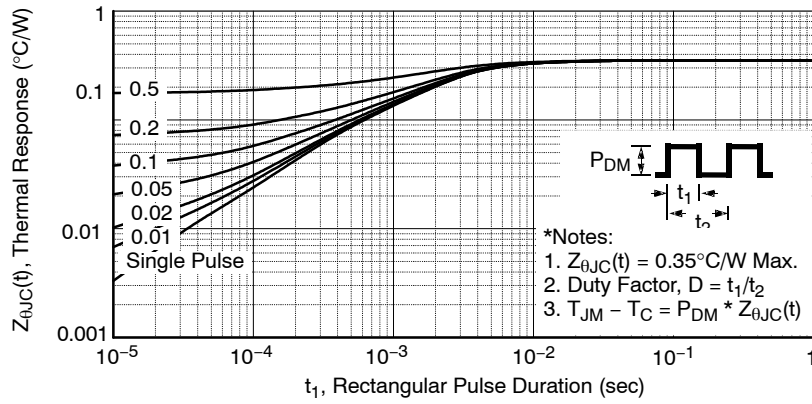


Figure 12. Transient Thermal Response Curve

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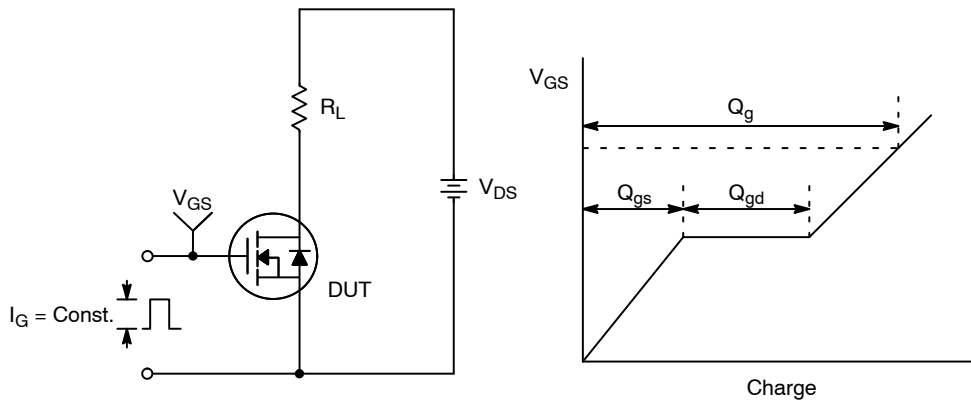


Figure 13. Gate Charge Test Circuit & Waveform

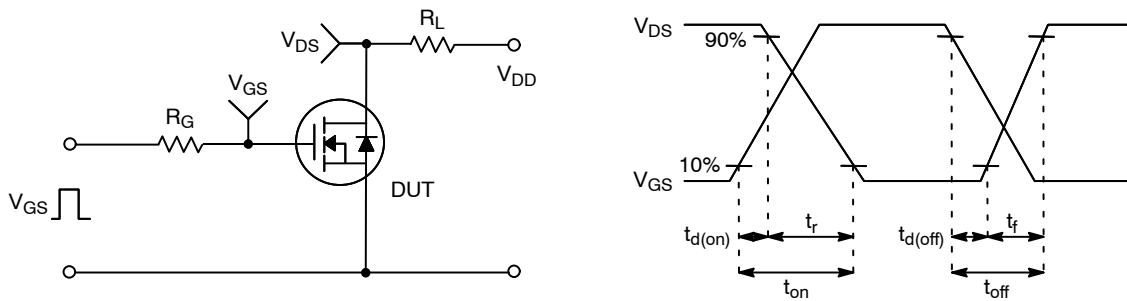


Figure 14. Resistive Switching Test Circuit & Waveforms

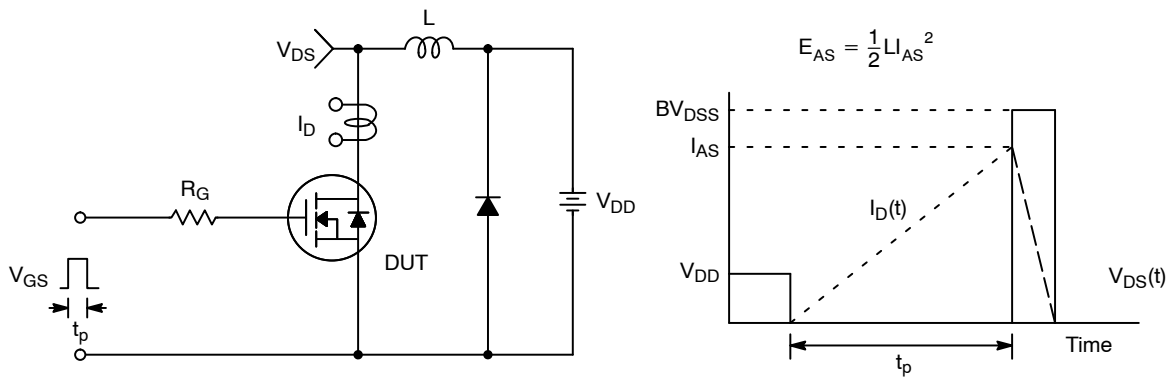
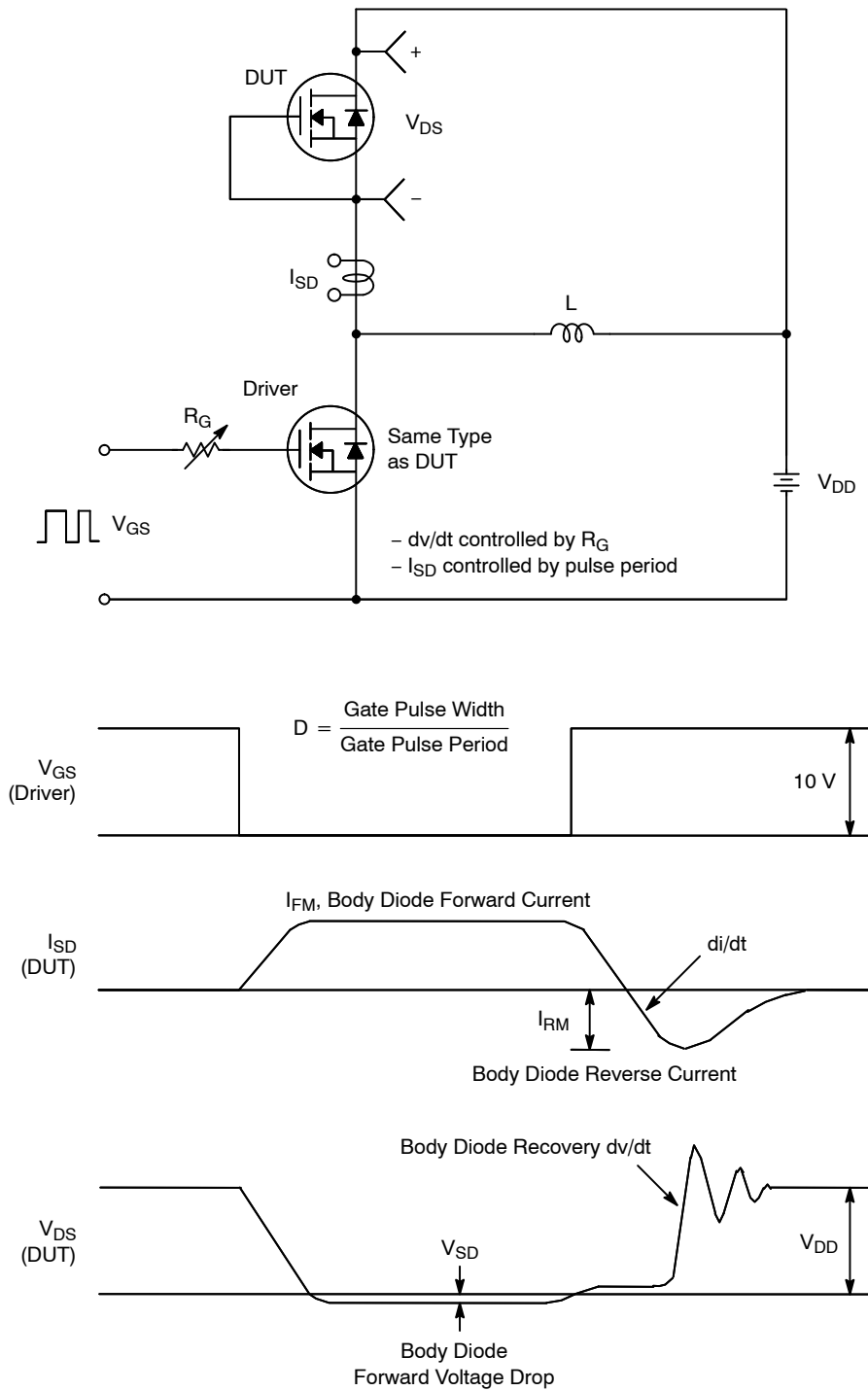


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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**Figure 16. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®



TO-247-3LD  
CASE 340CH  
ISSUE A

DATE 09 OCT 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.29	2.475	2.66
A2	1.40	1.50	1.60
D	20.32	20.57	20.82
E	15.37	15.62	15.87
E2	4.96	5.08	5.20
e	~	5.56	~
L	19.75	20.00	20.25
L1	3.69	3.81	3.93
∅P	3.51	3.58	3.65
Q	5.34	5.46	5.58
S	5.34	5.46	5.58
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D1	13.08	~	~
D2	0.51	0.93	1.35
E1	12.81	~	~
∅P1	6.61	6.73	6.85

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