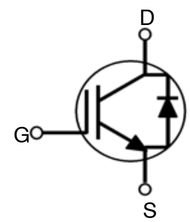
MOSFET – N-Channel, SUPERFET® II, FRFET®

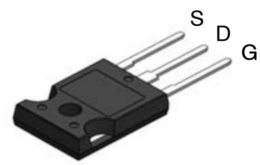
650 V, 54 A, 77 mΩ

FCH077N65F-F085

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
650 V	77 mΩ @ 10 V	54 A



N-CHANNEL MOSFET



TO−247−3LD
CASE 340CK

Description

SuperFET II MOSFET is **onsemi**'s brand−new high voltage super−junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on−resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently SuperFET II is very well suited for the Soft switching and Hard Switching topologies like High Voltage Full Bridge and Half Bridge DC−DC, Interleaved Boost PFC, Boost PFC for HEV−EV automotive.

SuperFET II FRFET MOSFET's optimized body diode reverse recovery performance can remove additional component and improve system reliability.

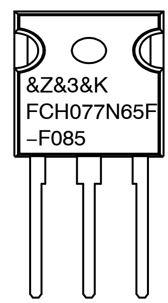
Features

- Typ. $R_{DS(on)}$ = 68 mΩ at V_{GS} = 10 V, I_D = 27 A
- Typ. $Q_{g(tot)}$ = 126 nC at V_{GS} = 10 V, I_D = 27 A
- UIS Capability
- AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Applications

- Automotive On Board Charger
- Automotive DC/DC Converter for HEV

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Numeric Date Code
&K	= Lot Code
FCH077N65F−F085	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

August, 2024 − Rev. 4

Publication Order Number:
FCH077N65F−F085/D

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	650	V
V_{GSS}	Gate to Source Voltage	±20	V
I_D	Drain Current − Continuous (V_{GS} = 10) (Note 1)	54	A
	Pulsed Drain Current	See Fig. 4	A
E_{AS}	Single Pulsed Avalanche Rating (Note 2)	1128	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	50	
P_D	Power Dissipation	481	W
	Derate Above 25°C	3.85	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range	−55 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. Current is limited by bondwire configuration.
2. Starting T_J = 25 °C, L = 18.65 mH, I_{AS} = 11 A, V_{DD} = 100 V during inductor charging and V_{DD} = 0 V during time in avalanche.
3. $I_{SD} \leq 27$ A, di/dt ≤ 200 A/μs, $V_{DD} \leq 380$ V, starting T_J = 25 °C.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FCH077N65F	FCH077N65F−F085	TO−247−3	−	−	30 Units

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.26	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max. (Note 4)	40	

4. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in^2 pad of 2oz copper.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition		Min.	Typ.	Max.	Unit
OFF CHARACTERISTICS							
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V		650	–	–	V
I_{DSS}	Drain to Source Leakage Current	V_{DS} = 650 V, V_{GS} = 0 V	T_J = 25 °C	–	–	10	μA
			T_J = 150 °C (Note 5)	–	–	1	mA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±20 V		–	–	±100	nA
ON CHARACTERISTICS							
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA		3	–	5	V
$R_{DS(on)}$	Drain to Source On Resistance	I_D = 27 A V_{GS} = 10 V	T_J = 25 °C	–	68	77	mΩ
			T_J = 150 °C (Note 5)	–	154	184	mΩ
DYNAMIC CHARACTERISTICS							
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz		–	5385	7162	pF
C_{oss}	Output Capacitance			–	5629	7486	pF
C_{rss}	Reverse Transfer Capacitance			–	194	–	pF
$C_{oss(eff.)}$	Effective Output Capacitance	V_{DS} = 0 V to 520 V, V_{GS} = 0 V		–	693	–	pF
R_g	Gate Resistance	f = 1 MHz		–	0.5	–	Ω
$Q_{g(tot)}$	Total Gate Charge	V_{DD} = 380 V, I_D = 27 A, V_{GS} = 10 V		–	126	164	nC
$Q_{g(th)}$	Threshold Gate Charge			–	9	12	nC
Q_{gs}	Gate to Source Gate Charge			–	28	–	nC
Q_{gd}	Gate to Drain “Miller”Charge			–	53	–	nC
SWITCHING CHARACTERISTICS							
t_{on}	Turn−On Time	V_{DD} = 380 V, I_D = 27 A, V_{GS} = 10 V, R_G = 4.7 Ω		–	64	148	ns
$t_{d(on)}$	Turn-On Delay Time			–	37	–	ns
t_r	Rise Time			–	27	–	ns
$t_{d(off)}$	Turn-Off Delay Time			–	105	–	ns
t_f	Fall Time			–	5.3	–	ns
t_{off}	Turn−Off Time			–	108.3	237	ns
DRAIN-SOURCE DIODE CHARACTERISTICS							
V_{SD}	Source to Drain Diode Voltage	V_{GS} = 0 V, I_{SD} = 27 A		–	–	1.2	V
t_{rr}	Reverse Recovery Time	V_{DD} = 520 V, I_F = 27 A, dI_{SD}/dt = 100 A/μs		–	190	–	ns
Q_{rr}	Reverse Recovery Charge			–	1.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. The maximum value is specified by design at T_J = 150°C. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

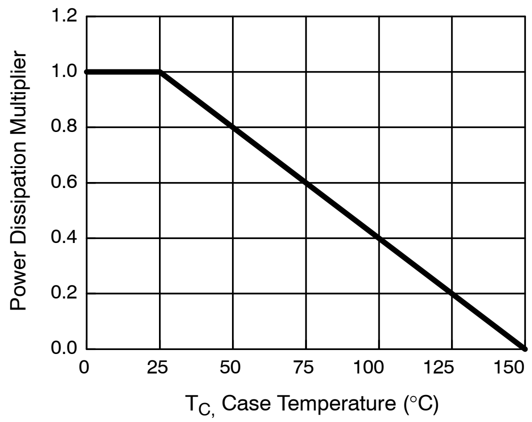


Figure 1. Normalized Power Dissipation vs. Case Temperature

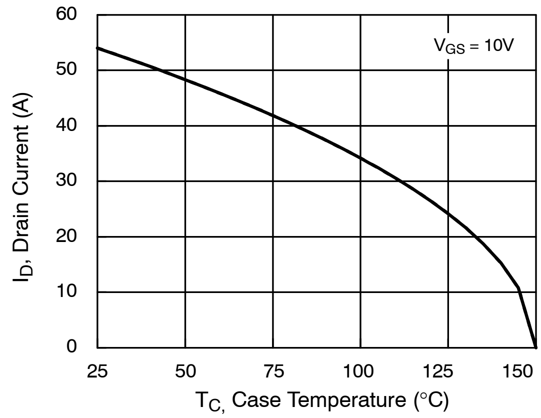


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

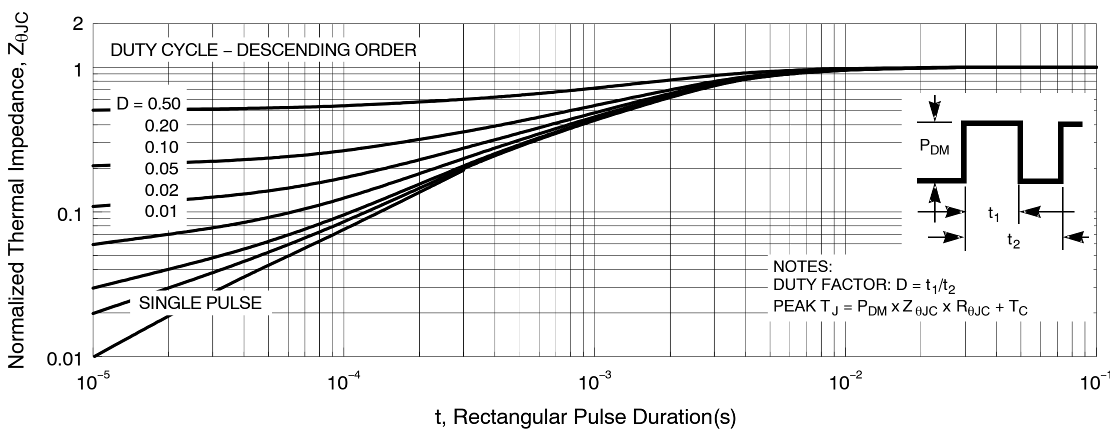


Figure 3. Normalized Maximum Transient Thermal Impedance

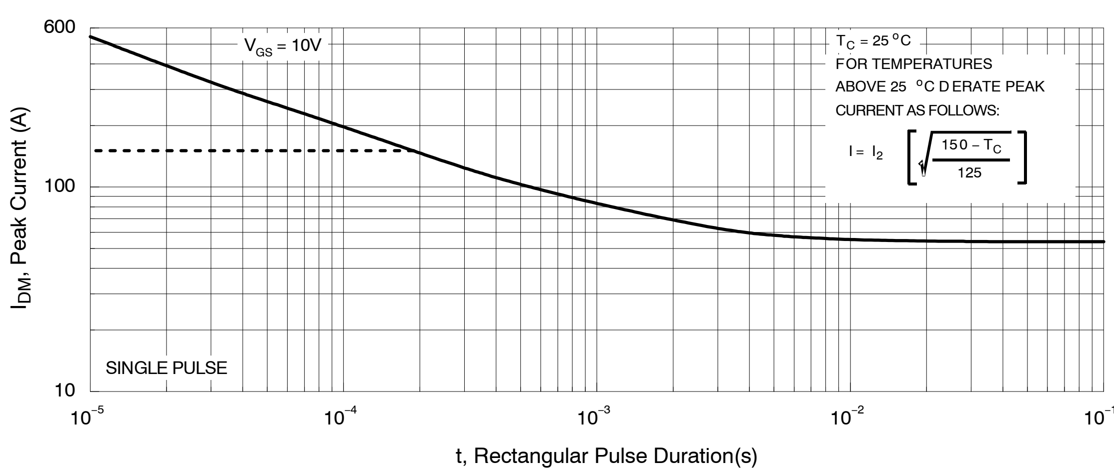


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

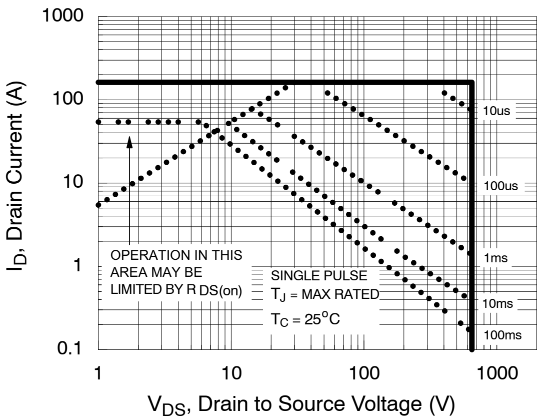


Figure 5. Forward Bias Safe Operating Area

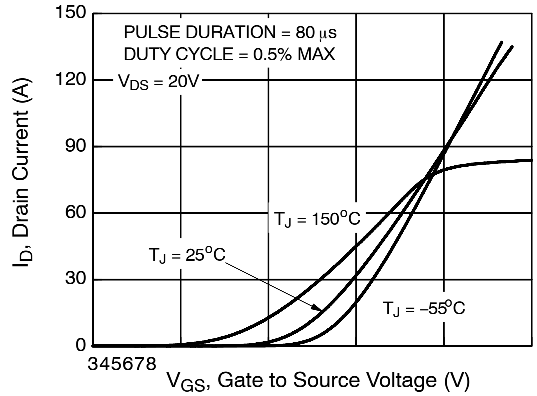


Figure 6. Transfer Characteristics

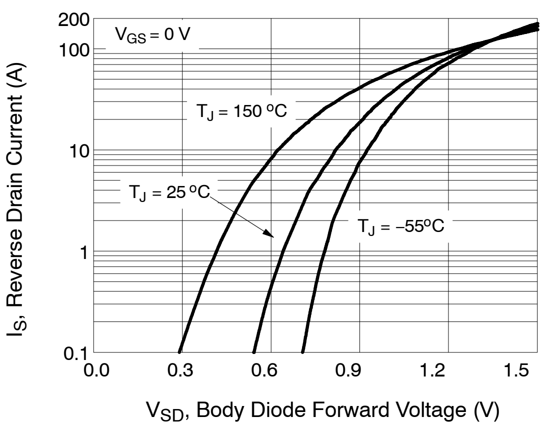


Figure 7. Forward Diode Characteristics

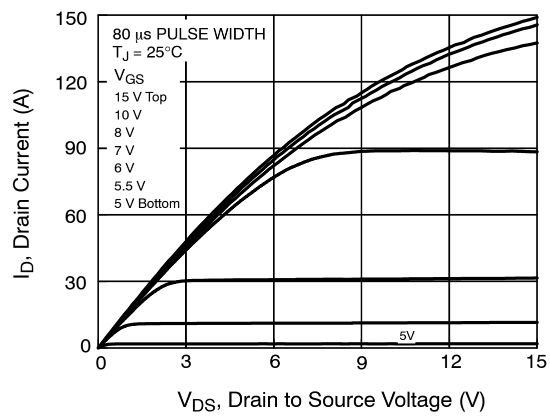


Figure 8. Saturation Characteristics

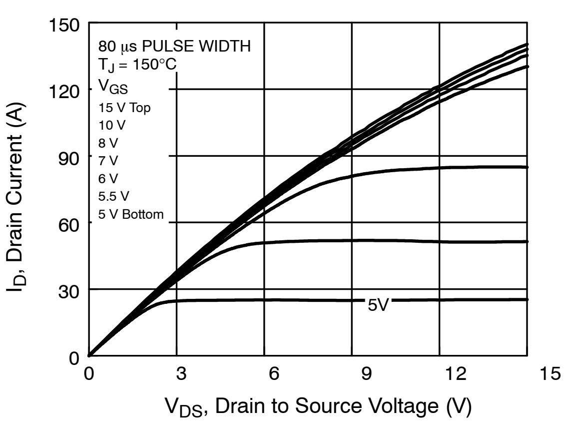


Figure 9. Saturation Characteristics

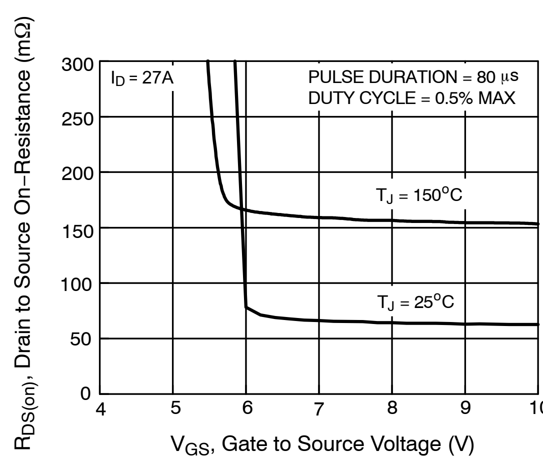


Figure 10. R_{DSON} vs. Gate Voltage

TYPICAL CHARACTERISTICS

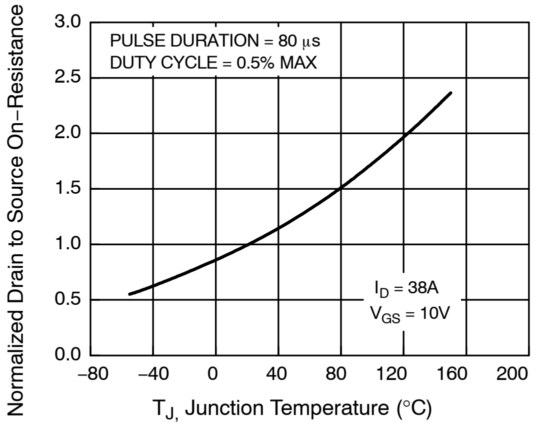


Figure 11. Normalized R_{DSON} vs. Junction Temperature

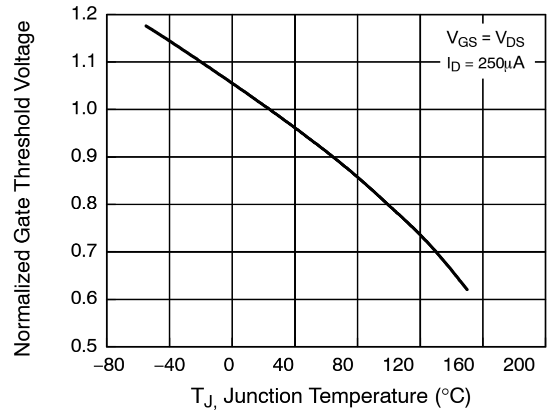


Figure 12. Normalized Gate Threshold Voltage vs. Temperature

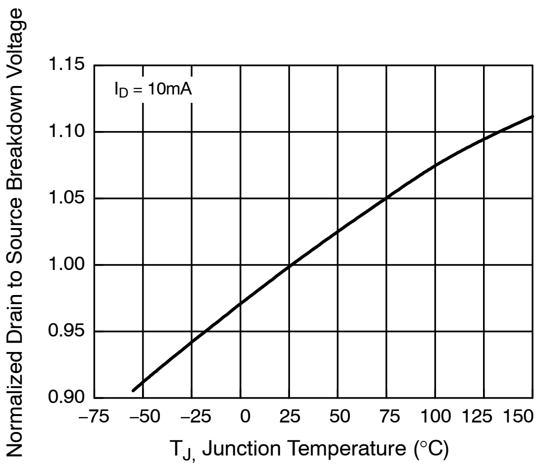


Figure 13. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

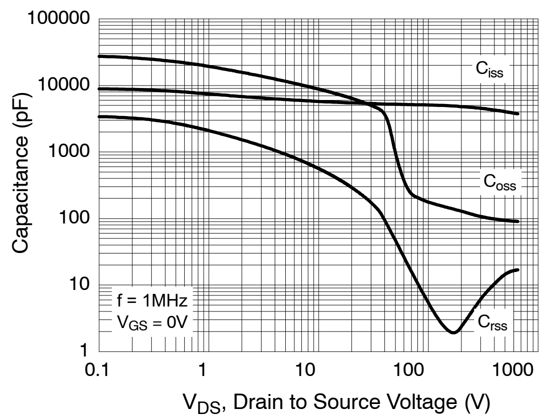


Figure 14. Capacitance vs. Drain to Source Voltage

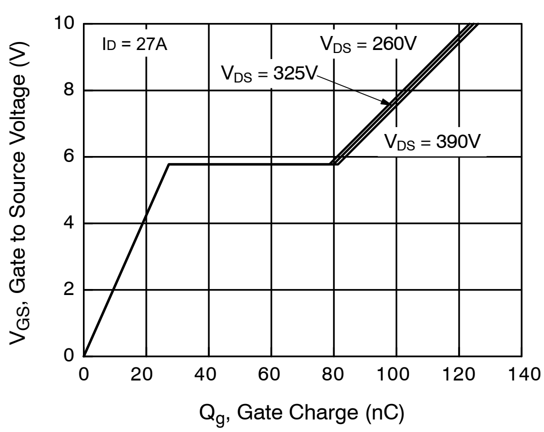


Figure 15. Gate Charge vs. Gate to Source Voltage

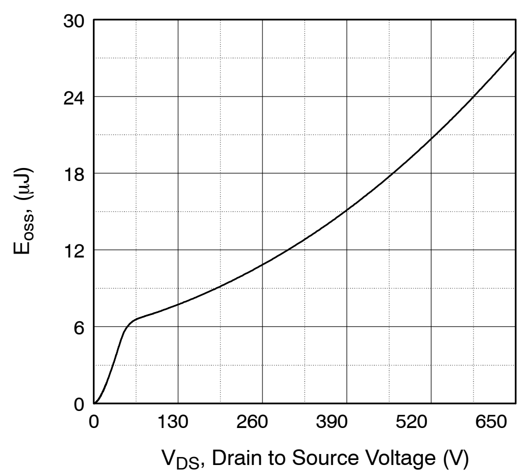


Figure 16. Eoss vs. Drain to Source Voltage

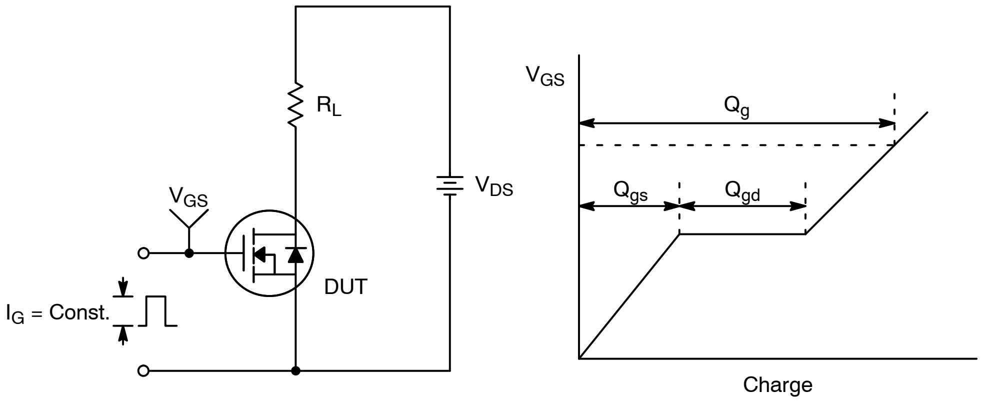


Figure 17. Gate Charge Test Circuit & Waveform

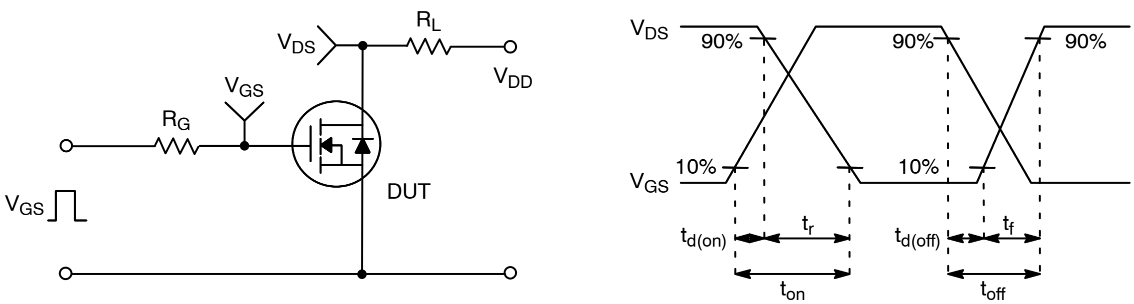


Figure 18. Resistive Switching Test Circuit & Waveforms

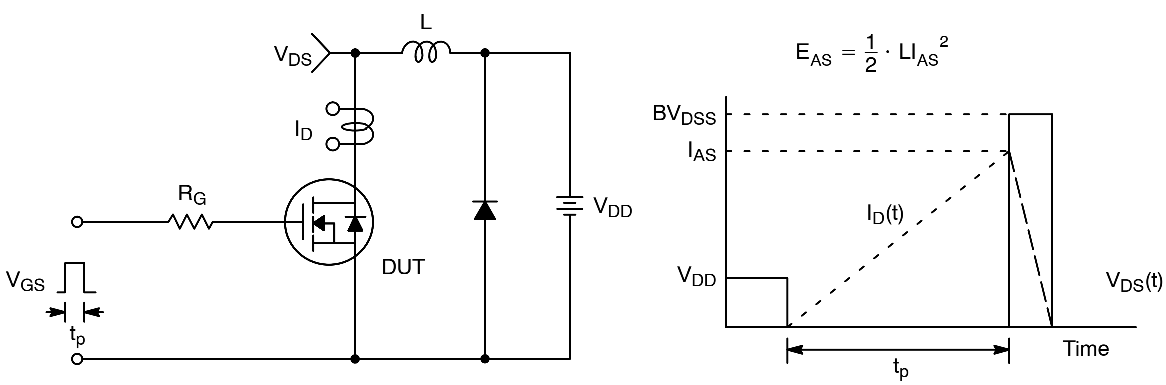


Figure 19. Unclamped Inductive Switching Test Circuit & Waveforms

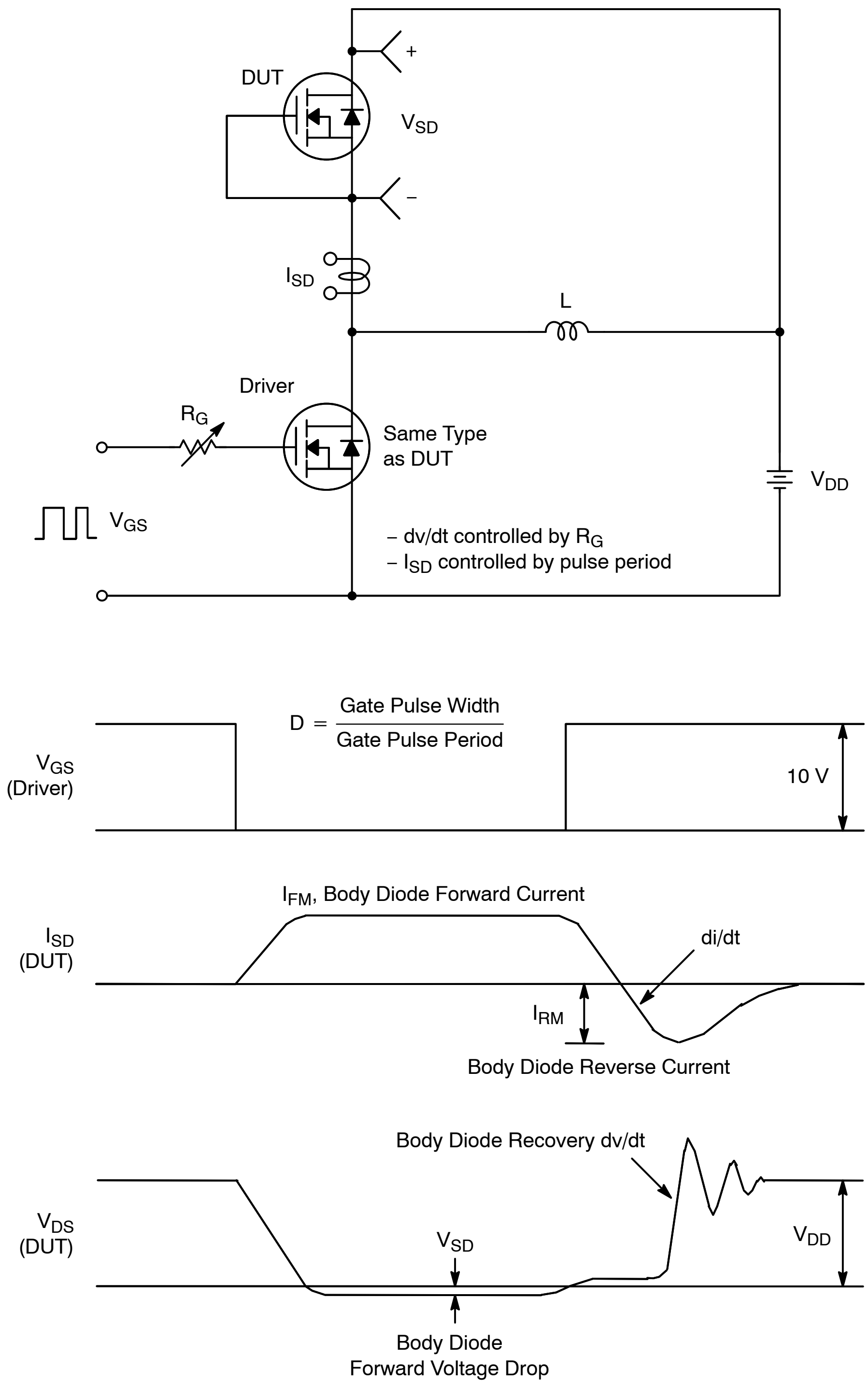
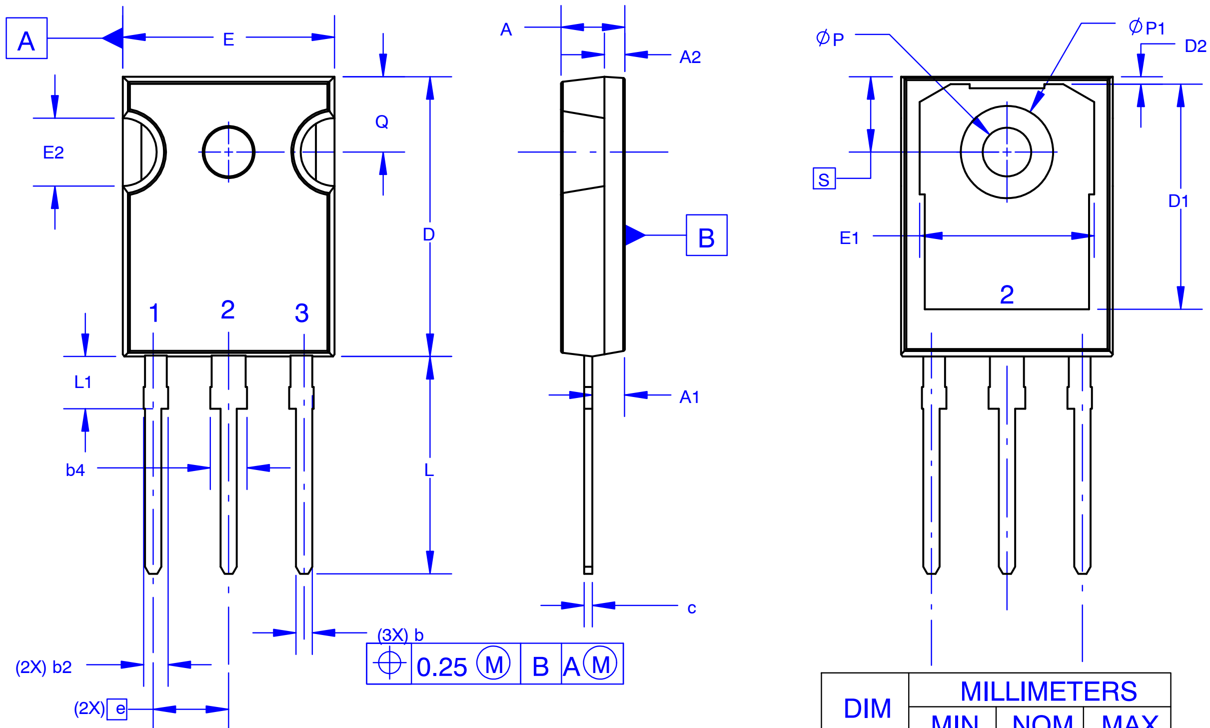


Figure 20. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO−247−3LD SHORT LEAD
CASE 340CK
ISSUE A

DATE 31 JAN 2019



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

NOTES: UNLESS OTHERWISE SPECIFIED.

A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
B. ALL DIMENSIONS ARE IN MILLIMETERS.
C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

GENERIC MARKING DIAGRAM*

AYWWZZ
XXXXXXX
XXXXXXX
∘

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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