

# MOSFET – N-Channel, SUPERFET<sup>®</sup> II, Easy-Drive

## 600 V, 77 A, 41 mΩ

### FCH041N60E

#### Description

SuperFET II MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET II MOSFET easy-drive series offers slightly slower rise and fall times compared to the SuperFET II MOSFET series. Noted by the "E" part number suffix, this family helps manage EMI issues and allows for easier design implementation. For faster switching in applications where switching losses must be at an absolute minimum, please consider the SuperFET II MOSFET series.

#### Features

- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 36\text{ m}\Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 285\text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 735\text{ pF}$ )
- 100% Avalanche Tested
- An Integrated Gate Resistor
- This Device is Pb-Free and is RoHS Compliant

#### Applications

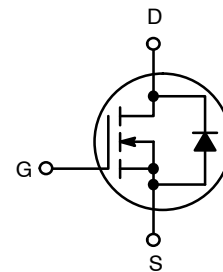
- LCD/LED/PDP TV Lighting
- Solar Inverter
- AC-DC Power Supply



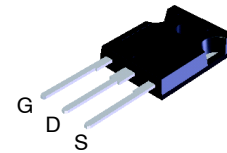
ON Semiconductor<sup>®</sup>

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$V_{DSS}$	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
600 V	41 mΩ	77 A

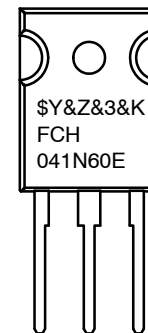


N-Channel MOSFET



TO-247  
CASE 340CK

#### MARKING DIAGRAM



- \$Y = ON Semiconductor Logo
- &Z = Assembly Plant Code
- &3 = Data Code (Year & Week)
- &K = Lot Code
- FCH041N60E = Specific Device Code

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FCH041N60E

## ABSOLUTE MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , Unless otherwise specified)

Symbol	Parameter		Value	Unit
$V_{DSS}$	Drain to Source Voltage		600	V
$V_{GSS}$	Gate to Source Voltage	DC	$\pm 20$	V
		AC ( $f > 1\text{ Hz}$ )	$\pm 30$	
$I_D$	Drain Current	Continuous ( $T_C = 25^\circ\text{C}$ )	77	A
		Continuous ( $T_C = 100^\circ\text{C}$ )	48.7	
$I_{DM}$	Drain Current	Pulsed (Note 1)	231	A
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)		2025	mJ
$I_{AS}$	Avalanche Current (Note 1)		15	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)		5.92	mJ
dv/dt	MOSFET dv/dt		100	V/ns
	Peak Diode Recovery dv/dt (Note 3)		20	
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	592	W
		Derate Above $25^\circ\text{C}$	4.74	W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.

2.  $I_{AS} = 15\text{ A}$ ,  $R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .

3.  $I_{SD} \leq 39\text{ A}$ ,  $di/dt \leq 200\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 380\text{ V}$ , starting  $T_J = 25^\circ\text{C}$ .

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.21	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FCH041N60E	FCH041N60E	TO-247	Tube	N/A	N/A	30 Units

# FCH041N60E

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 25°C	600	–	–	V
		V <sub>GS</sub> = 0 V, I <sub>D</sub> = 10 mA, T <sub>J</sub> = 150°C	650	–	–	V
ΔBV <sub>DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 10 mA, Referenced to 25°C	–	0.67	–	V/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 600 V, V <sub>GS</sub> = 0 V	–	–	1	μA
		V <sub>DS</sub> = 480 V, V <sub>GS</sub> = 0 V, T <sub>C</sub> = 125°C	–	9.7	–	
I <sub>GSS</sub>	Gate to Body Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	–	–	±100	nA

### ON CHARACTERISTICS

V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2.5	–	3.5	V
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 39 A	–	36	41	mΩ
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 39 A	–	71	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	10300	13700	pF
C <sub>oss</sub>	Output Capacitance		–	355	475	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	4	6	pF
C <sub>oss</sub>	Output Capacitance	V <sub>DS</sub> = 380 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	187	–	pF
C <sub>oss(eff.)</sub>	Effective Output Capacitance	V <sub>DS</sub> = 0 V to 480 V, V <sub>GS</sub> = 0 V	–	735	–	pF
Q <sub>g(tot)</sub>	Total Gate Charge at 10 V	V <sub>DS</sub> = 380 V, I <sub>D</sub> = 39 A, V <sub>GS</sub> = 10 V (Note 4)	–	285	380	nC
Q <sub>gs</sub>	Gate to Source Gate Charge		–	45	–	nC
Q <sub>gd</sub>	Gate to Drain "Miller" Charge		–	105	–	nC
ESR	Equivalent Series Resistance	f = 1 MHz	–	1.2	–	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 380 V, I <sub>D</sub> = 39 A, V <sub>GS</sub> = 10 V, R <sub>G</sub> = 4.7 Ω (Note 4)	–	50	110	ns
t <sub>r</sub>	Turn-On Rise Time		–	50	110	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	320	650	ns
t <sub>f</sub>	Turn-Off Fall Time		–	85	180	ns

### SOURCE-DRAIN DIODE CHARACTERISTICS

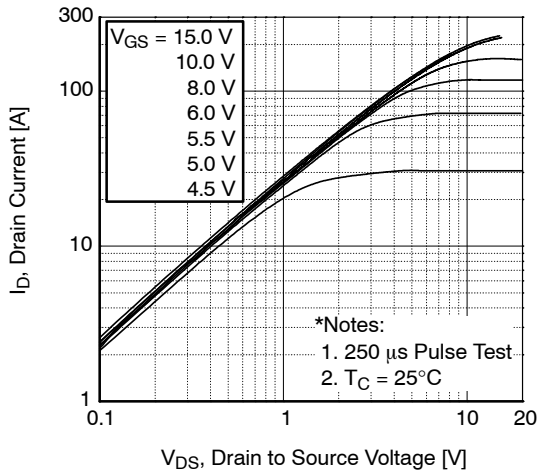
I <sub>S</sub>	Maximum Continuous Source to Drain Diode Forward Current	–	–	77	A	
I <sub>SM</sub>	Maximum Pulsed Source to Drain Diode Forward Current	–	–	231	A	
V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 39 A	–	–	1.2	V
t <sub>rr</sub>	Reverse Recovery Time	V <sub>GS</sub> = 0 V, I <sub>SD</sub> = 39 A, dI <sub>F</sub> /dt = 100 A/μs	–	590	–	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	18	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

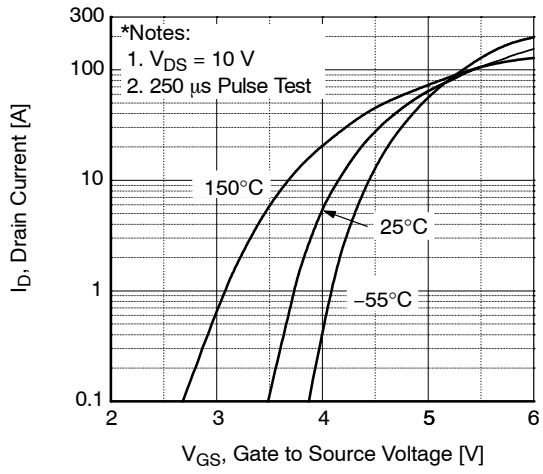
4. Essentially independent of operating temperature.

# FCH041N60E

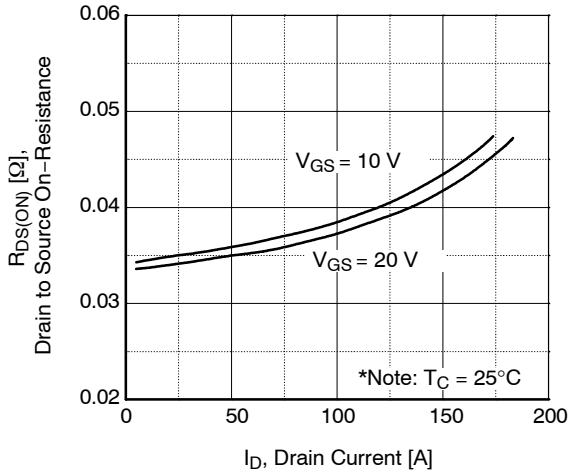
## TYPICAL CHARACTERISTICS



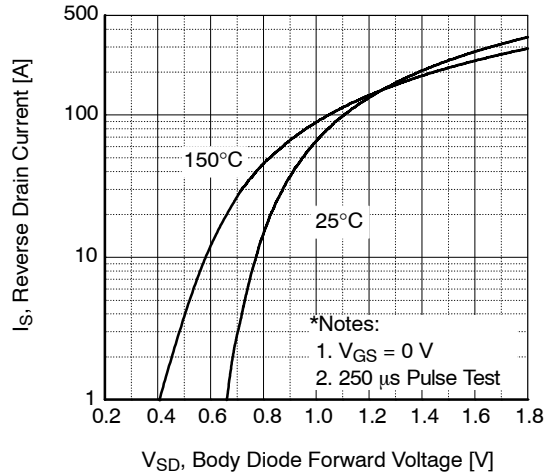
**Figure 1. On-Region Characteristics**



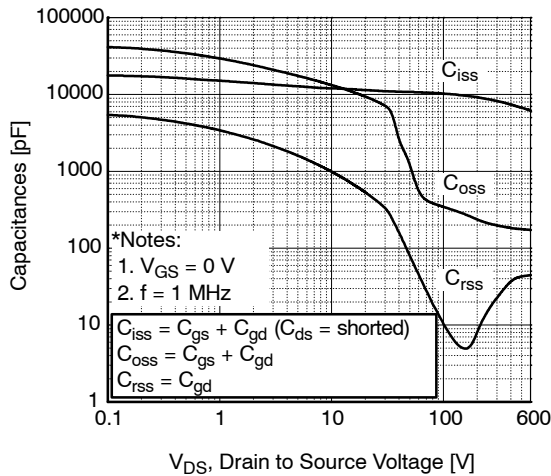
**Figure 2. Transfer Characteristics**



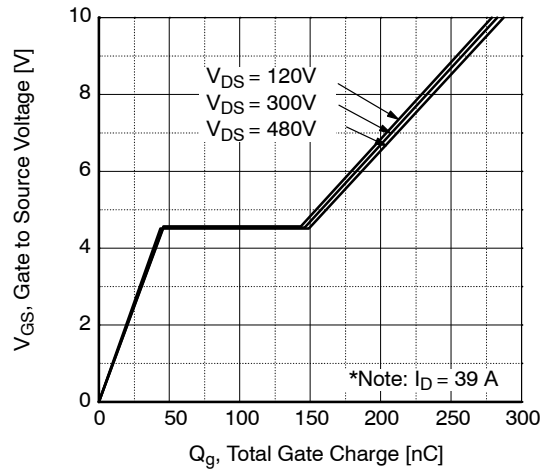
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**

TYPICAL CHARACTERISTICS (Continued)

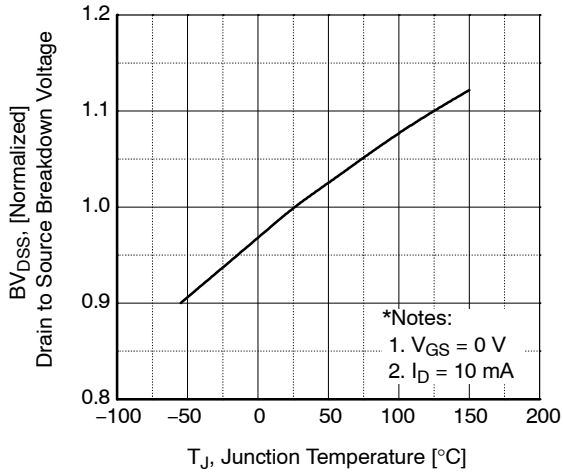


Figure 7. Breakdown Voltage Variation vs. Temperature

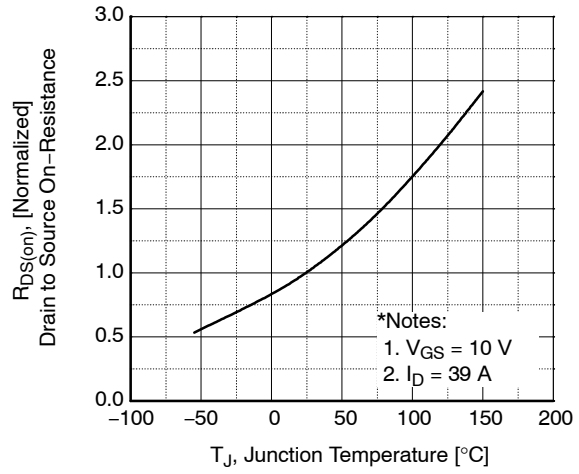


Figure 8. On-Resistance Variation vs. Temperature

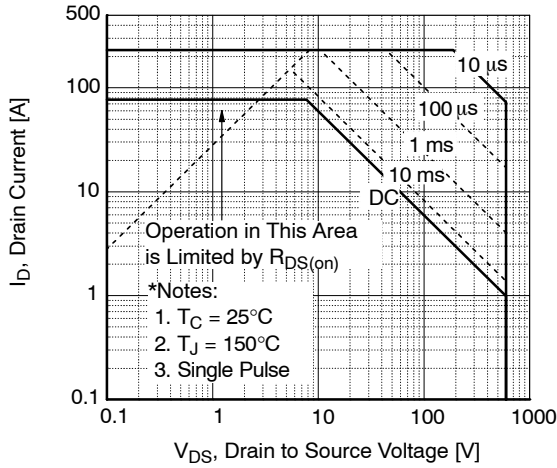


Figure 9. Maximum Safe Operation Area

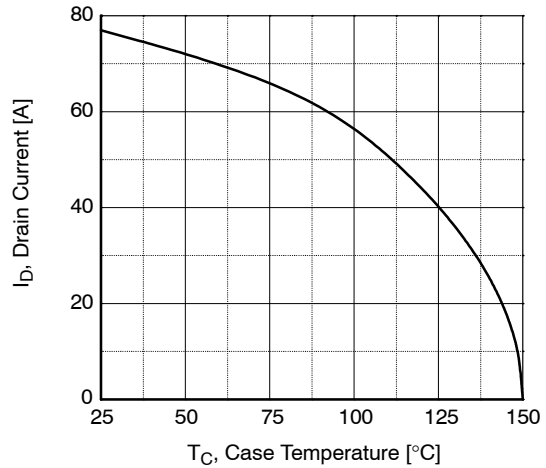


Figure 10. Maximum Drain Current vs. Case Temperature

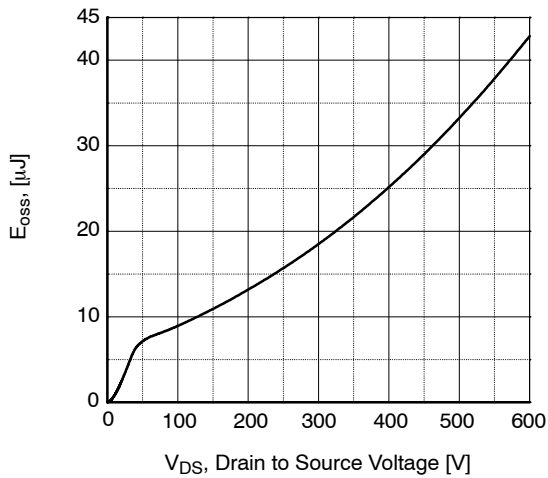


Figure 11.  $E_{OSS}$  vs. Drain to Source Voltage

# FCH041N60E

## TYPICAL CHARACTERISTICS (Continued)

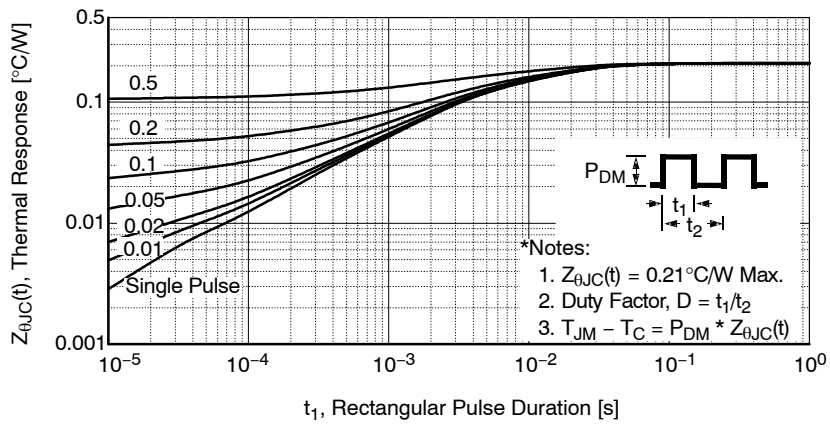


Figure 12. Transient Thermal Response Curve

# FCH041N60E



Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms

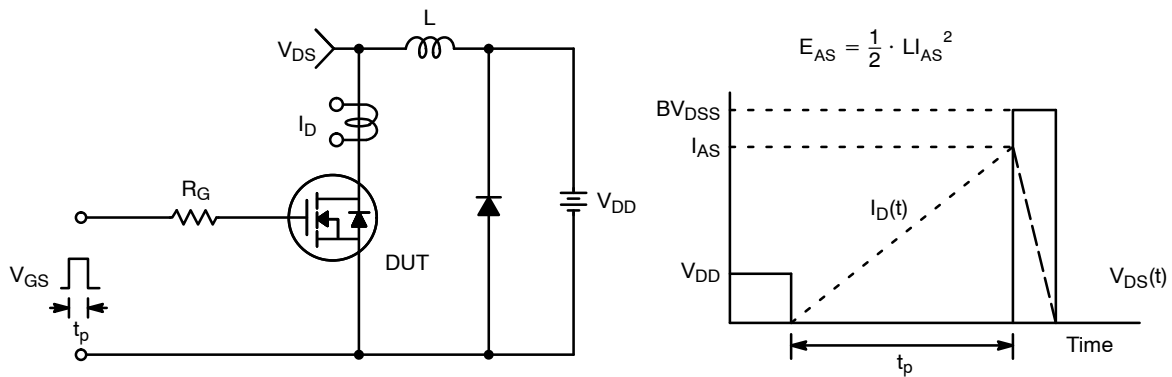
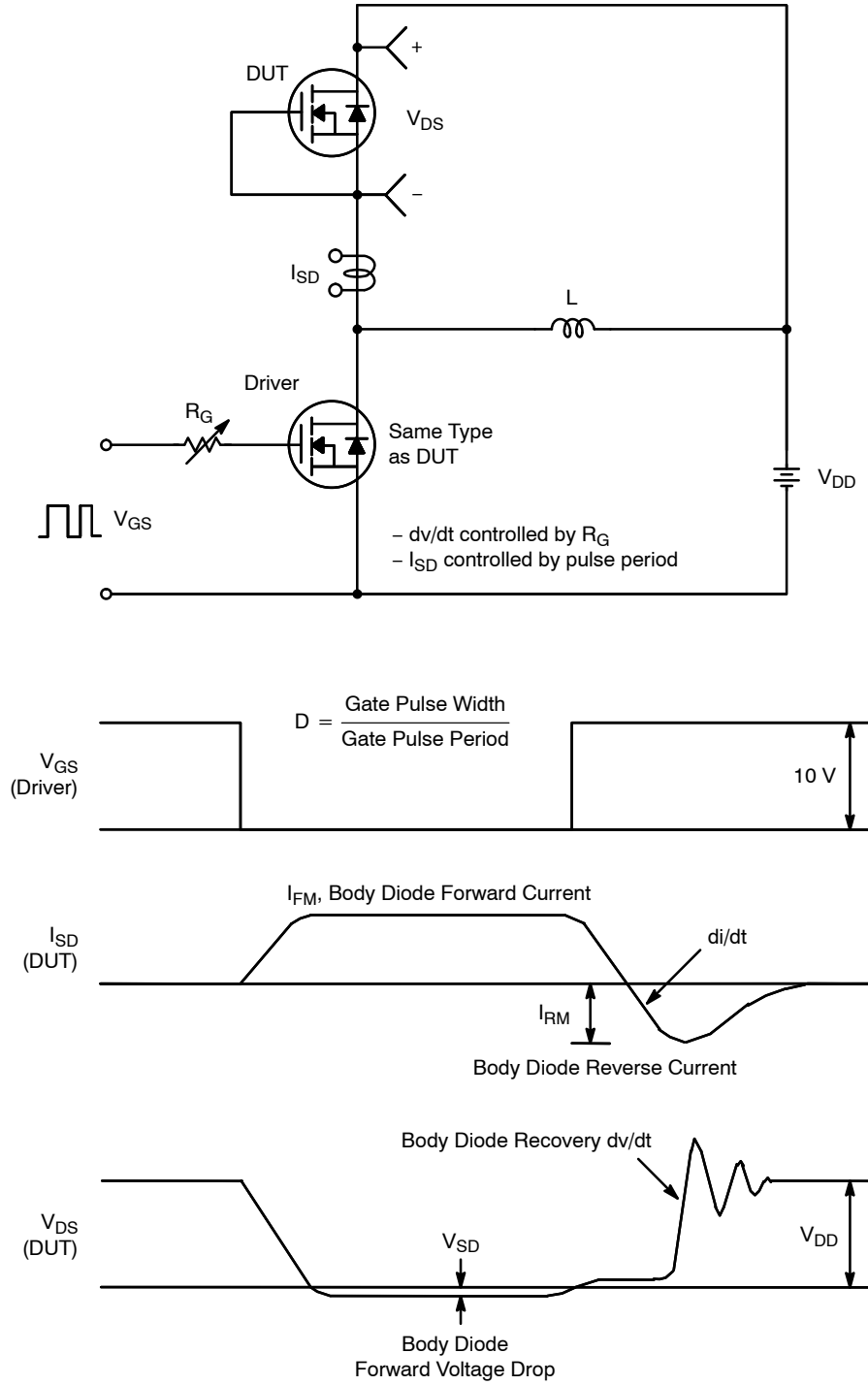


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

# FCH041N60E



**Figure 16. Peak Diode Recovery  $d v / d t$  Test Circuit & Waveforms**

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**TO-247-3LD SHORT LEAD**  
**CASE 340CK**  
**ISSUE A**

DATE 31 JAN 2019



NOTES: UNLESS OTHERWISE SPECIFIED.

- A. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DRAWING CONFORMS TO ASME Y14.5 - 2009.
- D. DIMENSION A1 TO BE MEASURED IN THE REGION DEFINED BY L1.
- E. LEAD FINISH IS UNCONTROLLED IN THE REGION DEFINED BY L1.

**GENERIC MARKING DIAGRAM\***



XXXX = Specific Device Code  
 A = Assembly Location  
 Y = Year  
 WW = Work Week  
 ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.58	4.70	4.82
A1	2.20	2.40	2.60
A2	1.40	1.50	1.60
b	1.17	1.26	1.35
b2	1.53	1.65	1.77
b4	2.42	2.54	2.66
c	0.51	0.61	0.71
D	20.32	20.57	20.82
D1	13.08	~	~
D2	0.51	0.93	1.35
E	15.37	15.62	15.87
E1	12.81	~	~
E2	4.96	5.08	5.20
e	~	5.56	~
L	15.75	16.00	16.25
L1	3.69	3.81	3.93
ØP	3.51	3.58	3.65
ØP1	6.60	6.80	7.00
Q	5.34	5.46	5.58
S	5.34	5.46	5.58

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