

FCD260N65S3

MOSFET – Power, N-Channel, SUPERFET III, Easy Drive

650 V, 12 A, 260 mΩ

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 222\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 24\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 248\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

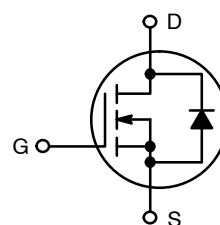
- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter



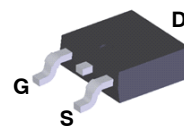
ON Semiconductor®

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V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	260 mΩ @ 10 V	12 A

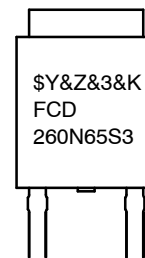


POWER MOSFET



D-PAK
CASE 369AS

MARKING DIAGRAM



\$Y = ON Semiconductor Logo
&Z = Assembly Plant Code
&3 = Data Code (Year & Week)
&K = Lot
FCD260N65S3 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FCD260N65S3

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	DC	±30
		AC (f > 1 Hz)	±30
I _D	Drain Current	Continuous (T _C = 25°C)	12
		Continuous (T _C = 100°C)	7.6
I _{DM}	Drain Current	Pulsed (Note 1)	30
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	57	mJ
I _{AS}	Avalanche Current (Note 1)	2.3	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	0.9	mJ
dv/dt	MOSFET dv/dt	100	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	90
		Derate Above 25°C	0.72
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s	300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 2.3 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 6 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	1.39	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max. (Note 4)	40	

4. Device on 1 in² pad 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping†
FCD260N65S3	FCD260N65S3	D-PAK	330 mm	16 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

FCD260N65S3

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 1 mA, Referenced to 25°C		0.66		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V			1	μA
		V _{DS} = 520 V, T _C = 125°C		0.77		
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 0.29 mA	2.5		4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 6 A		222	260	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 6 A		7.4		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 1 MHz		1010		pF
C _{oss}	Output Capacitance			25		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		248		pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		33		pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 6 A, V _{GS} = 10 V (Note 5)		24		nC
Q _{gs}	Gate to Source Gate Charge			6.1		nC
Q _{gd}	Gate to Drain "Miller" Charge			9.7		nC
ESR	Equivalent Series Resistance	f = 1 MHz		8.7		Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 6 A, V _{GS} = 10 V, R _g = 4.7 Ω (Note 5)		18		ns
t _r	Turn-On Rise Time			18		ns
t _{d(off)}	Turn-Off Delay Time			49		ns
t _f	Turn-Off Fall Time			12		ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current			12		A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current			30		A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 6 A			1.2	V
t _{rr}	Reverse Recovery Time	V _{DD} = 400 V, I _{SD} = 6 A, dI _F /dt = 100 A/μs		251		ns
Q _{rr}	Reverse Recovery Charge			3.4		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

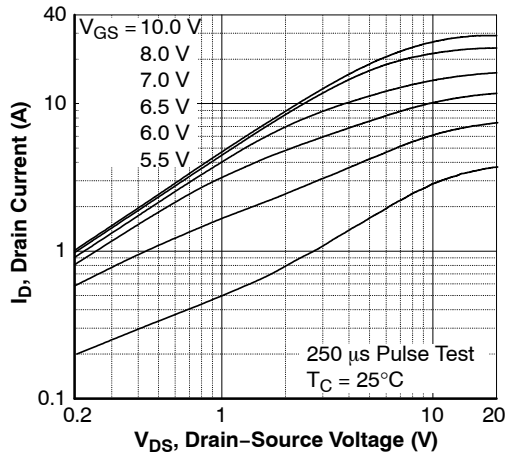


Figure 1. On-Region Characteristics

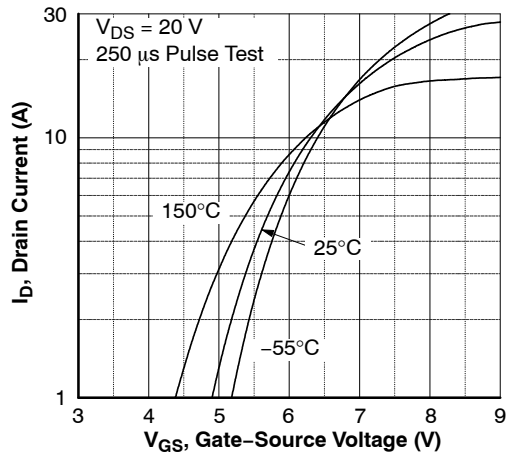


Figure 2. Transfer Characteristics

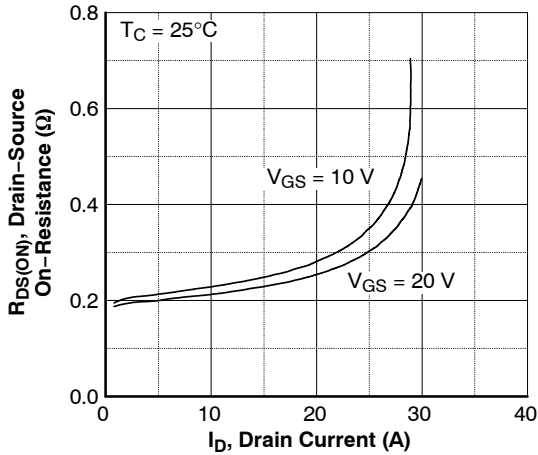


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

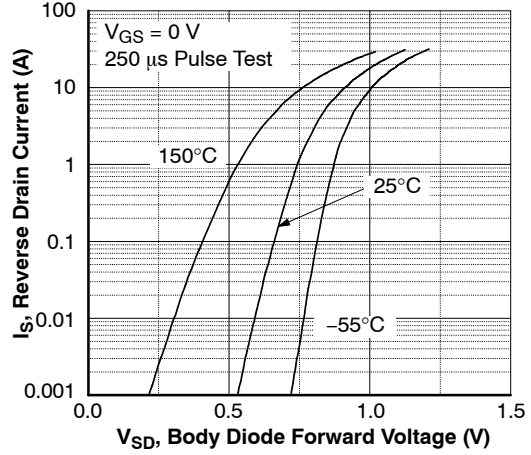


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

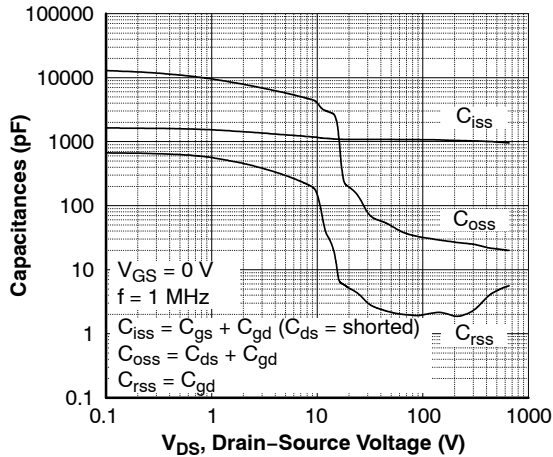


Figure 5. Capacitance Characteristics

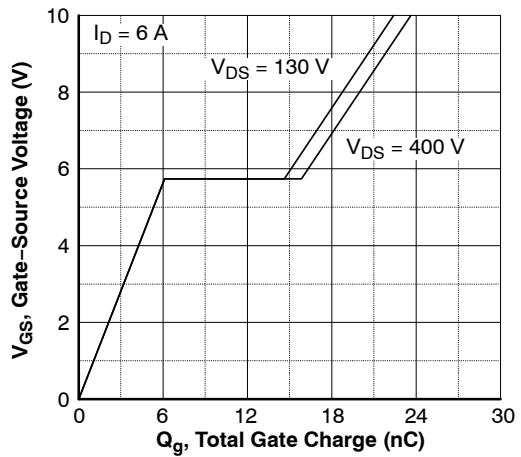


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

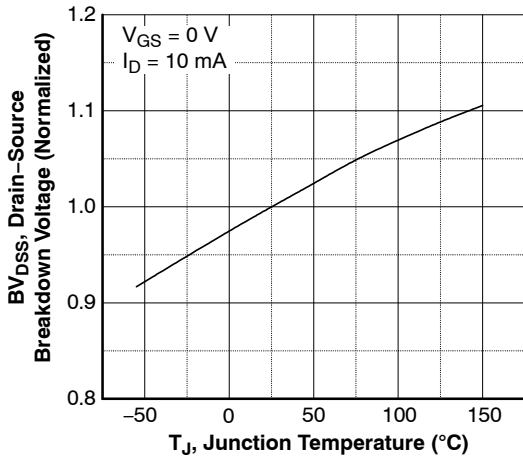


Figure 7. Breakdown Voltage Variation vs. Temperature

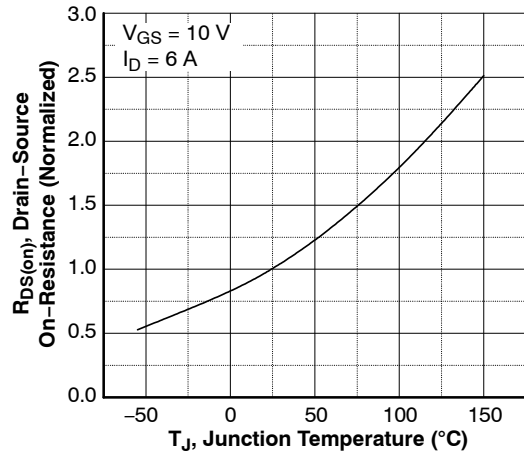


Figure 8. On-Resistance Variation vs. Temperature

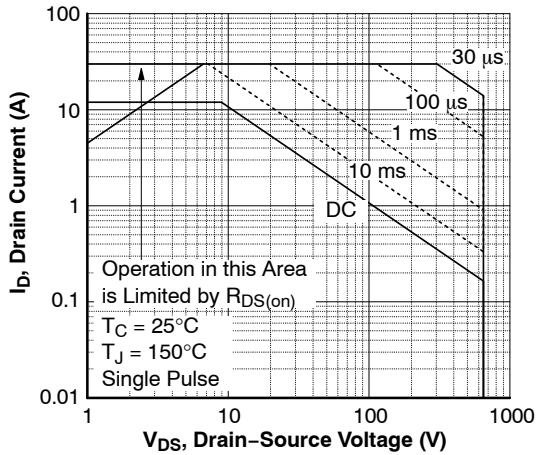


Figure 9. Maximum Safe Operating Area

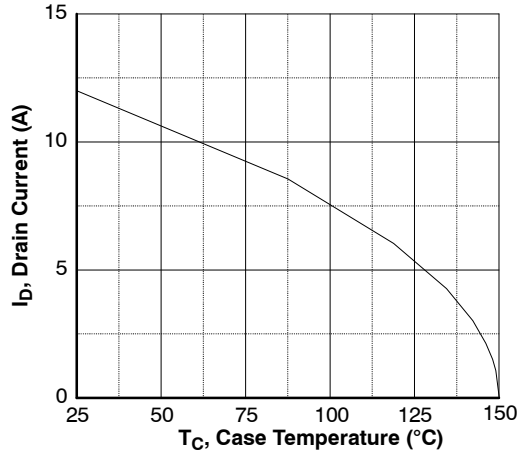


Figure 10. Maximum Drain Current vs. Case Temperature

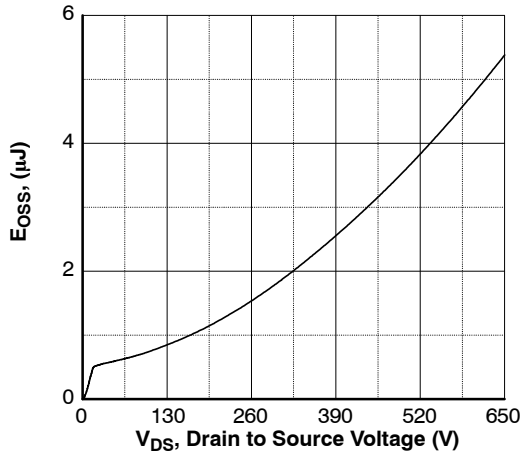


Figure 11. E_{OSS} vs. Drain to Source Voltage

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TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

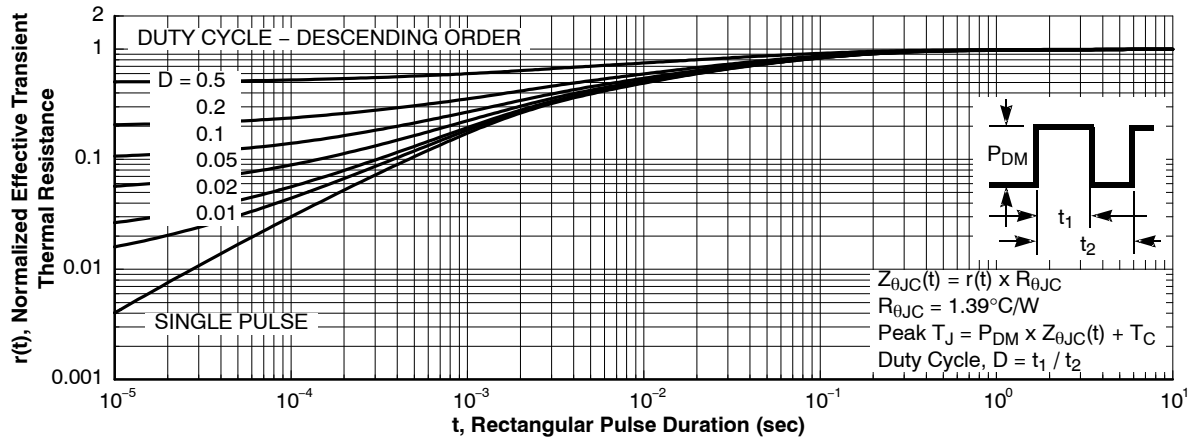


Figure 12. Transient Thermal Response Curve



Figure 13. Gate Charge Test Circuit & Waveform



Figure 14. Resistive Switching Test Circuit & Waveforms



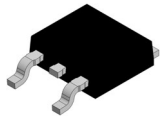
Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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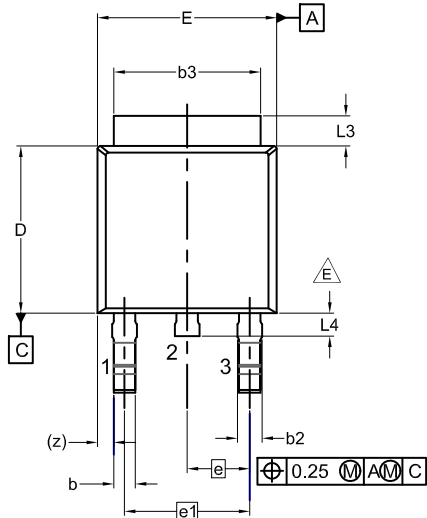
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

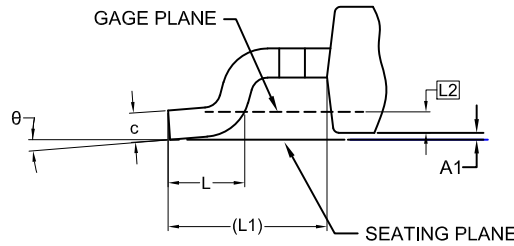


DPAK3 (TO-252 3 LD) CASE 369AS ISSUE A

DATE 28 SEP 2022

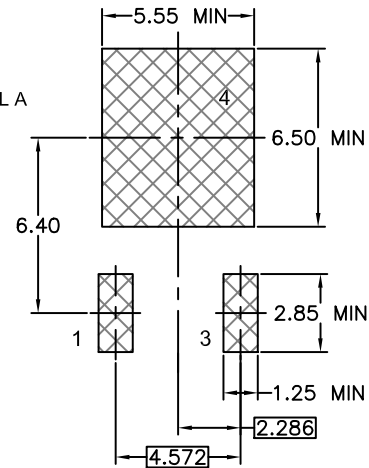
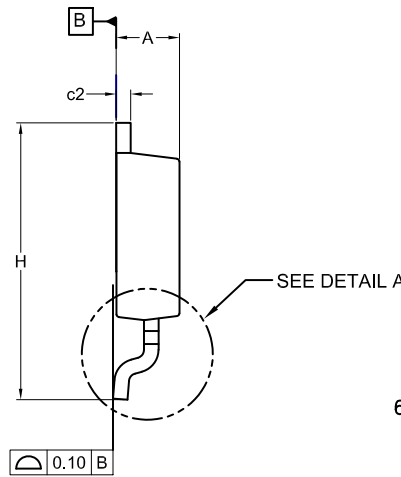
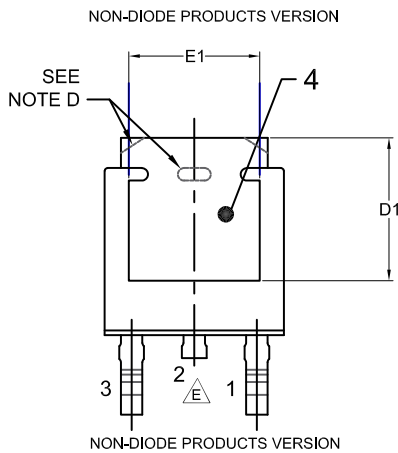


- NOTES: UNLESS OTHERWISE SPECIFIED
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
 E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



DETAIL A
(ROTATED -90°)
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	-	-
E	6.35	6.54	6.73
E1	4.32	-	-
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	-	-	1.02
θ	0°	--	10°



GENERIC MARKING DIAGRAM*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

LAND PATTERN RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

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