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FAIRCHILD SEMICONDUCTOR®

July 2012

FAN7384
Half-Bridge Gate-Drive IC

Features

- Floating Channel for Bootstrap Operation to +600V
- Typically 250mA/500mA Sourcing/Sinking Current Driving Capability for Both Channels
- Extended Allowable Negative V_S Swing to -9.8V for Signal Propagation at V_{DD}=V_{BS}=15V
- Matched Propagation Delay Below 50ns
- Output In-Phase with Input Signal
- 3.3V and 5V Input Logic Compatible
- Built-in Shoot-Through Prevention Logic
- Built-in Common Mode dv/dt Noise Canceling Circuit
- Built-in UVLO Functions for Both Channels
- Built-in Cycle-by-Cycle Shutdown Function
- Built-in Soft-Off Function
- Built-in Bi-Directional Fault Function
- Built-in Short-Circuit Protection Function

Applications

- Motor Inverter Driver
- Normal Half-Bridge and Full-Bridge Driver
- Switching Mode Power Supply

Description

The FAN7384 is a monolithic half-bridge gate-drive IC designed for high voltage, high speed driving MOSFETs and IGBTs operating up to +600V.

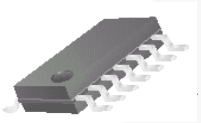
Fairchild's high-voltage process and common-mode noise canceling technique provide stable operation of high-side drivers under high-dv/dt noise circumstances.

An advanced level-shift circuit allows high-side gate driver operation up to V_S = -9.8V (typical) for V_{BS} =15V.

The UVLO circuits prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage.

Output drivers typically source/sink 250mA/500mA, respectively, which is suitable for half-bridge and full-bridge applications in motor drive systems.

14-SOP



Ordering Information

Part Number	Package	Operating Temperature Range	Packing Method
FAN7384MX(1)	14-Lead, Small Outline Integrated Circuit (SOIC), Non-JEDEC, .150 Inch Narrow Body, 225SOP	-40°C to +125°C	Tape & Reel

Note:

1. The device passed wave soldering test by JESD22A-111.

Typical Application Diagrams

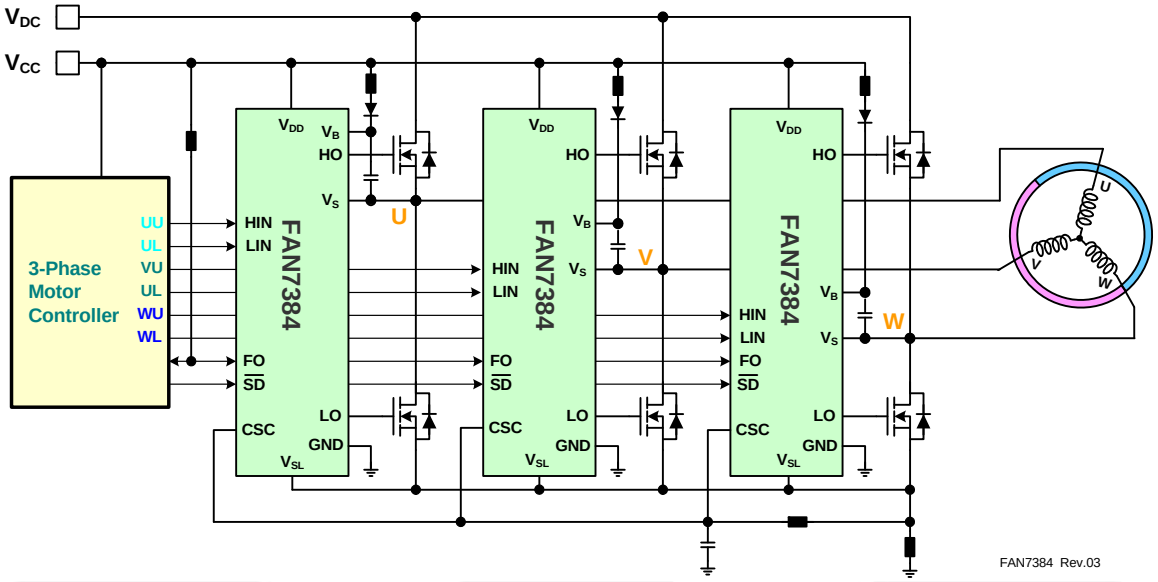


Figure 1. 3-Phase Motor Drive Application

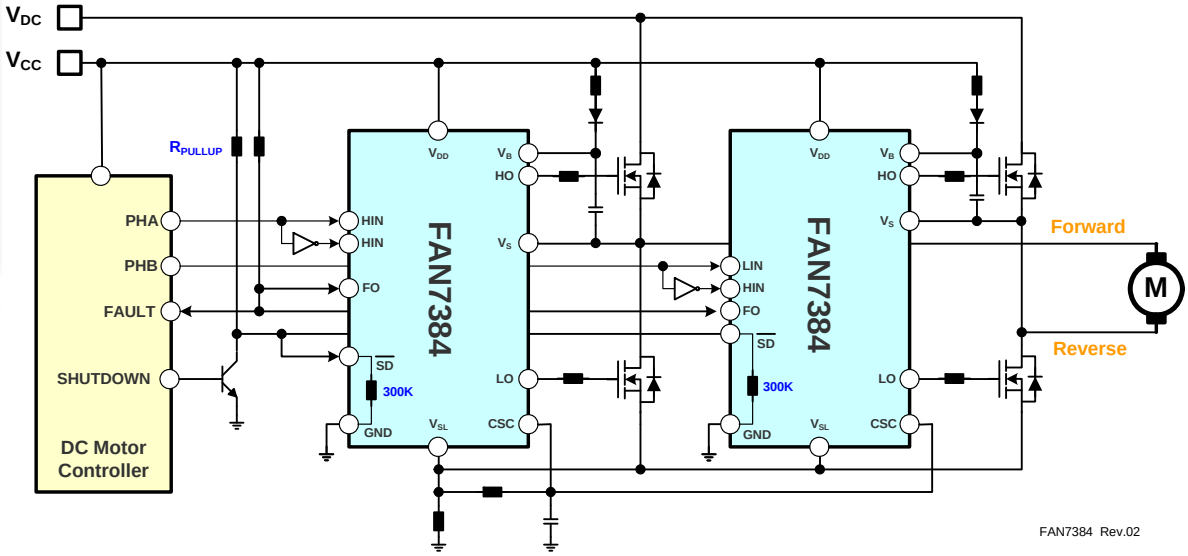


Figure 2. DC Motor Drive Application

Internal Block Diagram

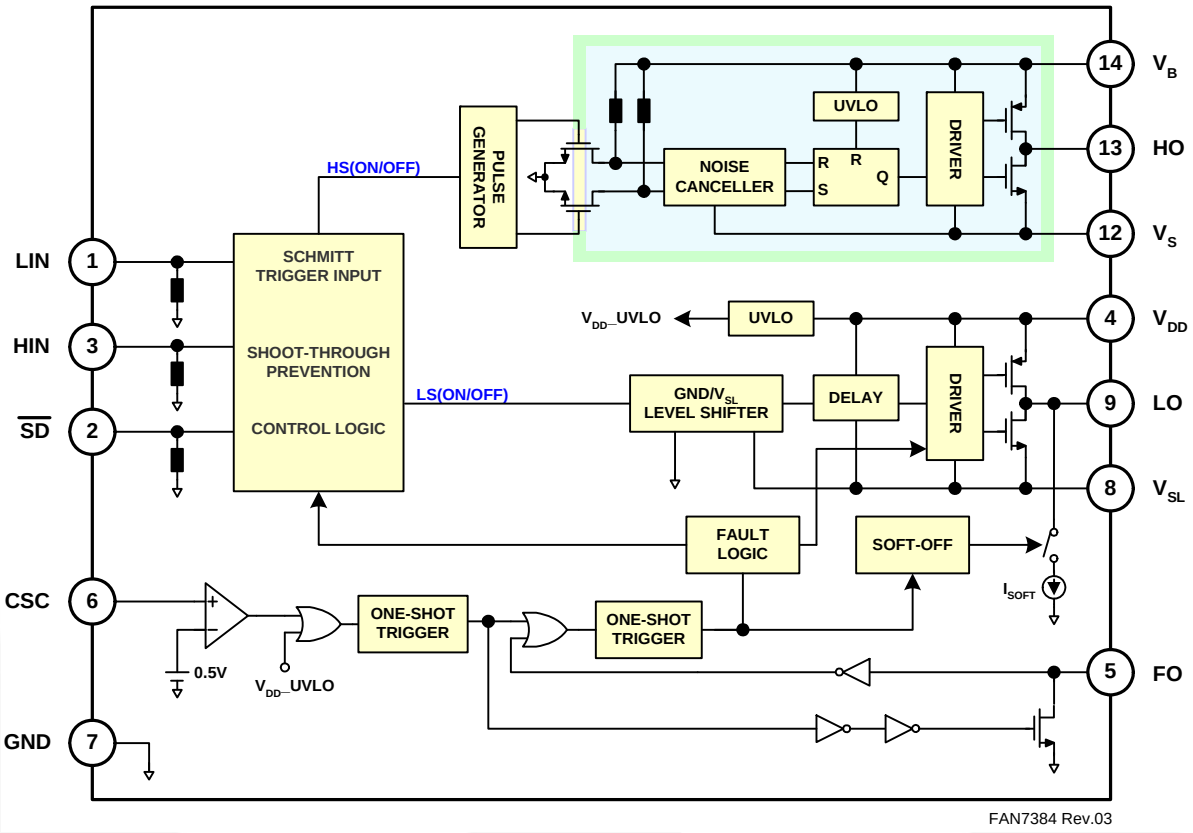


Figure 3. Functional Block Diagram

Switching Time Definitions

The overall switching timing waveforms definition of FAN7384 as shown Figure 33.

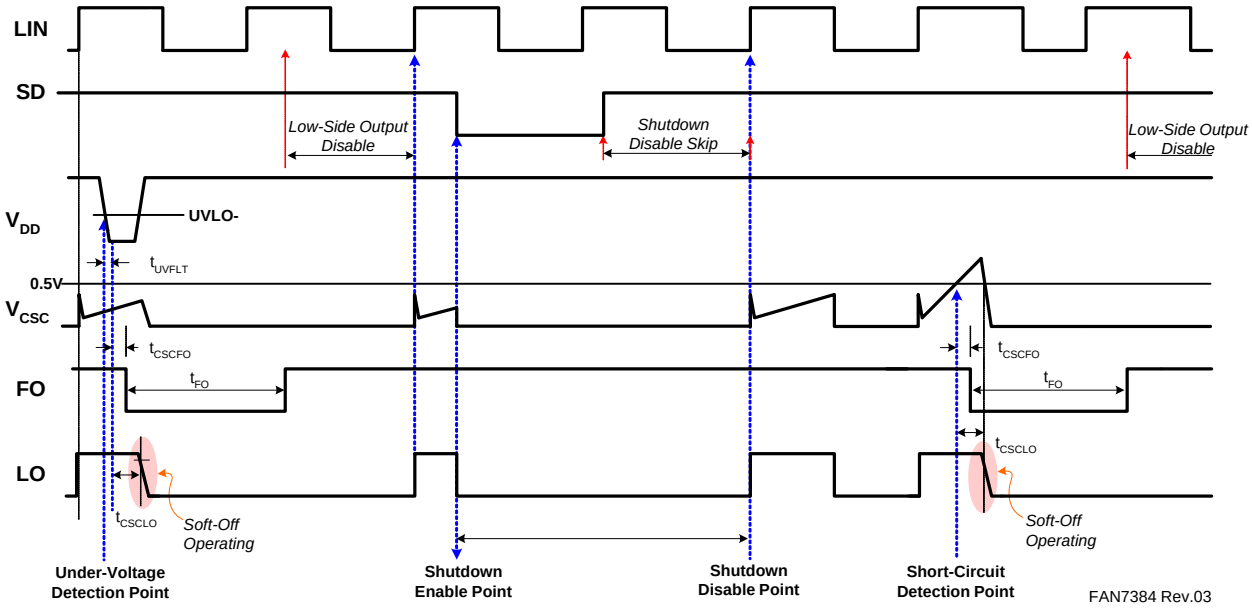


Figure 33. Switching Timing Waveforms Definition

Typical Application Information

1. Protection Function

1.1 Under-Voltage Lockout (UVLO)

The high- and low-side drivers include under-voltage lockout (UVLO) protection circuitry that monitors the supply voltage (V_{DD}) and bootstrap capacitor voltage (V_{BS}) independently. It can be designed to prevent malfunction when V_{DD} and V_{BS} are lower than the specified threshold voltage. Moreover, the UVLO hysteresis prevents chattering during power supply transitions. If the supply voltage (V_{DD}) maintains an under-voltage condition over under-voltage filtering times (typically 16μs), the fault and soft-off circuits are activated, as shown Figure 34.

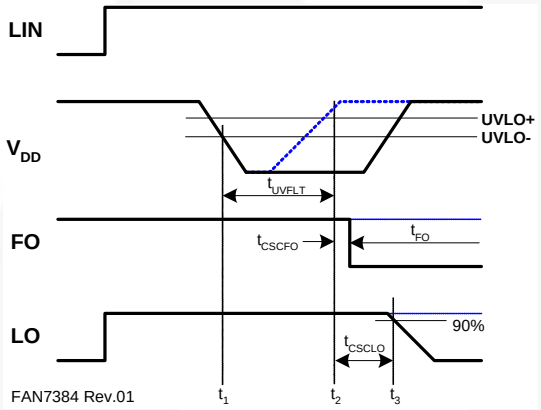


Figure 34. Waveforms for Under-Voltage Lockout

1.2 Shoot-Through Prevention Function

The FAN7384 has a shoot-through prevention circuitry that monitors the high- and low-side inputs. It can be designed to prevent outputs of high- and low-side turning on at same time, as shown Figure 35 and 36.

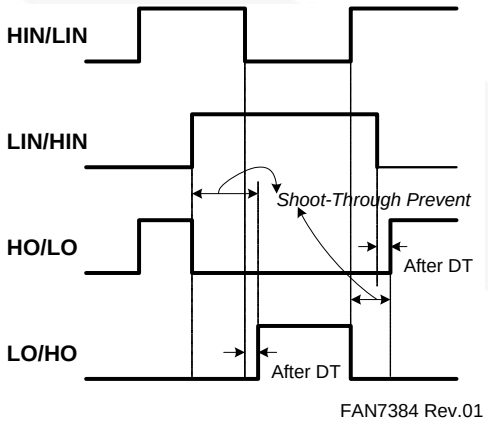


Figure 35. Waveforms for Shoot-Through Prevention

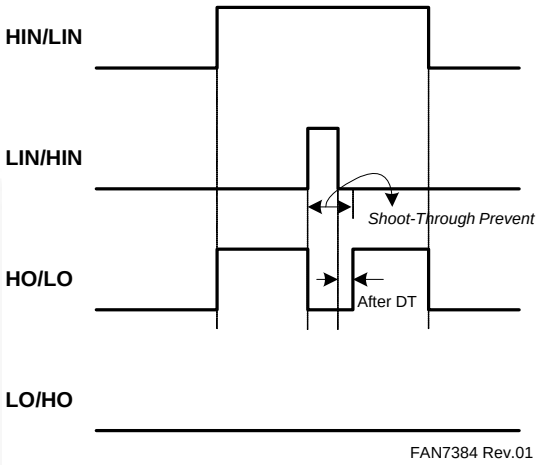


Figure 36. Waveforms for Shoot-Through Prevention

1.3 Over-Current Protection Function

The FAN7384 has over-current detection circuitry that monitors the current-by-current sensing resistor connected from the low-side switch source (V_{SL}) to ground.

It is a built-in time-filler from the over-current event to prevent malfunction from a noise source, such as leading-edge pulse in inductive load application, as shown Figure 37.

The sensing current is calculated as follows:

$$I_{CS} = \frac{V_{CSCREF}}{R_{CS}}[A] \quad (1)$$

where,

V_{CSCREF}: Reference voltage of current sense comparator

R_{CS}: Current sensing resistor

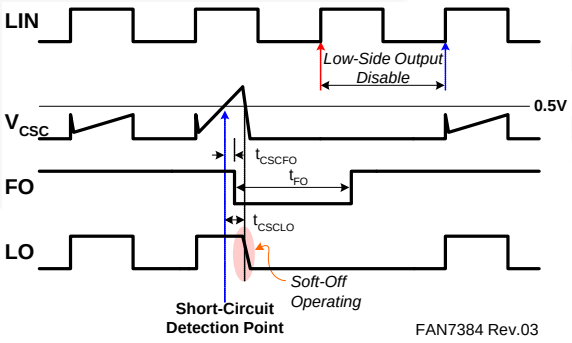


Figure 37. Waveforms for Short-Circuit Protection

2. Layout Considerations

For optimum performance, considerations must be taken during printed circuit board (PCB) layout.

2.1 Supply Capacitors

If the output stages are able to quickly turn on a switching device with a high value of current, the supply capacitors must be placed as close as possible to the device pins (V_{DD} and GND for the ground-tied supply, V_B and V_S for the floating supply) to minimize parasitic inductance and resistance.

2.2 Gate-Drive Loop

Current loops behave like antennae, able to receive and transmit noise. To reduce the noise coupling/emission and improve the power switch turn-on and off performance, gate-drive loops must be reduced as much as possible.

2.3 Ground Plane

To minimize noise coupling, the ground plane should not be placed under or near the high-voltage floating side.

Package Dimensions

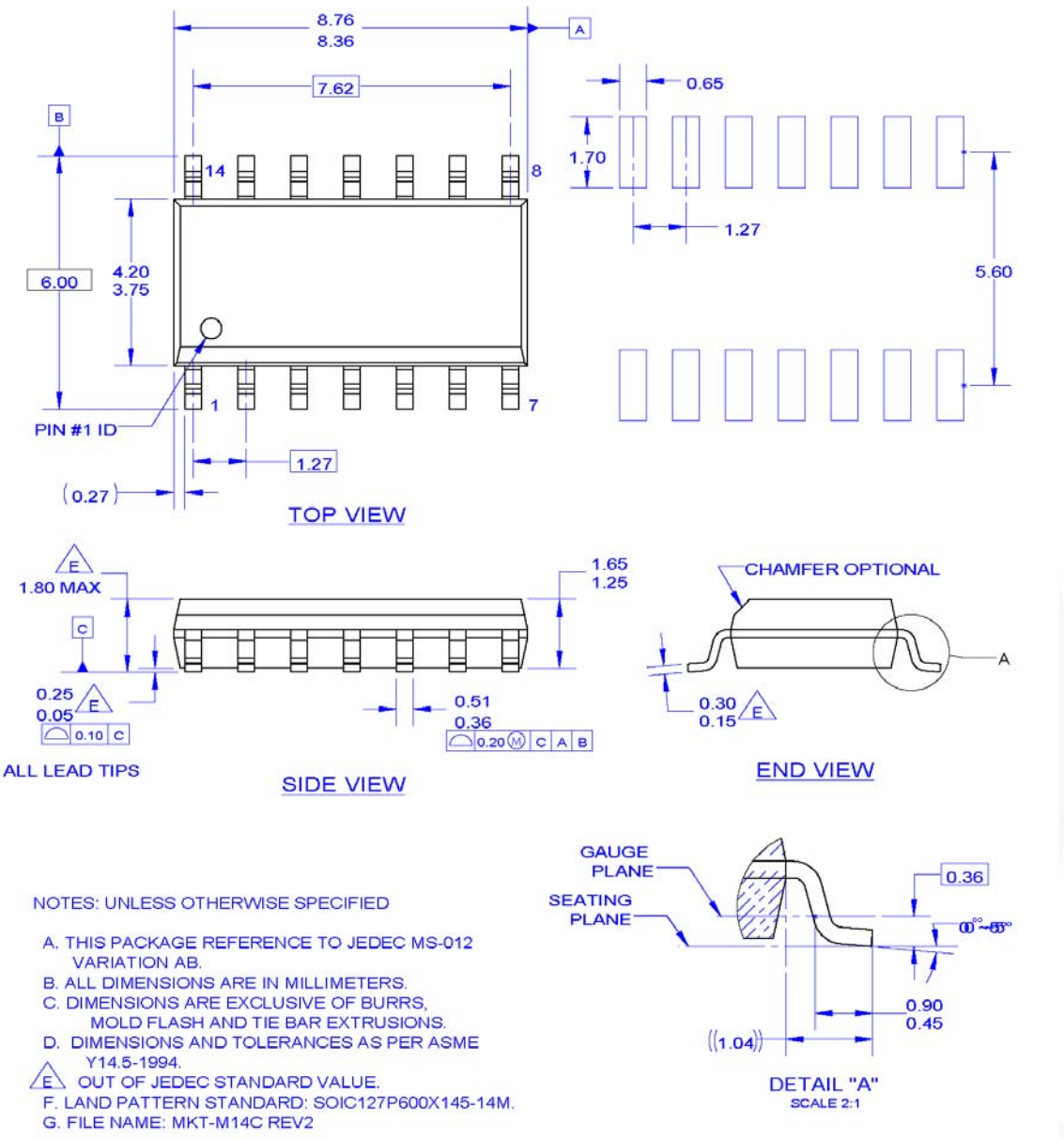


Figure 38. 14-Lead, Small Outline Integrated Circuit (SOIC), Non-JEDEC, .150 Inch Narrow Body, 225SOP

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