Dual Mobile-Friendly PWM/PFM Controller

FAN5234

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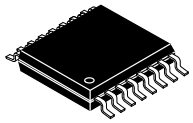
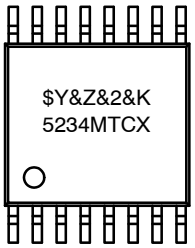


TSSOP16
CASE 948AH

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&Z	= Assembly Plant Code
&2	= Numeric Date Code
&K	= Lot Code
5234MTCX	= Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FAN5234MTCX	TSSOP 16 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

Description

The FAN5234 PWM controller provides high efficiency and regulation with an adjustable output from 0.9 V to 5.5 V required to power I/O, chip−sets, memory banks, or peripherals in high−performance notebook computers, PDAs, and Internet appliances. Synchronous rectification and hysteretic operation at light loads contribute to a high efficiency over a wide range of loads. The Hysteretic Mode of operation can be disabled if PWM Mode is desired for all load levels. Efficiency is further enhanced by using the MOSFET's $R_{DS(ON)}$ as a current−sense component.

Feed−forward ramp modulation, average current mode control, and internal feedback compensation provide fast response to load transients. The FAN5234 monitors these outputs and generates a PGOOD (power−good) signal when the soft−start is completed and the output is within ±10% of its set point. A built−in over−voltage protection prevents the output voltage from going above 120% of the set point. Normal operation is automatically restored when the over−voltage conditions cease. Under−voltage protection latches the chip off when the output drops below 75% of its set value after the soft− start sequence is completed. An adjustable over−current function monitors the output current by sensing the voltage drop across the lower MOSFET.

Features

- Wide Input Voltage Range for Mobile Systems: 2 V to 24 V
- Excellent Dynamic Response with Voltage Feed−Forward and Average−Current−Mode Control
- Lossless Current Sensing on Low−Side MOSFET or Precision Over−Current via Sense Resistor
- V_{CC} Under−Voltage Lockout
- Power−Good Signal
- Light−Load Hysteretic Mode Maximizes Efficiency
- 300 kHz or 600 kHz Operation
- Operating Temperature Range: −10°C to +85°C
- TSSOP16 Package
- This is a Pb−Free Device

Applications

- Mobile PC Regulator
- Handheld PC Power

Related Resources

- Application Note − AN−6002 Component Calculations and Simulation Tools for FAN5234 or FAN5236
- Application Note − AN−1029 Maximum Power Enhancement Techniques for SO−8 Power MOSFET

TYPICAL APPLICATION

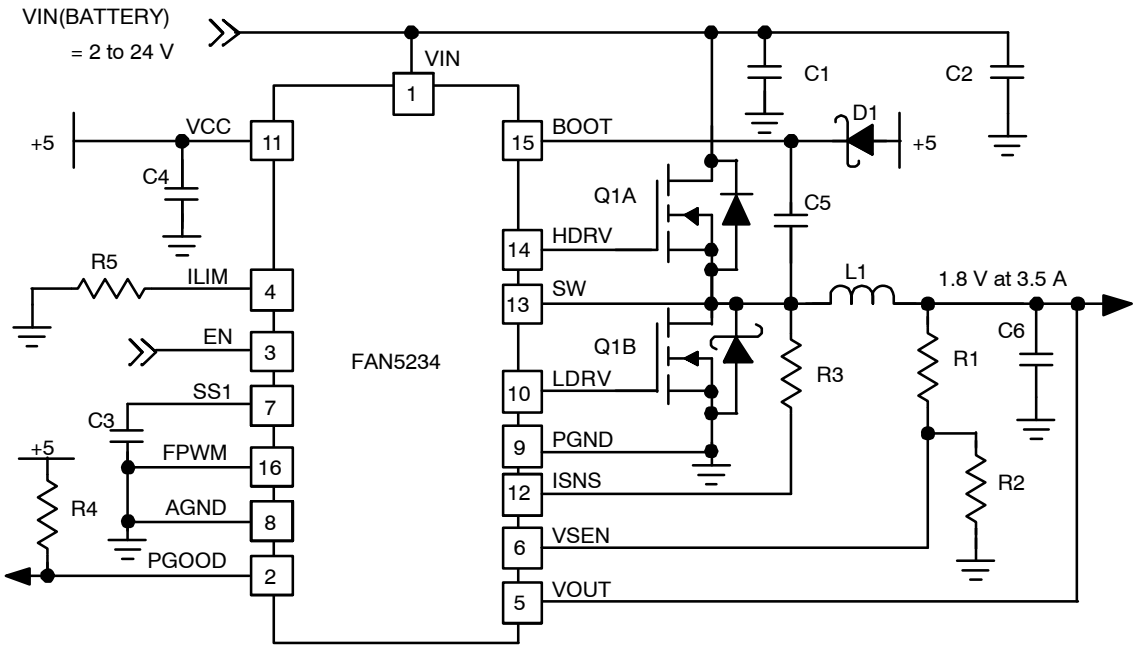


Figure 1. 1.18 V Output Regulator

BLOCK DIAGRAM

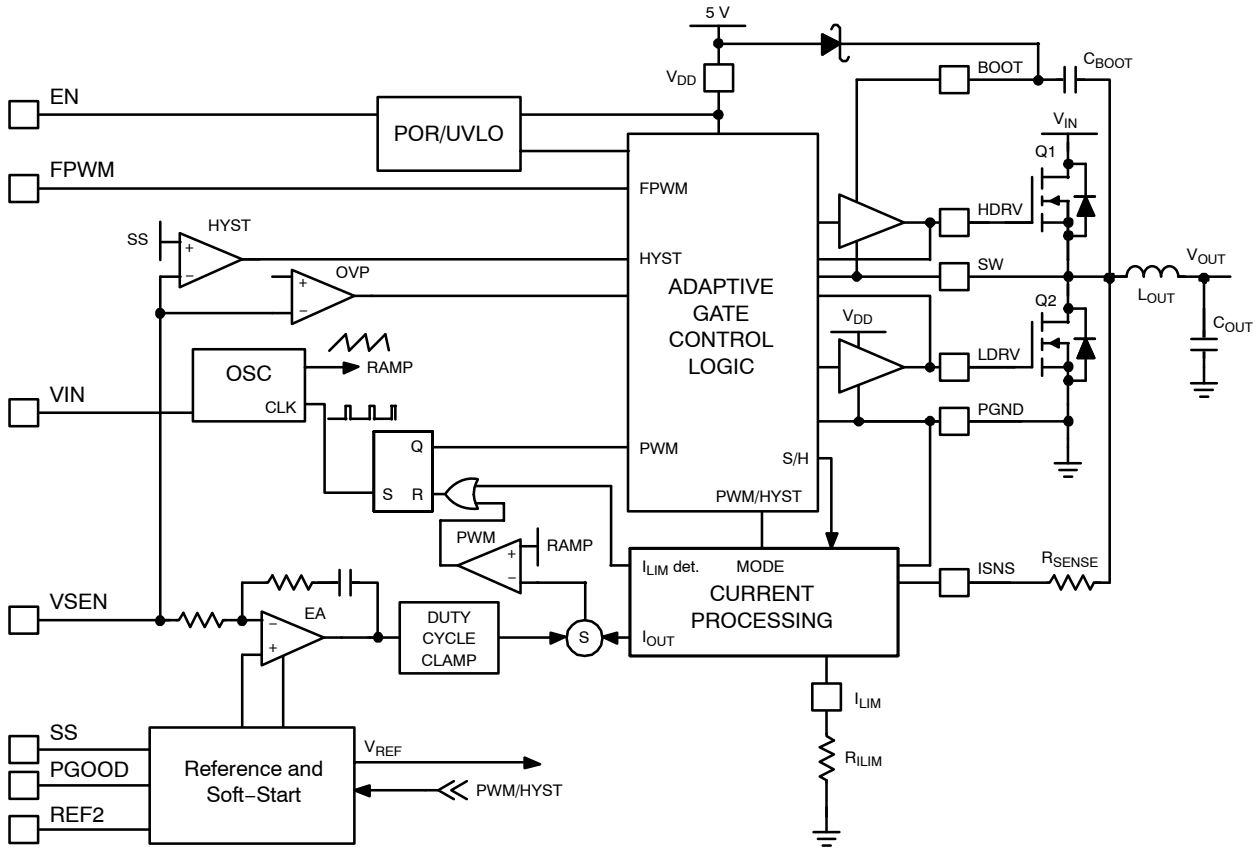


Figure 2. Block Diagram

PIN CONFIGURATION

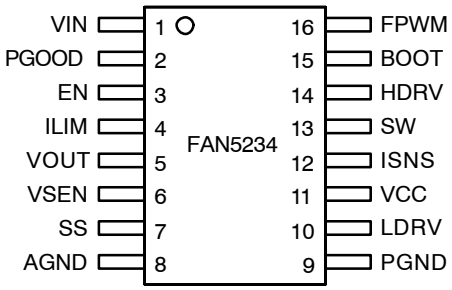


Figure 3. Pin Configuration

PIN DEFINITIONS

Pin #	Name	Description
1	VIN	*Input Voltage.* Connect to main input power source (battery), also used to program operating frequency for low input voltage operation (see Table 1)
2	PGOOD	*Power−Good Flag.* An open−drain output that pulls LOW when V_{SEN} is outside of a ±10% range of the 0.9 V reference
3	EN	*Enable.* Enables operation when pulled to logic HIGH. Toggling EN resets the regulator after a latched fault condition. This is a CMOS input whose state is indeterminate if left open
4	ILIM	*Current Limit.* A resistor from this pin to GND sets the current limit
5	VOUT	*Output Voltage.* Connect to output voltage. Used for regulation to ensure a smooth transition during mode changes. When VOUT is expected to exceed VCC, tie this pin to VCC
6	VSEN	*Output Voltage Sense.* The feedback from the output. Used for regulation as well as power−good, under−voltage, and over−voltage protection monitoring
7	SS	*Soft−Start.* A capacitor from this pin to GND programs the slew rate of the converter during initialization, when this pin is charged with a 5 μA current source
8	AGND	*Analog Ground.* This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin
9	PGND	*Power Ground.* The return for the low−side MOSFET driver output. Connect to the gate of the low−side MOSFET
10	LDRV	*Low−Side Drive.* The low−side (lower) MOSFET driver output. Connect to the gate of the low−side MOSFET
11	VCC	*Supply Voltage.* This pin powers the chip as well as the LDRV buffers. The IC starts to operate when voltage on this pin exceeds 4.6 V (UVLO rising) and shuts down when it drops below 4.3 V (UVLO falling)
12	ISNS	*Current−Sense Input.* Monitors the voltage drop across the lower MOSFET or external sense resistor for current feedback
13	SW	*Switching Node.* Return for the high−side MOSFET driver and a current−sense input. Connect to source of high−side MOSFET and low−side MOSFET drain
14	HDRV	*High−Side Drive.* High−side (upper) MOSFET driver output. Connect to the gate of the high−side MOSFET
15	BOOT	*BOOT.* Positive supply for the upper MOSFET driver. Connect as shown in Figure 2
16	FPWM	*Forced PWM Mode.* When logic HIGH, inhibits the regulation from entering Hysteretic Mode

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	V_{CC} Supply Voltage	–	6.5	V
V_{IN}	V_{IN} Supply Voltage	–	27	V
	BOOT, SW, ISNS, HDRV Pins	–	33	V
	BOOT to SW Pins	–	6.5	V
	All Other Pins	−0.3	V_{CC} + 0.3	V
T_J	Junction Temperature	−10	+150	°C
T_{STG}	Storage Temperature	−65	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds	–	+300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	V_{CC} Supply Voltage	4.75	5.00	5.25	V
V_{IN}	V_{IN} Supply Voltage	–	–	24	V
T_A	Ambient Temperature	−10	–	+85	°C
θ_{JA}	Thermal Resistance, Junction to Ambient	–	–	112	°C/W

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL SPECIFICATIONS Recommended operating conditions, unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLIES						
I_{VCC}	V_{CC} Current	LDRV, HDRV Open; V_{SEN} Forced Above Regulation Point	–	850	1300	μA
		Shutdown (EN−0)	–	5	15	μA
I_{SINK}	V_{IN} Current, Sinking	VIN Pin = Input Voltage Source	10	20	30	μA
I_{SOURCE}	V_{IN} Current, Sourcing	VIN Pin = GND	7	15	20	μA
I_{SD}	V_{IN} Current, Shutdown		–	–	1	μA
V_{UVLO}	UVLO Threshold	Rising V_{CC}	4.30	4.55	4.75	V
		Falling	4.10	4.27	4.50	
V_{UVLOH}	UVLO Hysteresis		0.1	–	0.5	V
OSCILLATOR						
f_{osc}	Frequency	V_{IN} > 5 V	255	300	345	kHz
		V_{IN} = 0 V	510	600	690	
V_{PP}	Ramp Amplitude	V_{IN} = 16 V	–	2	–	V
		V_{IN} > 5 V	–	1.25	–	
V_{RAMP}	Ramp Offset		–	0.5	–	V
G	Ramp / V_{IN} Gain	$V_{IN} \geq 3$ V	–	125	–	mV/V
		1 V < V_{IN} < 3 V	–	250	–	
REFERENCE AND SOFT−START						
V_{REF}	Internal Reference Voltage		0.891	0.900	0.909	V
I_{SS}	Soft−Start Current	At Startup	–	5	–	μA
V_{SS}	Soft−Start Complete Threshold		–	1.5	–	V

ELECTRICAL SPECIFICATIONS Recommended operating conditions, unless otherwise noted. (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PWM CONVERTER						
	Load Regulation	I_{OUT} from 0 to 3 A, V_{IN} from 2 to 24 V	–1	–	+1	%
I_{SEN}	V_{SEN} Bias Current		50	80	150	nA
	VOUT Pin Input Impedance		40	55	65	kΩ
$UVLO_{TSD}$	Under–Voltage Shutdown	% of Set Point, 2 μs Noise Filter	70	75	80	%
I_{SNS}	Over–Current Threshold	R_{ILIM} = 68.5 kΩ, Figure 6	115	144	172	%
UVLO	Over–Voltage Threshold	% of Set Point, 2 μs Noise Filter	113	–	120	μA
OUTPUT DRIVERS						
	HDRV Output Resistance	Sourcing	–	8.0	15.0	Ω
		Sinking	–	3.2	4.0	
	LDRV Output Resistance	Sourcing	–	8.0	15.0	Ω
		Sinking	–	1.5	2.4	
POWER–GOOD OUTPUT AND CONTROL PINS						
	Lower Threshold	% of Set Point, 2 μs Noise Filter	86	–	92	%
	Upper Threshold	% of Set Point, 2 μs Noise Filter	110	–	115	%
	PGOOD Output Low	I_{PGOOD} = 4 mA	–	–	0.5	V
	Leakage Current	V_{PULLUP} = 5 V	–	–	1	μA
	Soft–Start Voltage, PGOOD Enabled		–	1.5	–	% V_{REF2}
EN, FPWM INPUTS						
V_{INH}	Input High		2	–	–	V
V_{INL}	Input Low		–	–	0.8	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

FUNCTIONAL DESCRIPTION

Overview

The FAN5234 is a PWM controller intended for low–voltage power applications in notebook, desktop, and sub–notebook PCs. The output voltage of the controller can be set in the range of 0.9 V to 5.5 V by an external resistor divider.

The synchronous buck converter can operate from an unregulated DC source (such as a notebook battery), with voltage ranging from 2 V to 24 V, or from a regulated system rail. In either case, the IC is biased from a +5 V source. The PWM modulator uses an average–current–mode control with input voltage feed–forward for simplified feedback loop compensation and improved line regulation. The controller includes integrated feedback loop compensation that dramatically reduces the number of external components.

Depending on the load level, the converter can operate in fixed–frequency PWM Mode or in Hysteretic Mode. Switch–over from PWM to Hysteretic Mode improves the converters' efficiency at light loads and prolongs battery run time. In Hysteretic Mode, a comparator is synchronized to the main clock to allow seamless transition between the operational modes and reduced channel–to–channel interaction.

The Hysteretic Mode of operation can be inhibited independently using the FPWM pin if variable frequency operation is not desired.

Oscillator

Table 1. CONVERTER OPERATING MODES

Mode	f_{SW}	Converter Power	VIN Pin
Battery	300	2 to 24 V	Battery (> 5 V)
Fixed 300	300	< 5.5 V Fixed	100 kΩ to GND
Fixed 600	600	< 5.5 V Fixed	GND

When V_{IN} is from the battery, the oscillator ramp amplitude is proportional to V_{IN}, providing voltage feed–forward control for improved loop response. When in

either of the fixed modes, oscillator ramp amplitude is fixed. The operation frequency is determined according to the connection on the VIN pin (see Table 1)

Initialization and Soft Start

Assuming EN is HIGH, FAN5234 is initialized when V_{CC} exceeds the rising UVLO threshold. Should V_{CC} drop below the UVLO threshold, an internal power−on reset function disables the chip.

The voltage at the positive input of the error amplifier is limited by the voltage at the SS pin, which is charged with 5 mA current source. Once CSS has charged to V_{REF} (0.9 V), the output voltage is in regulation. The time it takes SS to reach 0.9 V is:

$$t_{0.9} = \frac{0.9 \times C_{SS}}{5} \qquad \text{(eq. 1)}$$

where $t_{0.9}$ is in seconds if C_{SS} is in μF.

When SS reaches 1.5 V, the power−good outputs are enabled and Hysteretic Mode is allowed. The converter is forced into PWM Mode during soft−start.

Operation Mode Control

The mode−control circuit changes the converter's mode from PWM to Hysteretic and vice versa based on the voltage polarity of the SW node when the lower MOSFET is conducting and just before the upper MOSFET turns on. For continuous inductor current, the SW node is negative when the lower MOSFET is conducting and the converters operate in fixed−frequency PWM Mode, as shown in Figure 4. This mode achieves high efficiency at nominal load. When the load current decreases to the point where the inductor current flows through the lower MOSFET in the "reverse" direction, the SW node becomes positive and the mode is changed to Hysteretic, which achieves higher efficiency at low currents by decreasing the effective switching frequency.

To prevent accidental mode change or "mode chatter," the transition from PWM to Hysteretic Mode occurs when the SW node is positive for eight consecutive clock cycles (see Figure 4). The polarity of the SW node is sampled at the end of the lower MOSFET conduction time. At the transition between PWM and Hysteretic Mode, both the upper and lower MOSFETs are turned off. The SW node "rings" based on the output inductor and the parasitic capacitance on the SW node and settles out at the value of the output voltage.

The boundary value of inductor current, where current becomes discontinuous, is estimated by the following:

$$I_{LOAD(DIS)} = \left(\frac{(V_{IN} - V_{OUT})V_{OUT}}{2f_{SW}L_{OUT}V_{IN}}\right) \qquad \text{(eq. 2)}$$

Hysteretic Mode

Conversely, the transition from Hysteretic Mode to PWM Mode occurs when the SW node is negative for eight consecutive cycles.

A sudden increase in the output current causes a change from Hysteretic to PWM Mode. This load increase causes an instantaneous decrease in the output voltage due to the voltage drop on the output capacitor ESR. If the load causes the output voltage (as presented at V_{SEN}) to drop below the hysteretic regulation level (20 mV below V_{REF}), the mode is changed to PWM on the next clock cycle.

In Hysteretic Mode, the PWM comparator and the error amplifier that provide control in PWM Mode are inhibited and the hysteretic comparator is activated. In Hysteretic Mode the low−side MOSFET is operated as a synchronous rectifier, where the voltage across ($V_{DS(ON)}$) is monitored and it is switched off when $V_{DS(ON)}$ goes positive (current flowing back from the load), allowing the diode to block reverse conduction.

The hysteretic comparator causes HDRV turn−on when the output voltage (at V_{SEN}) falls below the lower threshold (10 mV below V_{REF}) and terminates the PFM signal when V_{SEN} rises over the higher threshold (5 mV above V_{REF}).

The switching frequency is primarily a function of:

- Spread between the two hysteretic thresholds
- I_{LOAD}
- Output inductor and capacitor ESR

A transition back to PWM Continuous Conduction Mode or (CCM) occurs when the inductor current rises sufficiently to stay positive for eight consecutive cycles. This occurs when:

$$I_{LOAD(CCM)} = \left(\frac{\Delta V_{HYSTERESIS}}{2\ ESR}\right) \qquad \text{(eq. 3)}$$

where $\Delta V_{HYSTERESIS}$ = 15 mV and ESR is the equivalent series resistance of C_{OUT}.

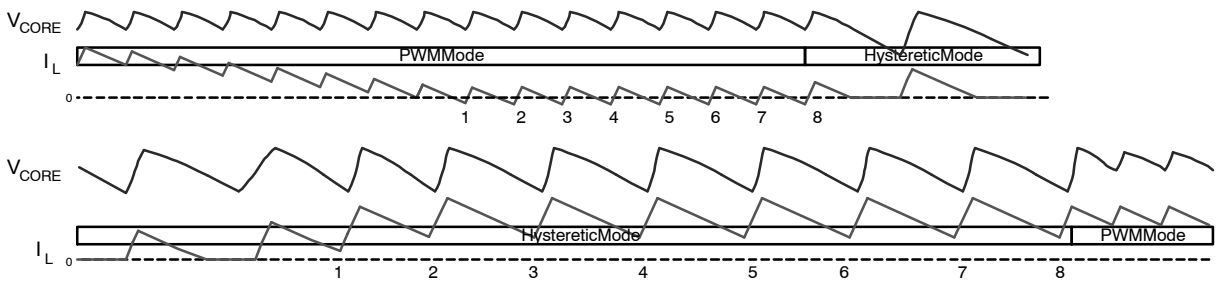


Figure 4. Transitioning between PWM and Hysteretic Mode

Due to different control mechanisms, the value of the load current where transition into PWM operation takes place is typically higher compared to the load level at which transition into Hysteretic Mode occurs. Hysteretic Mode can be disabled by setting the FPWM pin HIGH.

Current Processing

The following discussion refers to Figure 6.

The current through R_{SENSE} resistor (I_{SNS}) is sampled shortly after Q2 is turned on. That current is held and summed with the output of the error amplifier. This effectively creates a current−mode control loop. The resistor connected to the ISNS pin (R_{SENSE}) sets the gain in the current feedback loop. Equation 4 estimates the recommended value of R_{SENSE} as a function of the maximum load current ($I_{LOAD(MAX)}$) and the value of the MOSFET $R_{DS(ON)}$. R_{SENSE} must be kept higher than 700 Ω even if the number calculated comes out less than 700 Ω:

$$R_{SENSE} = \left(\frac{I_{LOAD(MAX)} \times R_{DS(ON)}}{150\ \mu A} - 100 \right) \quad \text{(eq. 4)}$$

Setting the Current Limit

A ratio of I_{SNS} is also compared to the current established when a 0.9 V internal reference drives the ILIM pin:

$$R_{LIM} = \frac{11}{I_{LOAD}} \times \left(\frac{(100 + R_{SENSE})}{R_{DS(ON)}} \right) \quad \text{(eq. 5)}$$

Since the tolerance on the current limit is largely dependent on the ratio of the external resistors, it is fairly accurate if the voltage drop on the switching node side of R_{SENSE} is an accurate representation of the load current. When using the MOSFET as the sensing element, the variation of $R_{DS(ON)}$ causes proportional variation in I_{SNS}. This value varies from device to device and has a typical junction temperature coefficient of about 0.4%/°C *(consult the MOSFET data sheet for* actual values), the actual current limit set point decreases proportional to increasing MOSFET die temperature. A factor of 1.6 in the current limit set point should compensate for all MOSFET $R_{DS(ON)}$ variations, assuming the MOSFET's heat sinking keep its operating die temperature below 125°C.

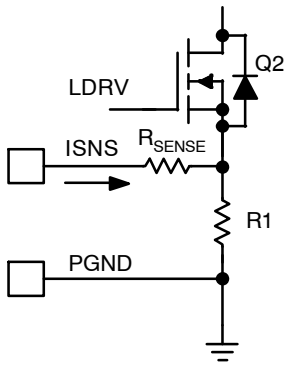


Figure 5. Improving Current−Sensing Accuracy

More accurate sensing can be achieved by using a resistor (R1) instead of the $R_{DS(ON)}$ of the FET, as shown in Figure 5. This approach causes higher losses, but yields greater accuracy in both V_{DROOP} and I_{LIMIT}. R1 is a low value (e.g. 10 mΩ) resistor.

Current limit (I_{LIMIT}) should be set high enough to allow inductor current to rise in response to an output load transient. Typically, a factor of 1.2 is sufficient. Since I_{LIMIT} is a peak current cut−off value, multiply $I_{LOAD(MAX)}$ by the inductor ripple current (use 25%). For example, in Figure 1 the target for I_{LIMIT} would be:

$$I_{LIMIT} > 1.2 \times 1.25 \times 1.6 \times 3.5\ A \approx 8.5\ A \quad \text{(eq. 6)}$$

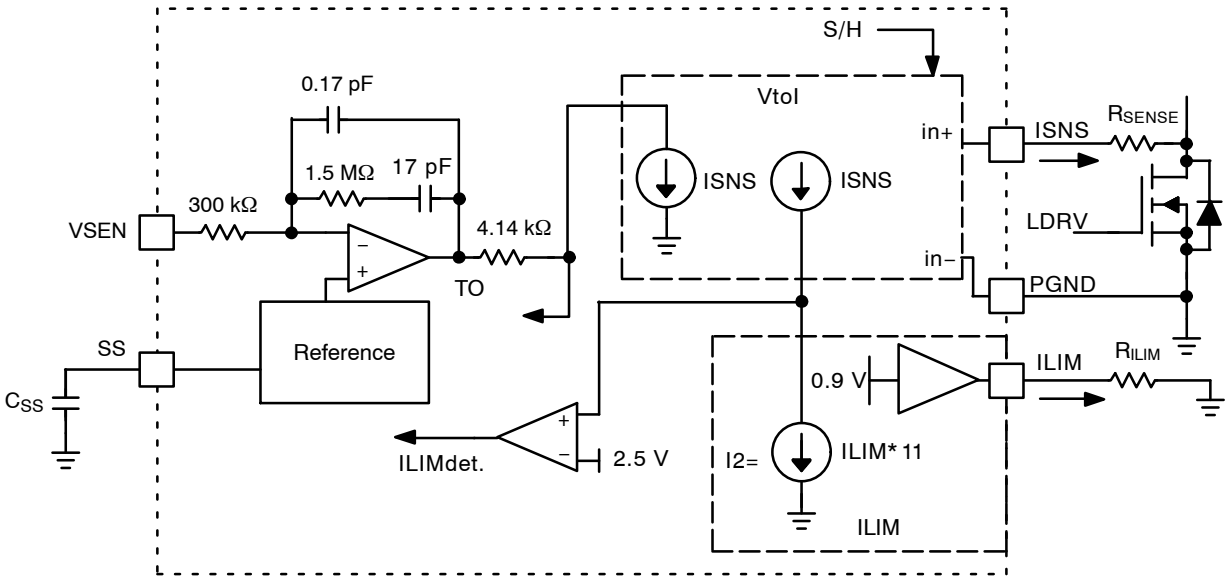


Figure 6. Current Limit / Summing Circuits

Duty Cycle Clamp

During severe load increase, the error amplifier output can go to its upper limit, pushing a duty cycle to almost 100% for a significant amount of time. This could cause a large increase of the inductor current and lead to a long recovery from a transient over−current condition or even to a failure at high input voltages. To prevent this, the output of the error amplifier is clamped to a fixed value after two clock cycles if severe output voltage excursion is detected, limiting maximum duty cycle to:

$$DC_{MAX} = \frac{V_{OUT}}{V_{IN}} + \left(\frac{2.4}{V_{IN}}\right) \quad \text{(eq. 7)}$$

This is designed to not interfere with normal PWM operation. When FPWM is grounded, the duty cycle clamp is disabled and the maximum duty cycle is 87%.

Gate Driver

The adaptive gate control logic translates the internal PWM control signal into the MOSFET gate drive signals, providing necessary amplification, level shifting, and shoot−through protection. It also has functions that help optimize the IC performance over a wide range of operating conditions. Since MOSFET switching time can vary dramatically from type to type and with the input voltage, the gate control logic provides adaptive dead time by monitoring the gate−to−source voltages of both upper and lower MOSFETs. The lower MOSFET drive is not turned on until the gate−to−source voltage of the upper MOSFET has decreased to less than approximately 1 V. Similarly, the upper MOSFET is not turned on until the gate−to−source voltage of the lower MOSFET has decreased to less than approximately 1 V. This allows a wide variety of upper and lower MOSFETs to be used without concern for simultaneous conduction or shoot−through.

There must be a low−resistance, low−inductance path between the driver pin and the MOSFET gate for the adaptive dead−time circuit to work properly. Any delay along that path subtracts from the delay generated by the adaptive dead−time circuit and shoot−through may occur.

Frequency Loop Compensation

Due to the implemented current−mode control, the modulator has a single−pole response with −1 slope at frequency determined by load. Therefore:

$$f_{PO} = \frac{1}{2\pi R_O C_O} \quad \text{(eq. 8)}$$

where R_O is load resistance and C_O is load capacitance.

For this type of modulator, type−2 compensation circuit is usually sufficient. To reduce the number of external components and simplify the design task, the PWM controller has an internally compensated error amplifier. Figure 7 shows a type two amplifier, its response, and the responses of a current mode modulator and the converter. The type−2 amplifier, in addition to the pole at the origin, has a zero−pole pair that causes a flat gain region at frequencies between the zero and the pole.

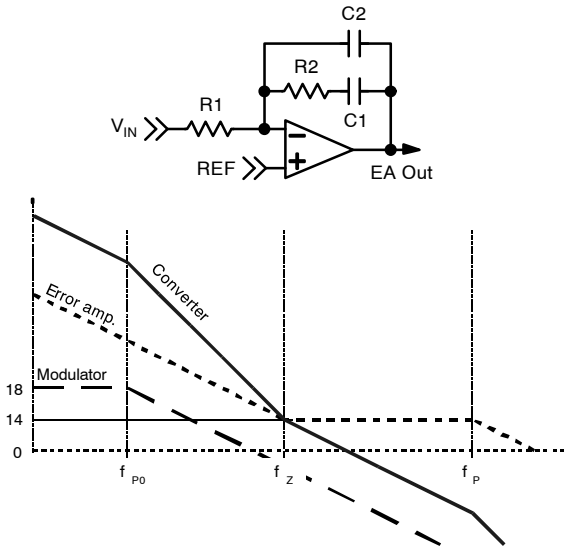


Figure 7. Compensation

$$f_z = \frac{1}{2\pi R_2 C_1} = 6\ \text{kHz} \quad \text{(eq. 9)}$$

$$f_P = \frac{1}{2\pi R_2 C_2} = 600\ \text{kHz} \quad \text{(eq. 10)}$$

This region is also associated with phase “bump” or reduced phase shift. The amount of phase shift reduction depends the width of the region of flat gain and has a maximum value of 90°. To further simplify the converter compensation, the modulator gain is kept independent of the input voltage variation by providing feed−forward of V_{IN} to the oscillator ramp.

The zero frequency, the amplifier high−frequency gain, and the modulator gain are chosen to satisfy most typical applications. The crossover frequency appears at the point where the modulator attenuation equals the amplifier high−frequency gain. The system designer must specify the output filter capacitors to position the load main pole somewhere within one decade lower than the amplifier zero frequency. With this type of compensation, plenty of phase margin is achieved due to zero−pole pair phase “boost.”

Conditional stability may occur only when the main load pole is positioned too much to the left side on the frequency axis due to excessive output filter capacitance. In this case, the ESR zero placed within the 10 kHz to 50 kHz range gives some additional phase boost. There is an opposite trend in mobile applications to keep the output capacitor as small as possible.

Protections

The converter output is monitored and protected against extreme overload, short circuit, over−voltage, and under−voltage conditions.

A sustained overload on an output sets the PGOOD pin LOW and latches off the chip. Operation is restored by cycling the V_{CC} voltage or by toggling the EN pin.

If V_{OUT} drops below the under−voltage threshold, the chip shuts down immediately.

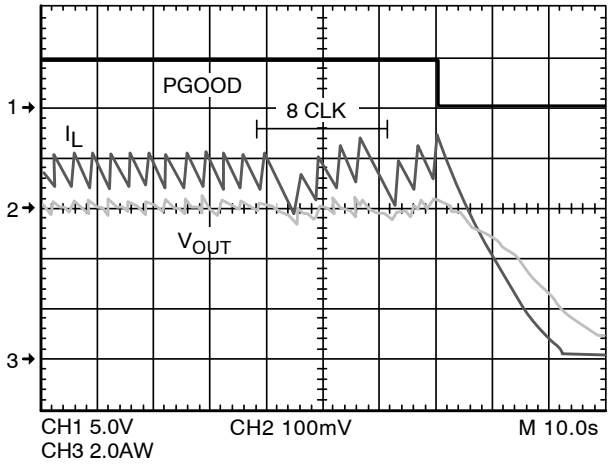


Figure 8. Over−Current Protection Waveforms

Over−Current Sensing

If the circuit's current−limit signal ("I_{LIM} det" in Figure 6) is HIGH at the beginning of a clock cycle, a pulseskipping circuit is activated and HDRV is inhibited. The circuit continues to pulse skip in this manner for the next eight clock cycles. If at any time from the ninth to the sixteenth clock cycle, the I_{LIM} det is again reached, the over−current protection latch is set, disabling the chip. If I_{LIM} det does not occur between cycles 9 and 16, normal operation is restored and the over−current circuit resets itself.

Over−Voltage / Under−Voltage Protection

Should the V_{SEN} voltage exceed 120% of V_{REF} (0.9 V) due to an upper MOSFET failure or for other reasons, the over−voltage protection comparator forces LDRV HIGH. This action actively pulls down the output voltage and, in the event of the upper MOSFET failure, eventually blows the battery fuse. As soon as the output voltage drops below the threshold, the OVP comparator is disengaged.

This OVP scheme provides a 'soft' crowbar function to tackle severe load transients and does not invert the output voltage when activated − a common problem for latched OVP schemes.

Similarly, if an output short−circuit or severe load transient causes the output to droop to less than 75% of its regulation set point, the regulator shuts down.

Over−Temperature Protection

The chip incorporates an over−temperature protection circuit that shuts the chip down when a die temperature reaches 150°C. Normal operation is restored at die temperature below 125°C with internal power on reset asserted, resulting in a full soft−start cycle.

DESIGN AND COMPONENT SELECTION

Guidelines

As an initial step, define operating input voltage range, output voltage, and minimum and maximum load currents for the controller.

For the examples in the following discussion, select components for:

V_{IN} from 5 V to 20 V

V_{OUT} = 1.8 V at $I_{LOAD(MAX)}$ = 3.5 A

Setting the Output Voltage

The internal reference is 0.9 V. The output is divided down by a voltage divider to the VSEN pin (for example, R1 and R2 in Figure 1). The output voltage therefore is:

$$\frac{0.9\ V}{R2} = \frac{V_{OUT} - 0.9\ V}{R1} \qquad \text{(eq. 11)}$$

To minimize noise pickup on this node, keep the resistor to GND (R2) below 2 K; for example R2 at 1.82 K, then choose R5:

$$R5 = \frac{(1.8\ k\Omega) \times (1.8\ V - 0.9)}{0.9} = 1.82\ K \qquad \text{(eq. 12)}$$

Output Inductor Selection

The minimum practical output inductor value keeps inductor current just on the boundary of continuous conduction at some minimum load. The industry standard practice is to choose the ripple current to be somewhere from 15% to 35% of the nominal current. At light−load, the ripple current determines the point where the converter automatically switches to Hysteretic Mode to sustain high efficiency. The following equations help to choose the proper value of the output filter inductor:

$$\Delta I = 2 - 1_{MIN} - \frac{\Delta V_{OUT}}{ESR} \qquad \text{(eq. 13)}$$

where ΔI is the inductor ripple current, which is chosen for 20% of the full load current and ΔV_{OUT} is the maximum output ripple voltage allowed:

$$L = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I} \times \frac{V_{OUT}}{V_{IN}} \qquad \text{(eq. 14)}$$

For this example, use:

$$V_{IN} = 20\ V, V_{OUT} = 1.8\ V \quad \text{(eq. 15)}$$
$$\Delta I = 20\% \times 3.5\ A = 0.7\ A$$
$$f_{SW} = 300\ kHz$$

Therefore:

$$L \approx 8\ \mu H \quad \text{(eq. 16)}$$

Output Capacitor Selection

The output capacitor serves two major functions in a switching power supply. Along with the inductor, it filters the sequence of pulses produced by the switcher and it supplies the load transient currents. The output capacitor requirements are usually dictated by ESR, inductor ripple current (ΔI), and the allowable ripple voltage (ΔV):

$$ESR < \frac{\Delta V}{\Delta I} \quad \text{(eq. 17)}$$

For this example,

$$ESR_{(MAX)} = \frac{\Delta V}{\Delta I} = \frac{0.1\ V}{0.7\ A} = 142\ m\Omega$$

In addition, the capacitor's ESR must be low enough to allow the converter to stay in regulation during a load step. The ripple voltage due to ESR for the converter in Figure 1 is 100 m V_{PP}. Some additional ripple will appear due to the capacitance value itself:

$$\Delta V = \frac{\Delta I}{C_{OUT} \times 8 \times f_{SW}} \quad \text{(eq. 18)}$$

which is only about 1.5 mV for the converter in Figure 1 and can be ignored.

The capacitor must also be rated to withstand the RMS current, which is approximately $0.3 \times (\Delta I)$ or about 210 mA for the converter in Figure 1. High−frequency decoupling capacitors should be placed as close to the loads as physically possible.

Input Capacitor Selection

The input capacitor should be selected by its ripple current rating. The input RMS current at maximum load current (I_L) is:

$$I_{RMS} = I_L \sqrt{D - D^2} \quad \text{(eq. 19)}$$

where the converter duty cycle;

$$D = \frac{V_{OUT}}{V_{IN}}$$

the circuit in Figure 1, with $V_{IN} = 6$, calculates to $I_{RMS} = 1.6$ A.

Power MOSFET Selection

Losses in a MOSFET are the sum of its switching (P_{SW}) and conduction (P_{COND}) losses.

In typical applications, the FAN5234 converter's output voltage is low with respect to its input voltage. Therefore, the lower MOSFET (Q2) is conducting the full−load current for most of the cycle. Q2 should therefore be selected to minimize conduction losses, thereby selecting a MOSFET with low $R_{DS(ON)}$.

In contrast, the high−side MOSFET (Q1) has a shorter duty cycle, and its conduction loss has less impact. Q1, however, sees most of the switching losses, so Q1's primary selection criteria should be gate charge.

High−Side Losses

Figure 9 shows a MOSFET's switching interval, with the upper graph being the voltage and current on the drainto source and the lower graph detailing V_{GS} vs. Time with a constant current charging the gate. The x−axis therefore is also representative of gate charge (Q_G). $C_{ISS} = C_{GD} + C_{GS}$, and it controls t1, t2, and t4 timing. C_{GD} receives the current from the gate driver during t3 (as V_{DS} is falling). The gate charge (Q_G) parameters on the lower graph are either specified or can be derived from MOSFET datasheets.

Assuming switching losses are about the same for both the rising edge and falling edge, Q1's switching losses, occur during the shaded time when the MOSFET has voltage across it and current through it.

These losses are given by:

$$P_{UPPER} = P_{SW} + P_{COND} \quad \text{(eq. 20)}$$

where:

$$P_{SW} = \left(\frac{V_{DS} \times I_L}{2} \times 2 \times t_s\right) f_{SW} \quad \text{(eq. 21)}$$

$$P_{COND} = \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT}{}^2 \times R_{DS(ON)} \quad \text{(eq. 22)}$$

P_{UPPER} is the upper MOSFET's total losses and P_{SW} and P_{COND} are the switching and conduction losses for a given MOSFET. $R_{DS(ON)}$ is at the maximum junction temperature (T_J). t_S is the switching period (rise or fall time) and is t2 + t3 in Figure 9.

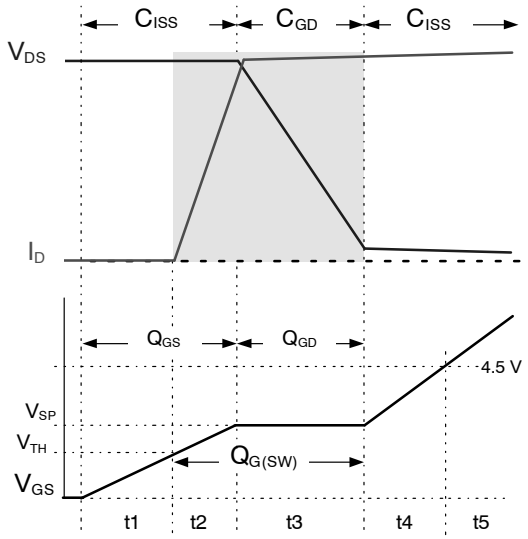


Figure 9. Switching Losses and Q_G ($C_{ISS} = C_{GS} \parallel C_{GD}$)

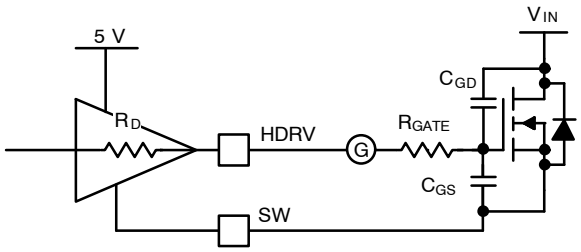


Figure 10. Drive Equivalent Circuit

The driver's impedance and C_{ISS} determine t2 while t3's period is controlled by the driver's impedance and Q_{GD}. Since most of ts occurs when $V_{GS} = V_{SP}$, use a constant current assumption for the driver to simplify the calculation of ts:

$$t_s = \frac{Q_{G(SW)}}{I_{DRIVER}} = \frac{Q_{S(SW)}}{\left(\frac{V_{CC} - V_{SP}}{R_{DRIVER} + R_{GATE}}\right)} \qquad \text{(eq. 23)}$$

Most MOSFET vendors specify Q_{GD} and Q_{GS}. $Q_{G(SW)}$ can be determined as:

$$Q_{G(SW)} = Q_{GD} + Q_{GS} - Q_{TH} \qquad \text{(eq. 24)}$$

where Q_{TH} is the gate charge required to get the MOSFET to its threshold (V_{TH}).

For the high−side MOSFET, $V_{DS} = V_{IN}$, which can be as high as 20 V in a typical portable application. Care should be taken to include the delivery of the MOSFET's gate power (P_{GATE}) in calculating the power dissipation required for the FAN5234:

$$P_{GATE} = Q_G \times V_{CC} \times f_{SW} \qquad \text{(eq. 25)}$$

where Q_G is the total gate charge to reach V_{CC}.

Low−Side Losses

Q2 switches on or off with its parallel Schottky diode conducting; therefore, $V_{DS} \approx 0.5$ V. Since P_{SW} is proportional to V_{DS}, Q2's switching losses are negligible and Q2 is selected based on $R_{DS(ON)}$ only.

Conduction losses for Q2 are given by:

$$P_{COND} = (1 - D) \times I_{OUT}^{\ 2} \times R_{DS(ON)} \qquad \text{(eq. 26)}$$

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the highest operating junction temperature and $D = V_{OUT} / V_{IN}$ is the minimum duty cycle for the converter.

Since $D_{MIN} < 20\%$ for portable computers, $(1-D) \approx 1$ produces a conservative result, simplifying the calculation.

The maximum power dissipation ($P_{D(MAX)}$) is a function of the maximum allowable die temperature of the lowside MOSFET, the Θ_{JA}, and the maximum allowable ambient temperature rise:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\Theta_{JA}} \qquad \text{(eq. 27)}$$

θ_{JA} depends primarily on the amount of PCB area that can be devoted to heat sinking (see AN−1029 − Maximum Power Enhancement Techniques for SO−8 Power MOSFET for MOSFET thermal information).

Table 2. BUILD OF MATERIALS FOR 1.8 V, 3.5 A REGULATOR

Description	Qty.	Ref.	Vendor	Part Number
Capacitor 68 μF, Tantalum, 25 V, ESR 95 mΩ	1	C1	AVX.	TPSV686*025#095
Capacitor 10 nF, Ceramic	2	C2, C3	Any	
Capacitor 68 μF, Tantalum, 6 V, ESR 1.8 Ω	1	C4	AVX.	TAJV686*006
Capacitor 0.1 μF, Ceramic	2	C5	Any	
Capacitor 330 μF, Tantalum, 6 V, ESR 100 mΩ	2	C6	AVX.	TPSE337*006#0100
1.82 kΩ, 1% Resistor	2	R1, R2	Any	
1.3 kΩ, 1% Resistor	1	R3	Any	
100 kΩ, 5% Resistor	1	R4	Any	
56.2 kΩ, 1% Resistor	1	R5	Any	
Schottky Diode; 0.5 A, 20 V	2	D1	ON Semiconductor	MBR05S0L
Inductor 8.4 μH, 6 A	1	L1	Any	
Dual MOSFET with Schottky	1	Q	ON Semiconductor	FDS6986AS (Note 1)
PWM Controller	1	U1	ON Semiconductor	FAN5234

1. If currents above 4 A continuous are required, use single SO−8 packages. For more information, refer to the Power MOSFET Selection Section and AN−6002 for design calculations.

Layout Considerations

Switching converters, even during normal operation, produce short pulses of current that could cause substantial ringing and be a source of EMI if layout constrains are not observed.

There are two sets of critical components in a dc−dc converter. The switching power components process large amounts of energy at high rate and are noise generators. The low−power components responsible for bias and feedback functions are sensitive to noise.

A multi−layer printed circuit board is recommended. Dedicate one solid layer for a ground plane. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels.

Notice all the nodes that are subjected to high dV/dt voltage swing; such as SW, HDRV, and LDRV. All surrounding circuitry tends to couple the signals from these nodes through stray capacitance. Do not oversize copper traces connected to these nodes. Do not place traces connected to the feedback components adjacent to these traces. It is not recommended to use high density interconnect systems, or micro−vias, on these signals. The use of blind or buried vias should be limited to the low−current signals only. The use of normal thermal vias is at the discretion of the designer.

Keep the wiring traces from the IC to the MOSFET gate and source as short as possible and capable of handling peak currents of 2 A. Minimize the area within the gate−source path to reduce stray inductance and eliminate parasitic ringing at the gate.

Locate small critical components, like the soft−start capacitor and current sense resistors, as close as possible to the respective pins of the IC.

The FAN5234 utilizes advanced packaging technologies with lead pitches of 0.6 mm. High performance analog semiconductors utilizing narrow lead spacing may require special considerations in PWB design and manufacturing. It is critical to maintain proper cleanliness of the area surrounding these devices. It is not recommended to use any type of rosin or acid core solder, or the use of flux, in either the manufacturing or touch up process as these may contribute to corrosion or enable electro−migration and / or eddy currents near the sensitive low−current signals. When chemicals are used on or near the PWB, it is suggested that the entire PWB be cleaned and dried completely before applying power.

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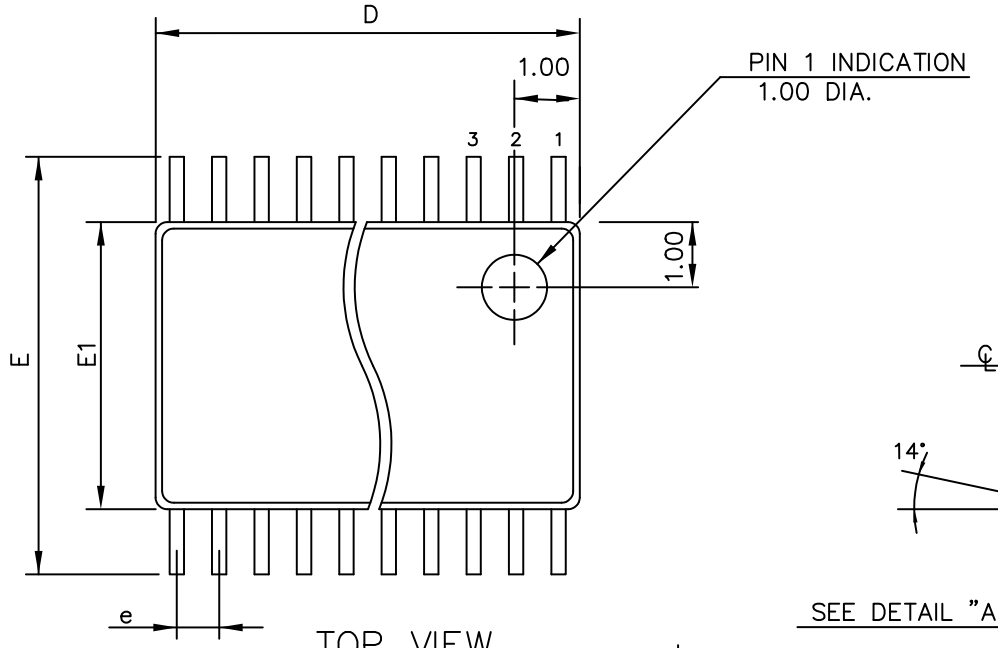
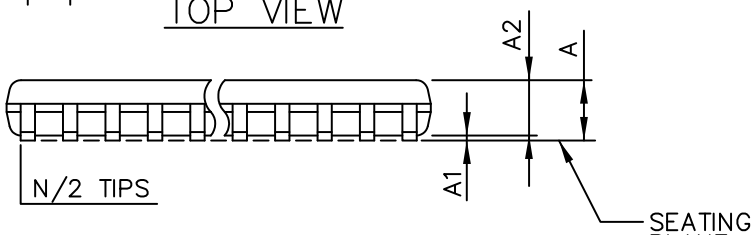
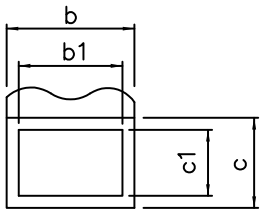


TOP VIEW

END VIEW



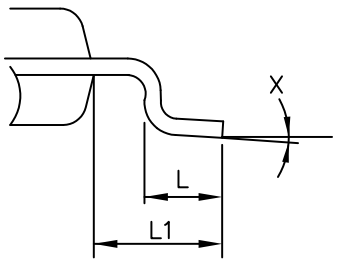
SIDE VIEW



SECTION "B–B"

THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	D	N
	MIN.	NOM.	MAX.			
A	——	——	1.10	AA/AAT	3.00 BSC	8
A_1	0.05	——	0.15	AB–1/ABT	5.00 BSC	14
A_2	0.85	0.90	0.95	AB/ABT	5.00 BSC	16
b	0.19	–	0.30	AD/ADT	7.80 BSC	24
b1	0.19	0.22	0.25			
c	0.09	–	0.20			
c1	0.09	0.127	0.16			
D	SEE VARIATIONS					
E1	4.30	4.40	4.50			
e	0.65 BSC					
E	6.40 BSC					
L	0.50	0.60	0.70			
L1	1.00 REF					
N	SEE VARIATIONS					
X	0°	——	8°			



DETAIL 'A'

ALL DIMENSIONS IN MILLIMETERS

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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