
FAIRCHILD

FAN5069 has a high gain error amplifier around which the loop is closed. Figure 24 shows a Type-3 compensation network. For Type-2 compensation, R3 and C3 are not used. Since the FAN5069 architecture employs summing current mode, Type-2 compensation can be used for most applications.

For further information about Type-2 compensation networks, refer to:

- *Venable, H. Dean, "The K factor: A new mathematical tool for stability analysis and synthesis," Proceedings of Powercon, March 1983.*

Note: For critical applications requiring wide loop bandwidth using very low ESR output capacitors, use Type-3 compensation.

Type 3 Feedback Component Calculations

Use the following steps to calculate feedback components:

Notation:

C_0 = Net Output Filter capacitance

$G_p(s)$ = Net Gain of Plant = control-to-output transfer function

L = Inductor Value

R_{DSON} = ON-state Drain-to Source Resistance of Low-side MOSFET

R_{es} = Net ESR of the Output Filter Capacitors

R_L = Load Resistance

T_s = Switching Period

V_{IN} = Input Voltage

F_{SW} = Switching Frequency

Equations:

Effective current sense resistance = $R_i = 2 \times R_{DSON}$ (EQ. 19)

Current modulator DC gain = $M_i = \frac{R_L}{R_i}$ (EQ. 20)

Effective ramp amplitude = $V_m = 3.33 \times 10^{10} \times \frac{(V_{IN} - 1.8) \times T_s}{R_{ramp}}$ (EQ. 21)

Voltage modulator DC gain = $M_v = \frac{V_{IN}}{V_m}$ (EQ. 22)

Plant DC gain = $M_o = M_v \| M_i = \frac{M_v \times M_i}{M_v + M_i}$ (EQ. 23)

Sampling gain natural frequency = $\omega_n = \frac{\pi}{T_s}$ (EQ. 24)

Sampling gain quality factor (damping) = $Q_z = \frac{-2}{\pi}$ (EQ. 25)

Effective inductance = $L_e = \frac{M_O}{M_v} \times \left(L + \frac{M_v \times R_i}{\omega_n \times Q_z}\right)$ (EQ. 26)

$R_p = \frac{M_v \times R_i \times R_L}{M_v \times R_i + R_L} = (M_v \times R_i) \| R_L$ (EQ. 27)

Poles and Zeros of Plant Transfer Function:

Plant zero frequency = $f_z = \frac{1}{2 \times \pi \times C_o \times R_{es}}$ (EQ. 28)

Plant 1st pole frequency = $f_{p1} = \frac{1}{2 \times \pi \times \left(C_o \times R_p + \frac{L_e}{R_L}\right)}$ (EQ. 29)

Plant 2nd pole frequency = $f_{p2} = \frac{1}{2 \times \pi} \times \left(\frac{1}{C_o \times R_L} + \frac{R_p}{L_e}\right)$ (EQ. 30)

Plant 3rd pole frequency = $f_{p3} = \frac{\omega_n^2 \times L_e}{2 \times \pi \times R_p}$ (EQ. 31)

Plant gain (magnitude) response:

$$|G_p|(f) = 20 \times \log M_0 + 10 \times \log\left[\frac{1 + \left(\frac{f}{f_z}\right)^2}{\left[1 + \left(\frac{f}{f_{p1}}\right)^2\right] \times \left[1 + \left(\frac{f}{f_{p2}}\right)^2\right] \times \left[1 + \left(\frac{f}{f_{p3}}\right)^2\right]}\right] \quad \text{(EQ. 32)}$$

Plant phase response:

$$\angle G_P(f) = \tan^{-1}\left(\frac{f}{f_z}\right) - \tan^{-1}\left(\frac{f}{f_{p1}}\right) - \tan^{-1}\left(\frac{f}{f_{p2}}\right) - -\tan^{-1}\left(\frac{f}{f_{p3}}\right) \quad \text{(EQ. 33)}$$

Choose R1, R_{BIAS} to set the output voltage to 0.6. Choose the zero crossover frequency F_{cross} of the overall loop. Typically F_{cross} should be less than fifth of F_{sw}. Choose the desired phase margin, typically between 60° to 90°.

Calculate plant gain at F_{cross} using EQ.34 by substituting F_{cross} in place of *f*. The gain that the amplifier needs to provide to get the required crossover is given by:

$$G_{AMP} = \frac{1}{|G_p|(F_{cross})} \quad \text{(EQ. 34)}$$

The phase boost required is calculated as given in (EQ. 35)

$$\text{Phase boost} = M - \angle G_P(F_{cross}) - 90° \quad \text{(EQ. 35)}$$

where M is the desired phase margin in degrees.

The feedback component values are calculated as given in equations below:

$$K = \left\{\tan\left[\left(\frac{\text{Boost}}{4}\right) + 45°\right]\right\}^2 \quad \text{(EQ. 36)}$$

$$C2 = \frac{1}{2 \times \pi \times F_{cross} \times G_{AMP} \times R1} \quad \text{(EQ. 37)}$$

$$C1 = C2 \times (K - 1) \quad \text{(EQ. 38)}$$

$$C3 = \frac{1}{2 \times \pi \times F_{cross} \times \sqrt{K} \times R3} \quad \text{(EQ. 39)}$$

$$R2 = \frac{\sqrt{K}}{2 \times \pi \times F_{cross} \times C1} \quad \text{(EQ. 40)}$$

$$R3 = \frac{R1}{(K - 1)} \quad \text{(EQ. 41)}$$

Design Tools

Fairchild application note **AN-6010** provides a PSPICE model and spreadsheet calculator for the PWM regulator, simplifying external component selections and verifying loop stability. The topics covered provide an understanding of the calculations in the spreadsheet.

The spreadsheet calculator, which is part of **AN-6010,** can be used to calculate all external component values for designing around FAN5069. The spreadsheet provides optimized compensation components and generates a Bode Plot to ensure loop stability.

Based on the input values entered, **AN-6010**'s PSPICE model can be used to simulate Bode Plots (for loop stability) as well as transient analysis to help customize the design for a wide range of applications.

Use Fairchild Application Note **AN-6005** for prediction of the losses and die temperatures for the power semiconductors used in the circuit.

AN-6010 and **AN-6005** can be downloaded from www.fairchildsemi.com/apnotes/.

Layout Considerations

The switching power converter layout needs careful attention and is critical to achieving low losses and clean and stable operation. Below are specific recommendations for good board layout:

- Keep the high-current traces and load connections as short as possible.
- Use thick copper boards whenever possible to achieve higher efficiency.
- Keep the loop area between the SW node, low-side MOSFET, inductor, and the output capacitor as small as possible.
- Route high dV/dt signals, such as SW node, away from the error amplifier input/output pin. Keep components connected to these pins close to the pins.
- Place ceramic de-coupling capacitor very close to the VCC pin.
- All input signals are referenced with respect to AGND pin. Dedicate one layer of the PCB for a GND plane. Use at least four layers for the PCB.
- Minimize GND loops in the layout to avoid EMI-related issues.
- Use wide traces for the lower gate drive to keep the drive impedances low.
- Connect PGND directly to the lower MOSFET source pin.
- Use wide land areas with appropriate thermal vias to effectively remove heat from the MOSFETs.
- Use snubber circuits to minimize high-frequency ringing at the SW nodes.
- Place the output capacitor for the LDO close to the source of the LDO MOSFET.

Application Board Schematic

V_{IN} = 3 to 24V; V_{OUT} =1.5V at 20A.

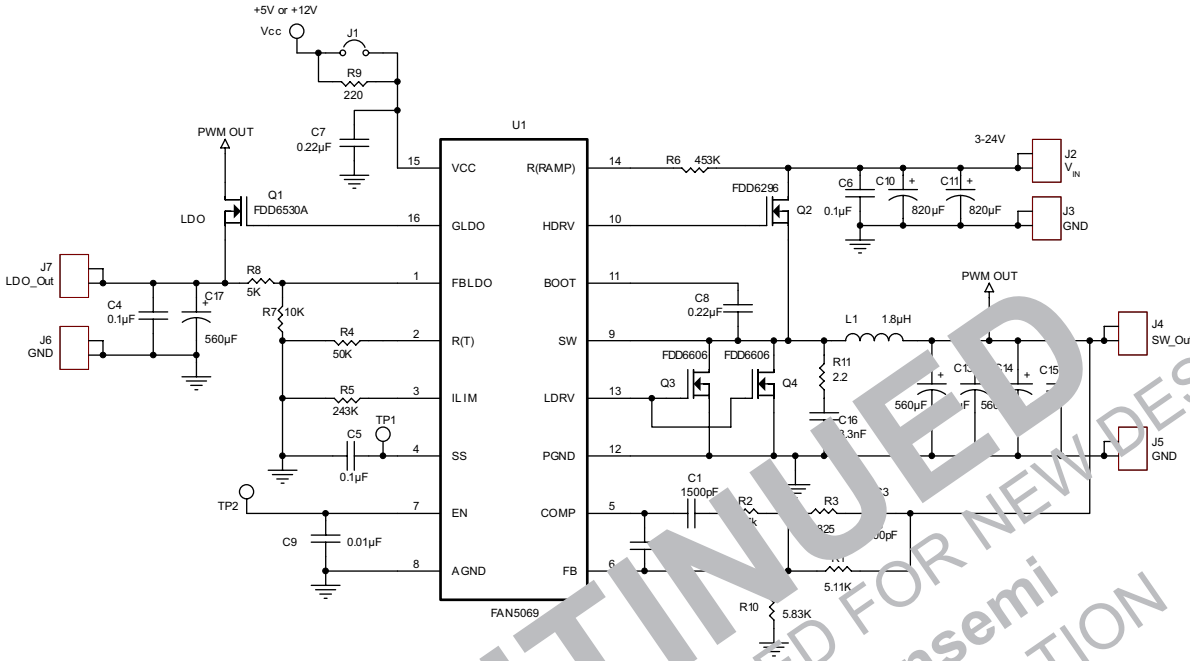


Figure 25. Application Board Schematic

Bill of Materials

Part Description	Quantity	Designator	Vendor	Vendor Part #
Capacitor, 1500pF, 20%, 25V, 0603,X7R	1	C1	Panasonic	PCC1774CT-ND
Capacitor, 220pF, 5%, 50V, 0603,NPO	1	C2	Panasonic	PCC221ACVCT-ND
Capacitor, 3300pF, 10%, 50V, 0603,X7R	1	C3	Panasonic	PCC1778CT-ND
Capacitor, 0.1µF, 10%, 25V, 0603,X7R	4	C4, C5, C6, C15	Panasonic	PCC2277CT-ND
Capacitor, 0.22µF, 10%, 50V, 0603,X7R	2	C7, C8	Panasonic	PCC1767CT-ND
Capacitor, 0.1µF, 10%, 50V, 0603,X7R	1	C9	Panasonic	PCC1784CT-ND
Capacitor, 820µF, 20%, 2.5V, 25V,20mOhm,1.96A	2	C10, C11	Nippon-Chemicon	KZH25VB820MHJ20
Capacitor, 820µF, 20%, 8X8, 2.5V,7mOhm,6.1A	1	C17	Nippon-Chemicon	PSC2.5VB820MH08
Capacitor, 560µF, 20%, 8X11.5, 4V,7mOhm,5.58A	3	C12, C13, C14	Nippon-Chemicon	PSA4VB560MH11
Capacitor, 1000pF, 10%, 50V, 0603,X7R	1	C16	Panasonic	PCC332BNCT-ND
Connector Header 0.100 Vertical, Tin - 2 Pin	1	J1	Molex	WM6436-ND
Terminal Quickfit Male .052"Dia.187" Tab	6	J2 - J7	Keystone	1212K-ND
Inductor, 1.8µH, 20%, 26Amps Max, 3.24mOhm	1	L1	Inter-Technical	SC5018-1R8M
MOSFET N-CH, 32 mΩ, 20V, 21A, D-PAK, FSID: FDD6530A	1	Q1	Fairchild Semiconductor	FDD6530A
MOSFET N-CH, 8.8 mΩ, 30V, 50A, D-PAK, FSID: FDD6296	1	Q2	Fairchild Semiconductor	FDD6296
MOSFET N-CH, 6 mΩ, 30V, 75A, D-PAK, FSID: FDD6606	2	Q3, Q4	Fairchild Semiconductor	FDD6606
Resistor, 5.11K, 1%, 1/16W	1	R1	Panasonic	P5.11KHCT-ND
Resistor, 12.7K, 1%, 1/16W	1	R2	Panasonic	P12.7KHCT-ND
Resistor, 825Ω, 1%, 1/16W	1	R3	Panasonic	P825HCT-ND
Resistor, 49.9K, 1%, 1/16W	1	R4	Panasonic	P49.9KHCT-ND
Resistor, 243K, 1%, 1/16W	1	R5	Panasonic	P243KHCT-ND
Resistor,453K, 1%, 1/16W	1	R6	Panasonic	P453KHCT-ND
Resistor,10K, 1%, 1/16W	1	R7	Panasonic	P10.0KHCT-ND
Resistor, 4.99K, 1%, 1/16W	1	R8	Panasonic	P4.99KHCT-ND
Resistor, 220Ω, 1%, 1/4W	1	R9	Panasonic	P200FCT-ND
Resistor, 5.90K, 1%, 1/16W	1	R10	Panasonic	P5.90KHCT-ND
Resistor, 2.2Ω, 1%, 1/4W	1	R11	Panasonic	P2.2ECT-ND
Connector Header 0.100 Vertical, Tin - 1 Pin	3	TP1,TP2, Vcc	Molex	WM6436-ND
IC, System Regulator, TSSOP16, FSID: FAN5069	1	U1	Fairchild Semiconductor	FAIRCHILD

Typical Application Board Layout

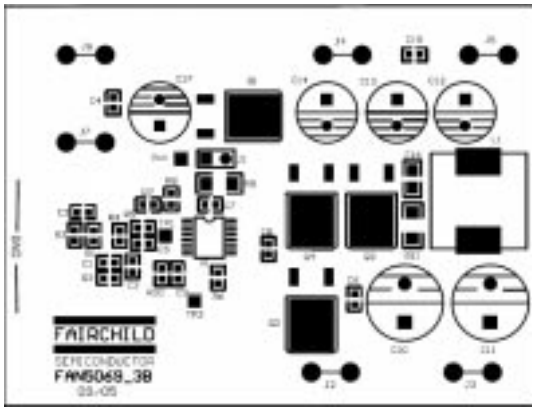


Figure 26. Assembly Diagram

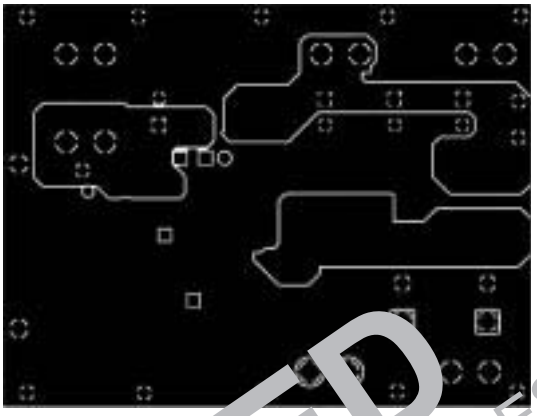


Figure 29. Mid Layer 2

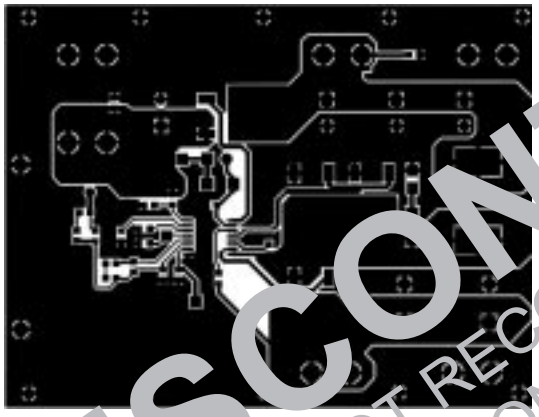


Figure 27. Top Layer

Figure 30. Bottom Layer

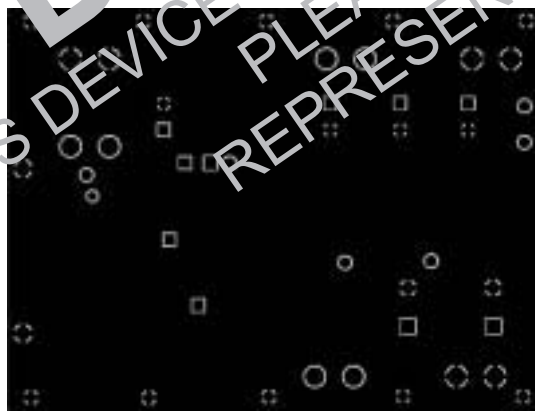
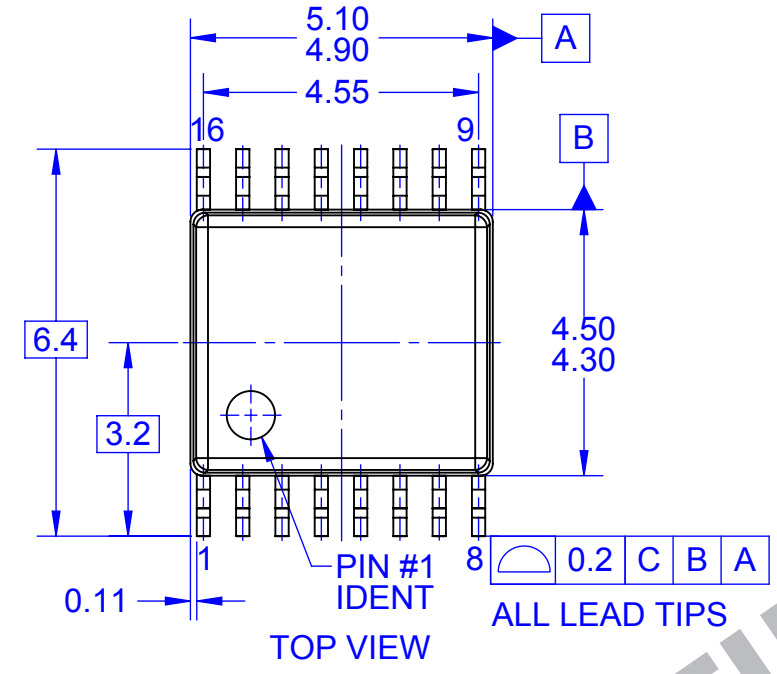
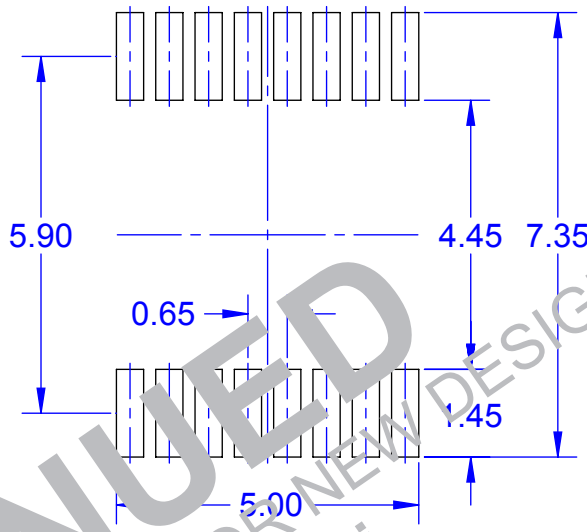
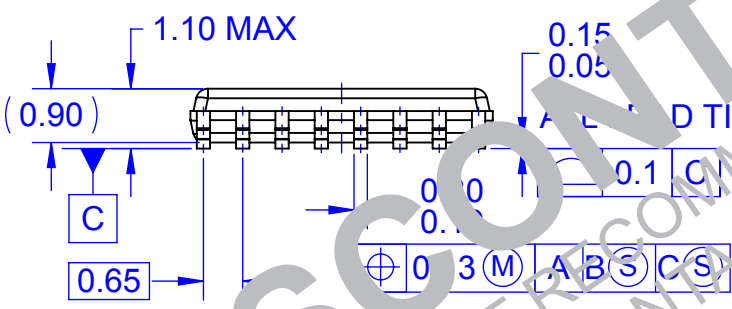
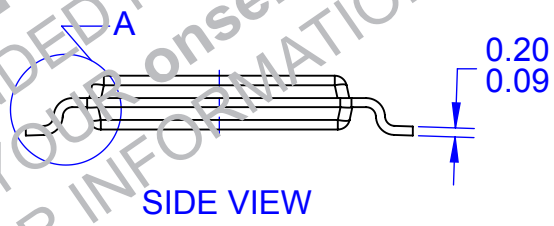


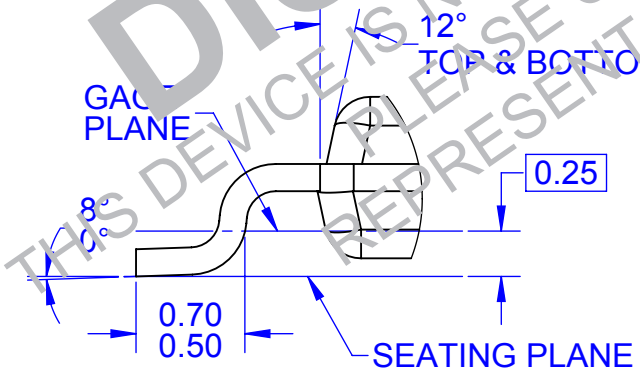
Figure 28. Mid Layer 1











NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB
B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009
E. LAND PATTERN RECOMMENDATION PER IPC7351 - ID# TSOP65P640X110-16N
F. DRAWING FILENAME: MKT-MTC16rev5

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