

# Fixed-Output Synchronous Regulator, TINYBOOST<sup>®</sup>, 2.5 MHz

## FAN48610

### Description

The FAN48610 is a low-power boost regulator designed to provide a minimum voltage-regulated rail from a standard single-cell Li-Ion battery and advanced battery chemistries. Even below the minimum system battery voltage, the device maintains the output voltage regulation for a minimum output load current of 1.0 A. The combination of built-in power transistors, synchronous rectification, and low supply current suit the FAN48610 for battery-powered applications.

The FAN48610 is available in a 9-bump, 0.4 mm pitch, Wafer-Level Chip-Scale Package (WLCSP).

### Features

- Input Voltage Range: 2.5 V to 4.8 V
- Output Voltages Range: 3.0 V to 5.0 V
- $I_{OUT} \geq 1 \text{ A}$  at  $V_{OUT} = 5.0 \text{ V}$ ,  $V_{IN} \geq 2.5 \text{ V}$
- $I_{OUT} \geq 1.5 \text{ A}$  at  $V_{OUT} = 5.0 \text{ V}$ ,  $V_{IN} \geq 3.0 \text{ V}$
- Up to 94% Efficient
- Internal Synchronous Rectification
- Soft-Start with True Load Disconnect
- Short-Circuit Protection
- 9-Bump, 1.215 mm × 1.215 mm, 0.4 mm Pitch WLCSP
- Three External Components: 2016 0.47  $\mu\text{H}$  Inductor, 0603 Case Size Input / Output Capacitors
- Total Application Board Solution Size: < 11 mm<sup>2</sup>

### Applications

- Class-D Audio Amplifier and USB OTG Supply
- Boost for Low-Voltage Li-Ion Batteries
- Smart Phones, Tablets, Portable Devices, Wearables

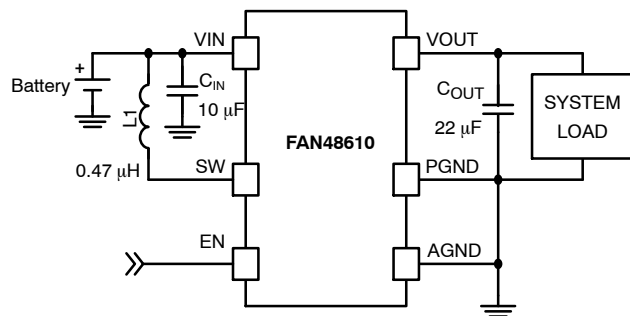


Figure 1. Typical Application



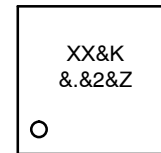
ON Semiconductor<sup>®</sup>

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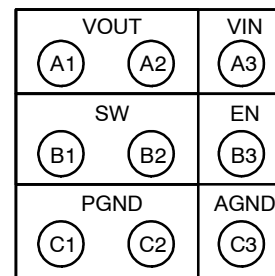
WLCSP9  
CASE 567QW

### MARKING DIAGRAM



XX = KA / KF / KN  
&K = Lot Code  
&. = Alphabetical Year Code  
&2 = Numeric Date Code  
&Z = Assembly Plant Code

### PIN ASSIGNMENT



(Top View)

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FAN48610

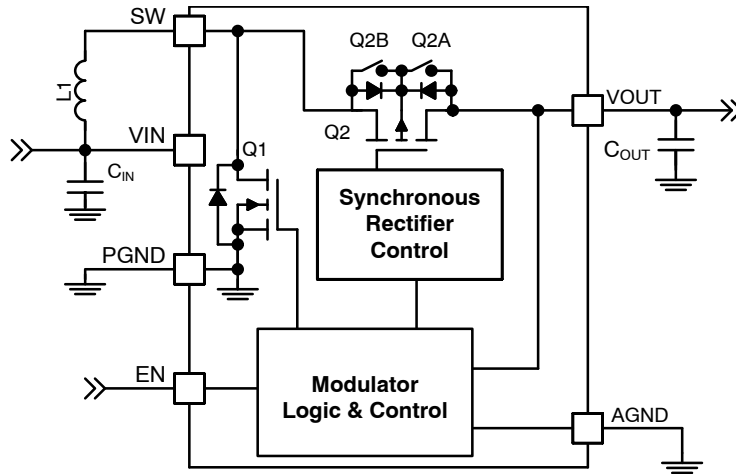
**Table 1. ORDERING INFORMATION**

Part Number	V <sub>OUT</sub>	Operating Temperature	Package	Packing <sup>†</sup>	Device Marking
FAN48610UC50X	5.0 V	-40°C to 85°C	WLCSP, 0.4 mm Pitch	Tape and Reel	KF
FAN48610BUC50X (Note 1)					
FAN48610BUC45X (Note 1)	4.5 V				KA
FAN48610BUC33X (Note 1)	3.3 V				KN

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. Includes backside lamination.

## BLOCK DIAGRAM



**Figure 2. IC Block Diagram**

**Table 2. RECOMMENDED COMPONENTS**

Component	Description	Ventor	Parameter	Typ.	Unit
L1	0.47 $\mu$ H, 30%, 2016	Toko: DFE201612C DFR201612C Cyntec: PIFE20161B	L	0.47	$\mu$ H
			DCR (Series R)	40	m $\Omega$
C <sub>IN</sub>	10 $\mu$ F, 10%, 6.3 V, X5R, 0603	Murata: GRM188R60J106K TDK: C1608X5R0J106K	C	10	$\mu$ F
C <sub>OUT</sub>	22 $\mu$ F, 20%, 6.3 V, X5R, 0603	TDK: C1608X5R0J226M	C	22	$\mu$ F

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## PIN CONFIGURATION

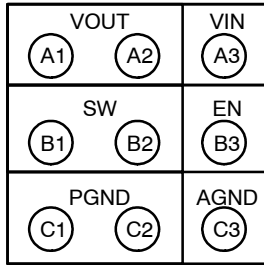


Figure 3. Top View

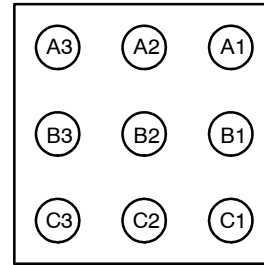


Figure 4. Bottom View

Table 3. PIN DEFINITIONS

Pin #	Name	Description
A1, A2	VOUT	<b>Output Voltage.</b> This pin is the output voltage terminal; connect directly to C <sub>OUT</sub> .
A3	VIN	<b>Input Voltage.</b> Connect to Li-Ion battery input power source and the bias supply for the gate drivers.
B1, B2	SW	<b>Switching Node.</b> Connect to inductor.
B3	EN	<b>Enable.</b> When this pin is HIGH, the circuit is enabled.
C1, C2	PGND	<b>Power Ground.</b> This is the power return for the IC. C <sub>OUT</sub> capacitor should be returned with the shortest path possible to these pins.
C3	AGND	<b>Analog Ground.</b> This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin – connect to PGND at a single point.

Table 4. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min.	Max.	Unit
V <sub>IN</sub>	Voltage on VIN Pin		-0.3	6.0	V
V <sub>OUT</sub>	Voltage on VOUT Pin			6.0	V
SW	SW Node	DC	-0.3	6.0	V
		Transient: 10 ns, 3 MHz	-1.0	8.0	
V <sub>CC</sub>	Voltage on Other Pins		-0.3	6.0 (Note 2)	V
ESD	Electrostatic Discharge Protection Level	Human Body Model per JESD22-A114	2		kV
		Charged Device Model per JESD22-C101	1		
T <sub>J</sub>	Junction Temperature		-40	+150	°C
T <sub>STG</sub>	Storage Temperature		-65	+150	°C
T <sub>L</sub>	Lead Soldering Temperature, 10 Seconds			+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Lesser of 6.0 V or V<sub>IN</sub> + 0.3 V.

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**Table 5. RECOMMENDED OPERATING CONDITIONS**

Symbol	Parameter	Min.	Max.	Unit
V <sub>IN</sub>	Supply Voltage	2.5	4.8	V
I <sub>OUT</sub>	Maximum Output Current	1000		mA
T <sub>A</sub>	Ambient Temperature	-40	+85	°C
T <sub>J</sub>	Junction Temperature	-40	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 6. THERMAL PROPERTIES**

Symbol	Parameter	Typical	Unit
θ <sub>JA</sub>	Junction-to-Ambient Thermal Resistance	50	°C/W

Junction-to-ambient thermal resistance is a function of application and board layout. This data is measured with four-layer 2s2p boards in accordance to JEDEC standard JESD51. Special attention must be paid not to exceed junction temperature T<sub>J(max)</sub> at a given ambient temperature T<sub>A</sub>.

**Table 7. ELECTRICAL CHARACTERISTICS**

(Recommended operating conditions, unless otherwise noted, circuit per Figure 1, V<sub>OUT</sub> = 3.0 V to 5.0 V, V<sub>IN</sub> = 2.5 V to 4.5 V, T<sub>A</sub> = -40°C to 85°C. Typical values are given V<sub>IN</sub> = 3.6 V and T<sub>A</sub> = 25°C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
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**POWER SUPPLY**

I <sub>Q</sub>	V <sub>IN</sub> Quiescent Current	V <sub>IN</sub> = 3.6 V, I <sub>OUT</sub> = 0 A, EN = V <sub>IN</sub>		85	125	μA
		Shutdown: EN = 0, V <sub>IN</sub> = 3.6 V		3	10	
V <sub>UVLO</sub>	Under-Voltage Lockout	V <sub>IN</sub> Rising		2.2	2.3	V
V <sub>UVLO_HYS</sub>	Under-Voltage Lockout Hysteresis			150		mV

**INPUTS**

V <sub>IH</sub>	Enable HIGH Voltage		1.05			V
V <sub>IL</sub>	Enable LOW Voltage				0.4	V
I <sub>PD</sub>	Current Sink Pull-Down	EN Pin, Logic HIGH		100		nA
R <sub>LOW</sub>	Low-State Active Pull-Down	EN Pin, Logic LOW	200	300	400	kΩ

**OUTPUTS**

V <sub>REG</sub>	Output Voltage Accuracy DC (Note 3)	Referred to V <sub>OUT</sub> , 2.5 V ≤ V <sub>IN</sub> ≤ V <sub>OUT</sub> - 150 mV	-2		4	%
I <sub>LK_OUT</sub>	VIN-to-VOUT Leakage Current	V <sub>OUT</sub> = 0, EN = 0, V <sub>IN</sub> = 4.2 V			1	μA
I <sub>LK</sub>	VOUT-to-VIN Reverse Leakage Current	V <sub>OUT</sub> = 5.0 V, EN = 0, V <sub>IN</sub> = 2.5 V			3.5	μA
V <sub>TRSP</sub>	Output Voltage Accuracy Transient (Note 4)	Referred to V <sub>OUT</sub> , 50-500 mA Load Step	-5		5	%

**TIMING**

f <sub>SW</sub>	Switching Frequency	V <sub>IN</sub> = 3.6 V, V <sub>OUT</sub> = 5.0 V, Load = 1000 mA	2.0	2.5	3.0	MHz
t <sub>SS</sub>	Soft-Start EN HIGH to Regulation (Note 4)	50 Ω Load, V <sub>OUT</sub> = 5.0 V		600		μA
t <sub>RST</sub>	FAULT Restart Timer (Note 4)			20		ms

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**Table 7. ELECTRICAL CHARACTERISTICS** (continued)

(Recommended operating conditions, unless otherwise noted, circuit per Figure 1,  $V_{OUT}$  = 3.0 V to 5.0 V,  $V_{IN}$  = 2.5 V to 4.5 V,  $T_A$  =  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Typical values are given  $V_{IN}$  = 3.6 V and  $T_A$  =  $25^{\circ}\text{C}$ )

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>POWER STAGE</b>						
$R_{DS(ON)N}$	N-Channel Boost Switch $R_{DS(ON)}$	$V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 5.0\text{ V}$		80	130	$\text{m}\Omega$
$R_{DS(ON)P}$	P-Channel Sync. Rectifier $R_{DS(ON)}$	$V_{IN} = 3.6\text{ V}$ , $V_{OUT} = 5.0\text{ V}$		65	115	$\text{m}\Omega$
$I_{V\_LIM}$	Boost Valley Current Limit	$V_{OUT} = 5.0\text{ V}$		3.00	3.85	A
$I_{V\_LIM\_SS}$	Boost Soft-Start Valley Current Limit	$V_{IN} < V_{OUT} < V_{OUT\_TARGET}$ , SS Mode		1.7		A
$V_{MIN\_1.0A}$	Minimum $V_{IN}$ for 1000 mA Load (Note 4)	$V_{OUT} = 5.0\text{ V}$		2.5		V
$V_{MIN\_1.5A}$	Minimum $V_{IN}$ for 1500 mA Load (Note 4)	$V_{OUT} = 5.0\text{ V}$		3.0		V
$T_{150T}$	Over-Temperature Protection (OTP)			150		$^{\circ}\text{C}$
$T_{150H}$	OTP Hysteresis			20		$^{\circ}\text{C}$

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- DC  $I_{LOAD}$  from 0 to 1 A.  $V_{OUT}$  measured from mid-point of output voltage ripple. Effective capacitance of  $C_{OUT} \geq 3\ \mu\text{F}$ .
- Guaranteed by design and characterization; not tested in production.

TYPICAL CHARACTERISTICS

(Unless otherwise specified;  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and circuit and components according to Figure 1)

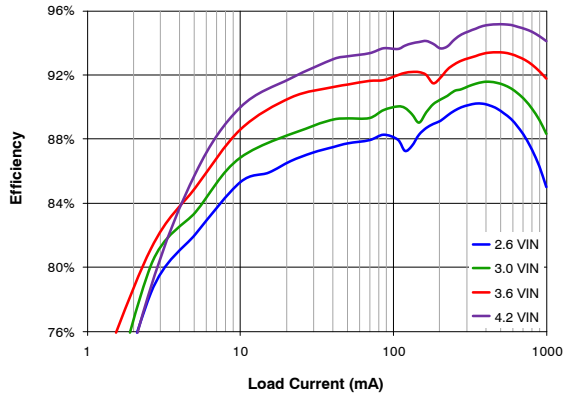


Figure 5. Efficiency vs. Load Current and Input Voltage

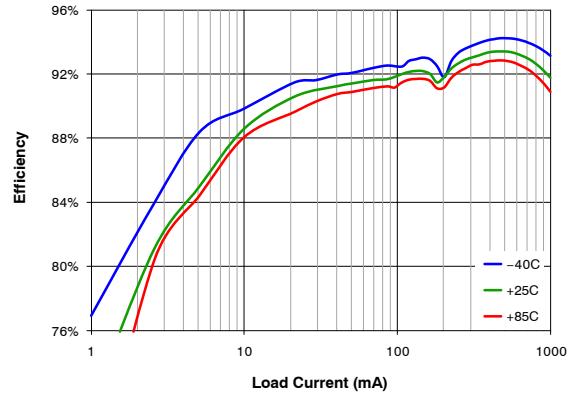


Figure 6. Efficiency vs. Load Current and Temperature

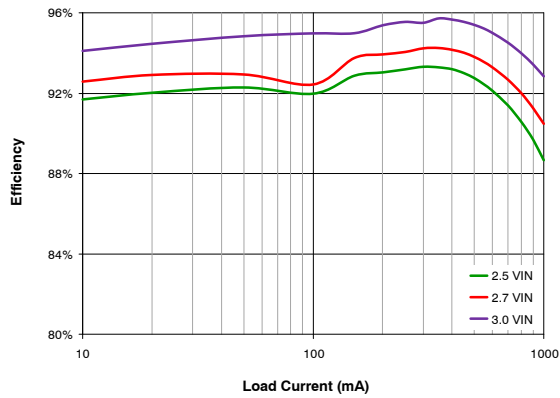


Figure 7. Efficiency vs. Load Current and Input Voltage,  $V_{OUT} = 3.3\text{ V}$

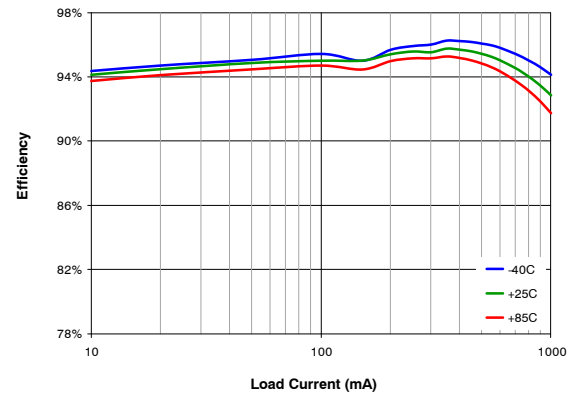


Figure 8. Efficiency vs. Load Current and Temperature,  $V_{IN} = 3.0\text{ V}$ ,  $V_{OUT} = 3.3\text{ V}$

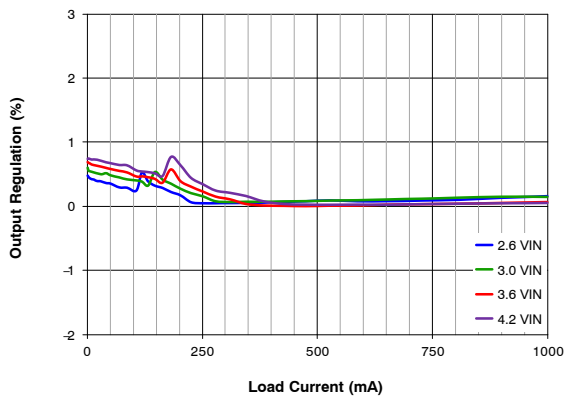


Figure 9. Output Regulation vs. Load Current and Input Voltage (Normalized to  $3.6\text{ V}_{IN}$ , 500 mA Load)

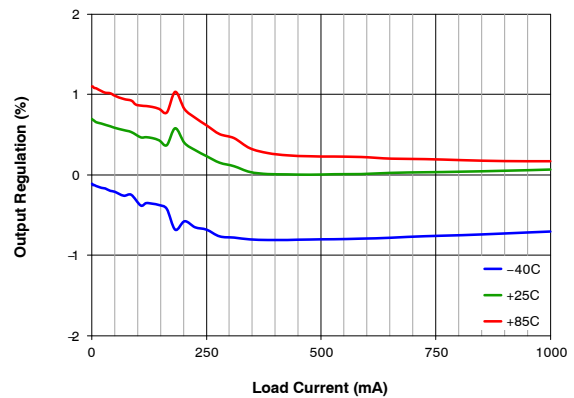


Figure 10. Output Regulation vs. Load Current and Temperature (Normalized to  $3.6\text{ V}_{IN}$ , 500 mA Load,  $T_A = 25^\circ\text{C}$ )

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## TYPICAL CHARACTERISTICS

(Unless otherwise specified;  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and circuit and components according to Figure 1)

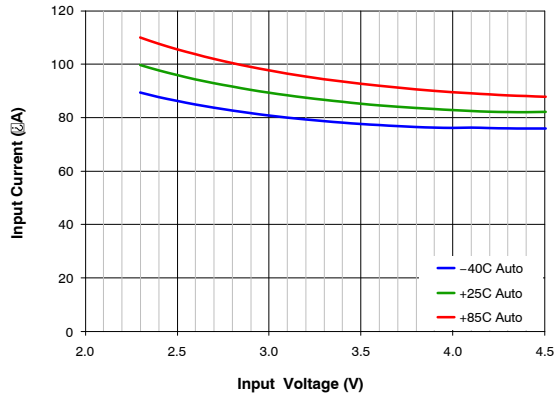


Figure 11. Quiescent Current vs. Input Voltage, Temperature

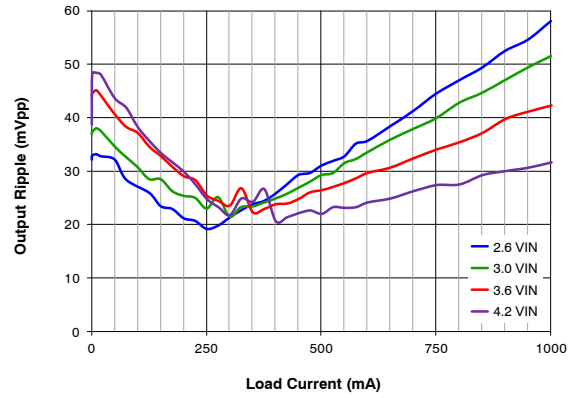


Figure 12. Output Ripple vs. Load Current and Input Voltage

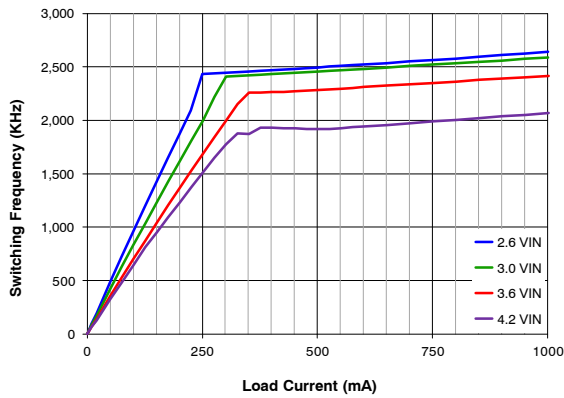


Figure 13. Frequency vs. Load Current and Input Voltage

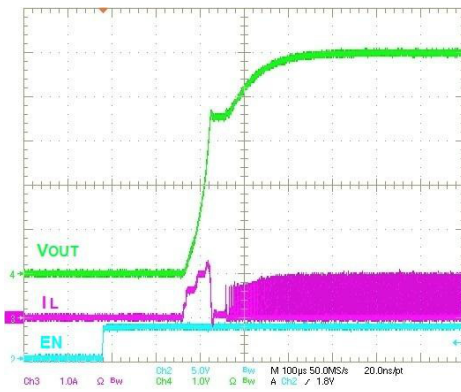


Figure 14. Startup, 50  $\Omega$  Load

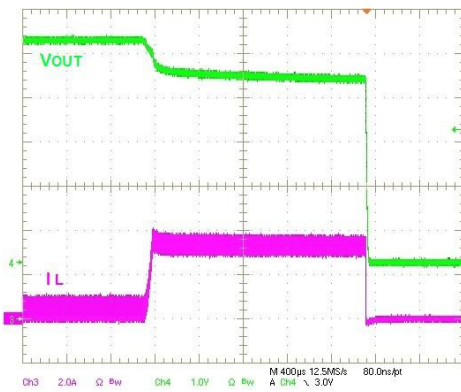


Figure 15. Overload Protection

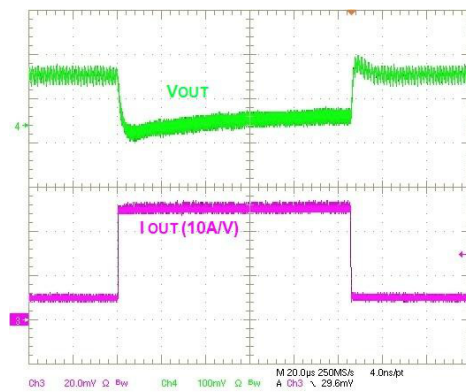
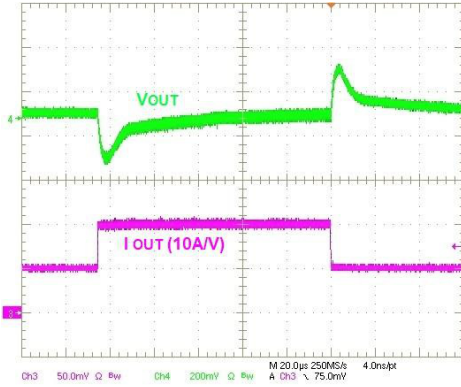


Figure 16. Load Transient, 100–500 mA, 100 ns Edge

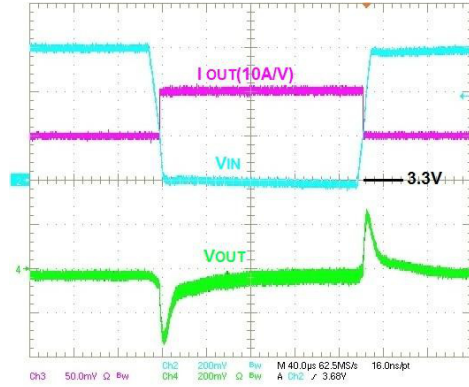
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## TYPICAL CHARACTERISTICS

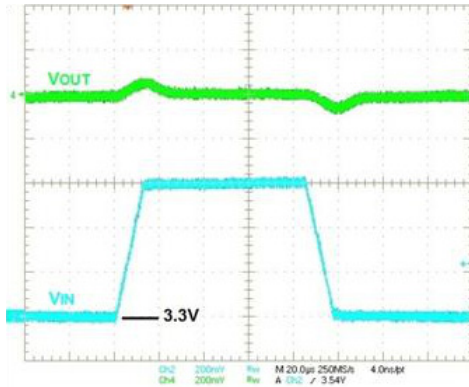
(Unless otherwise specified;  $V_{IN} = 3.6\text{ V}$ ,  $V_{OUT} = 5.0\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , and circuit and components according to Figure 1)



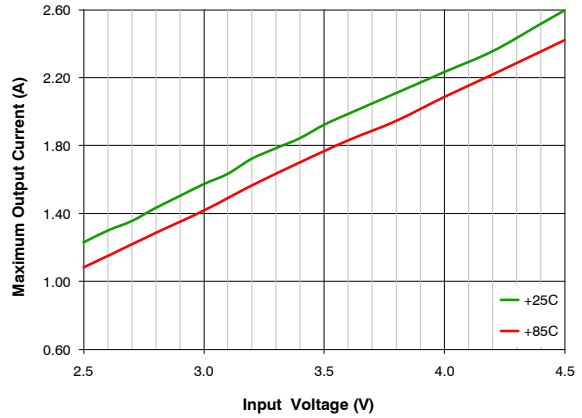
**Figure 17. Load Transient, 500–1000 mA, 100 ns Edge**



**Figure 18. Simultaneous Line / Load Transient, 3.3 –3.9  $V_{IN}$ , 10  $\mu\text{s}$  Edge, 500–1000 mA Load, 100 ns Edge**



**Figure 19. Line Transient, 3.3–3.9  $V_{IN}$ , 10  $\mu\text{s}$  Edge, 500 mA Load**



**Figure 20. Typical Maximum Output Current vs. Input Voltage**



CIRCUIT DESCRIPTION

FAN48610 is a synchronous boost regulator, typically operating at 2.5 MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low  $V_{IN}$  voltages. The regulator's Pass-Through Mode automatically activates when  $V_{IN}$  is above the boost regulator's set point.

**Boost Mode Regulation**

The FAN48610 uses a current-mode modulator to achieve excellent transient response and smooth transitions between CCM and DCM operation. During CCM operation, the device maintains a switching frequency of about 2.5 MHz. In lightload operation (DCM), frequency is naturally reduced to maintain high efficiency.

**Table 8. OPERATING MODES**

Mode	Description	Invoked When:
LIN	Linear Startup	$V_{IN} > V_{OUT}$
SS	Boost Soft-Start	$V_{IN} < V_{OUT} < V_{OUT(TARGET)}$
BST	Boost Operating Mode	$V_{OUT} = V_{OUT(TARGET)}$
PT	Pass-Through Mode	$V_{IN} > V_{OUT(TARGET)}$

**Shutdown and Startup**

When EN is LOW, all bias circuits are off and the regulator is in Shutdown Mode. During shutdown, current flow is prevented from  $V_{IN}$  to  $V_{OUT}$ , as well as reverse flow from  $V_{OUT}$  to  $V_{IN}$ . It is recommended to keep load current draw below 500 mA until the devices successfully executes startup. The following table describes the startup sequence.

**Table 9. BOOST STARTUP SEQUENCE**

Start Mode	Entry	Exit	End Mode	Timeout ( $\mu$ s)
LIN1	$V_{IN} > V_{UVLO}$ , EN = 1	$V_{OUT} > V_{IN} - 300$ mV	SS	
		TIMEOUT	LIN2	512
LIN2	LIN1 Exit	$V_{OUT} > V_{IN} - 300$ mV	SS	
		TIMEOUT	FAULT	1024
SS	LIN1 or LIN2 Exit	$V_{OUT} = V_{OUT(TARGET)}$	BST	
		OVERLOAD TIMEOUT	FAULT	64

**LIN Mode**

When EN is HIGH and  $V_{IN} > V_{UVLO}$ , the regulator first attempts to bring  $V_{OUT}$  within 300 mV of  $V_{IN}$  by using the internal fixed-current source from  $V_{IN}$  (Q2). The current is limited to the LIN1 set point.

If  $V_{OUT}$  reaches  $V_{IN} - 300$  mV during LIN1 Mode, the SS Mode is initiated. Otherwise, LIN1 times out after 512  $\mu$ s and LIN2 Mode is entered.

In LIN2 Mode, the current source is incremented to 1.6 A. If  $V_{OUT}$  fails to reach  $V_{IN} - 300$  mV after 1024  $\mu$ s, a fault condition is declared and the device waits 20 ms to attempt an automatic restart.

**Soft-Start (SS) Mode**

Upon the successful completion of LIN Mode ( $V_{OUT} \geq V_{IN} - 300$  mV), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS Mode, if  $V_{OUT}$  fails to reach regulation during the SS ramp sequence for more than 64  $\mu$ s, a fault is declared. If large  $C_{OUT}$  is used, the reference is automatically stepped slower to avoid excessive input current draw.

**Boost (BST) Mode**

This is a normal operating mode of the regulator.

**Pass-Through (PT) Mode**

In normal operation, the device automatically transitions from Boost Mode to Pass-Through Mode if  $V_{IN}$  goes above the target  $V_{OUT}$ . In Pass-Through Mode, the device fully enhances Q2 to provide a very low impedance path from  $V_{IN}$  to  $V_{OUT}$ . Entry to the Pass-Through Mode is triggered by condition where  $V_{IN} > V_{OUT}$  and no switching has occurred during the past 5  $\mu$ s. To soften the entry into Pass-Through Mode, Q2 is driven as a linear current source for the first 5  $\mu$ s. Pass-Through Mode exit is triggered when  $V_{OUT}$  reaches the target  $V_{OUT}$  voltage. During Automatic Pass-Through Mode, the device is short-circuit protected by a voltage comparator tracking the voltage drop from  $V_{IN}$  to  $V_{OUT}$ ; if the drop exceeds 300 mV, a fault is declared.

**Fault State**

The regulator enters Fault State under any of the following conditions:

- $V_{OUT}$  fails to achieve the voltage required to advance from LIN Mode to SS Mode.
- $V_{OUT}$  fails to achieve the voltage required to advance from SS Mode to BST Mode.
- Boost current limit triggers for 2 ms during BST Mode.

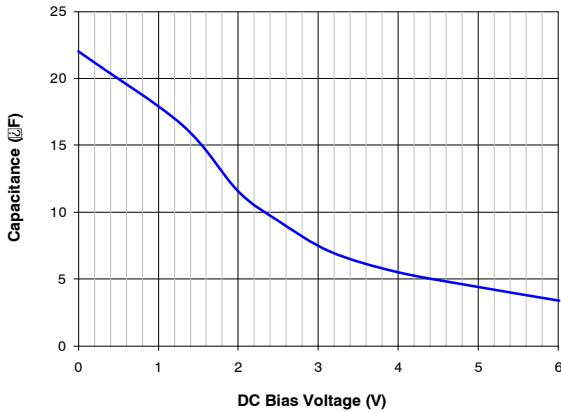
- $V_{IN} - V_{OUT} > 300$  mV; this fault can occur only after successful completion of the soft-start sequence.
- $V_{IN} < V_{UVLO}$ .

Once a fault is triggered, the regulator stops switching and presents a high-impedance path between VIN and VOUT. After waiting 20 ms, an automatic restart is attempted.

**APPLICATION INFORMATION**

**Output Capacitance (C<sub>OUT</sub>)**

The effective capacitance (C<sub>EFF</sub> (Note 5)) of small, high-value ceramic capacitors decreases as their bias voltage increases, as illustrated in the graph below:



**Figure 21. C<sub>EFF</sub> for 22 µF, 0603, X5R, 6.3 V-Rated Capacitor (TDK C1608X5R0J226M)**

FAN48610 is guaranteed for stable operation with the minimum value of C<sub>EFF</sub> (C<sub>EFF(MIN)</sub>) outlined in Table 10.

**Table 10. MINIMUM C<sub>EFF</sub> REQUIRED FOR STABILITY**

Operating Conditions			C <sub>EFF(MIN)</sub> (µF)
V <sub>OUT</sub> (V)	V <sub>IN</sub> (V)	I <sub>LOAD</sub> (mA)	
5.0	2.5 to 4.5	0 to 1000	3.0

5. C<sub>EFF</sub> varies by manufacturer, capacitor material, and case size.

**Introduction Selection**

Recommended nominal inductance value is 0.47 µH. The FAN48610 employs valley-current limiting, so peak inductor current can reach 3.8 A for a short duration during overload conditions. Saturation effects cause the inductor current ripple to become higher under high loading, as only the valley of the inductor current ripple is controlled.

**Startup**

Input current limiting is in effect during soft-start, which limits the current available to charge C<sub>OUT</sub> and any

**Over-Temperature**

The regulator shuts down if the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

additional capacitance on the V<sub>OUT</sub> line. If the output fails to achieve regulation within the limits described in the Soft-Start section above, a fault occurs, causing the circuit to shut down. It waits about 20 ms before attempting a restart. If the total combined output capacitance is very high, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high current load and high capacitance are both present during soft-start, the circuit may fail to achieve regulation and continually attempt soft-start, only to have the output capacitance discharged by the load when in Fault State.

**Output Voltage Ripple**

Output voltage ripple is inversely proportional to C<sub>OUT</sub>. During t<sub>ON</sub>, when the boost switch is on, all load current is supplied by C<sub>OUT</sub>.

$$V_{\text{RIPPLE(P-P)}} = t_{\text{ON}} \cdot \frac{I_{\text{LOAD}}}{C_{\text{OUT}}} \quad (\text{eq. 1})$$

And

$$t_{\text{ON}} = t_{\text{SW}} \cdot D = t_{\text{SW}} \cdot \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right) \quad (\text{eq. 2})$$

therefore:

$$V_{\text{RIPPLE(P-P)}} = t_{\text{SW}} \cdot \left(1 - \frac{V_{\text{IN}}}{V_{\text{OUT}}}\right) \cdot \frac{I_{\text{LOAD}}}{C_{\text{OUT}}} \quad (\text{eq. 3})$$

$$t_{\text{SW}} = \frac{1}{f_{\text{SW}}} \quad (\text{eq. 4})$$

The maximum V<sub>RIPPLE</sub> occurs when V<sub>IN</sub> is minimum and I<sub>LOAD</sub> is maximum. For better ripple performance, more output capacitance can be added.

**Layout Recommendations**

The layout recommendations below highlight various topcopper pours by using different colors.

To minimize spikes at V<sub>OUT</sub>, C<sub>OUT</sub> must be placed as close as possible to PGND and V<sub>OUT</sub>, as shown below.

For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal vias.

# FAN48610

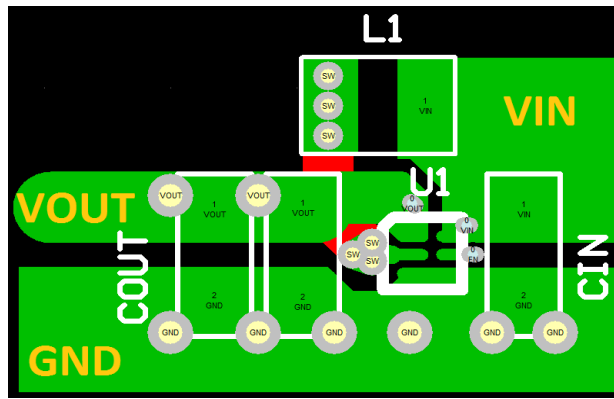


Figure 22. Layout Recommendation

**PRODUCT-SPECIFIC DIMENSIONS** (This table pertains to the package information on the following page.)

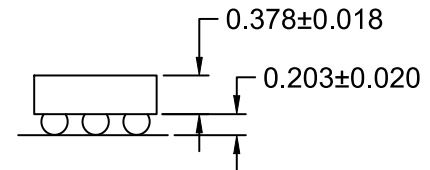
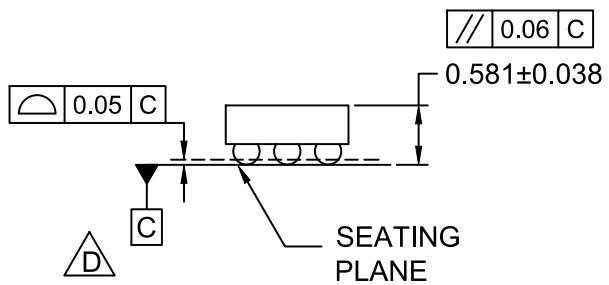
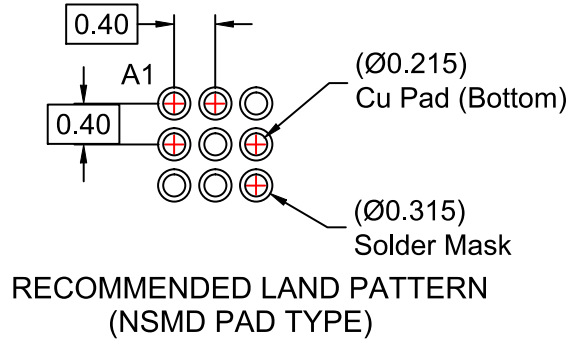
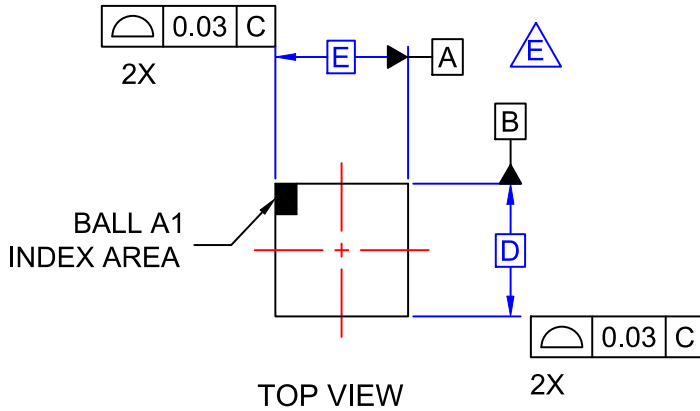
D	E	X	Y
1.215 ±0.030 mm	1.215 ±0.030 mm	0.2075 mm	0.2075 mm

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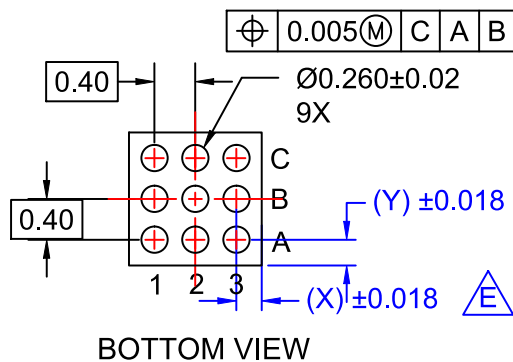


**WLCSP9 1.215x1.215x0.581**  
CASE 567QW  
ISSUE O

DATE 31 OCT 2016



SIDE VIEWS



BOTTOM VIEW

**NOTES**

- A. NO JEDEC REGISTRATION APPLIES.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.
- D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
- E. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

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