# 3.3V ESD Protection Diodes

## Ultra Low Capacitance ESD Protection Diode for High Speed Data Line

# ESDL1531

The ESDL1531 ESD protection diodes are designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines.

### Features

- Low Capacitance (0.15 pF Typ, I/O to GND)
- Protection for the Following IEC Standards: IEC 61000−4−2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

### Typical Applications

- USB 2.0/3.x
- Thunderbolt
- MHL 2.0
- eSATA

**MAXIMUM RATINGS** ($T_J$ = 25°C unless otherwise noted)

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Operating Junction Temperature Range | $T_J$ | −55 to +150 | °C |
| Storage Temperature Range | $T_{stg}$ | −55 to +150 | °C |
| Lead Solder Temperature − Maximum (10 Seconds) | $T_L$ | 260 | °C |
| IEC 61000−4−2 Contact<br>IEC 61000−4−2 Air | ESD | ±30<br>±30 | kV<br>kV |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

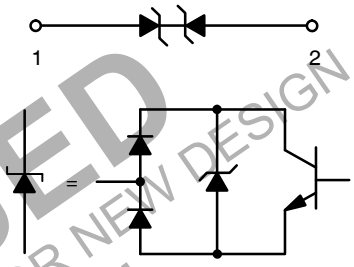
See Application Note AND8308/D for further description of survivability specs.

**MARKING DIAGRAM**

ESDL1531
X4DFN2 (01005)
CASE 718AA


J = Device Code
M = Date Code

**PIN CONFIGURATION AND SCHEMATIC**



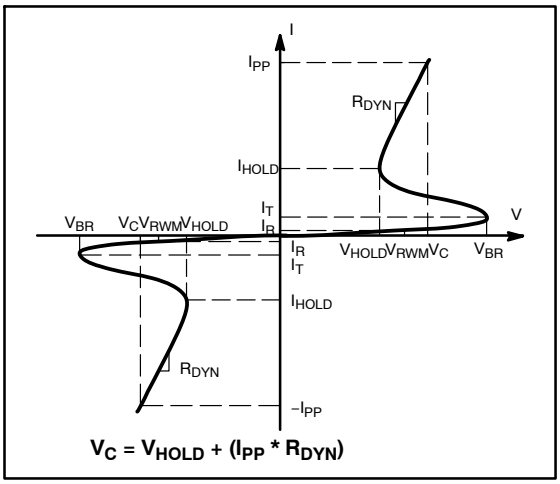

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 5 of this data sheet.

## ELECTRICAL CHARACTERISTICS

($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter |
|---|---|
| $V_{RWM}$ | Working Peak Voltage |
| $I_R$ | Maximum Reverse Leakage Current @ $V_{RWM}$ |
| $V_{BR}$ | Breakdown Voltage @ $I_T$ |
| $I_T$ | Test Current |
| $V_{HOLD}$ | Holding Reverse Voltage |
| $I_{HOLD}$ | Holding Reverse Current |
| $R_{DYN}$ | Dynamic Resistance |
| $I_{PP}$ | Maximum Peak Pulse Current |
| $V_C$ | Clamping Voltage @ $I_{PP}$<br>$V_C = V_{HOLD} + (I_{PP} * R_{DYN})$ |




## ELECTRICAL CHARACTERISTICS ($T_A$ = 25°C unless otherwise specified)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Reverse Working Voltage | $V_{RWM}$ | I/O Pin to GND | | | 3.3 | V |
| Breakdown Voltage | $V_{BR}$ | $I_T$ = 1 mA, I/O Pin to GND | 5.5 | | 8.6 | V |
| Reverse Leakage Current | $I_R$ | $V_{RWM}$ = 3.3 V, I/O Pin to GND | | | 1.0 | μA |
| Reverse Holding Voltage | $V_{HOLD}$ | I/O Pin to GND | | 2.1 | | V |
| Holding Reverse Current | $I_{HOLD}$ | I/O Pin to GND | | 17 | | mA |
| Clamping Voltage TLP (Note 1) | $V_C$ | $I_{PP}$ = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±4 kV Air) | | 6.5 | | V |
| | | $I_{PP}$ = 16 A } IEC 61000−4−2 Level 2 equivalent (±8 kV Contact, ±15 kV Air) | | 10.2 | | |
| Reverse Peak Pulse Current | $I_{PP}$ | IEC61000−4−5 (8/20 μs) | 5.7 | 7.5 | | A |
| Clamping Voltage (8/20 μs) | $V_C$ | $I_{PP}$ = 5.7 A | | 5.6 | 6.5 | V |
| Dynamic Resistance | $R_{DYN}$ | I/O Pin to GND | | 0.46 | | Ω |
| Junction Capacitance | $C_J$ | $V_R$ = 0 V, f = 1 MHz | | 0.15 | 0.3 | pF |



Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
   TLP conditions: $Z_0$ = 50 Ω, $t_p$ = 100 ns, $t_r$ = 1 ns, averaging window; $t_1$ = 70 ns to $t_2$ = 90 ns.

## TYPICAL CHARACTERISTICS

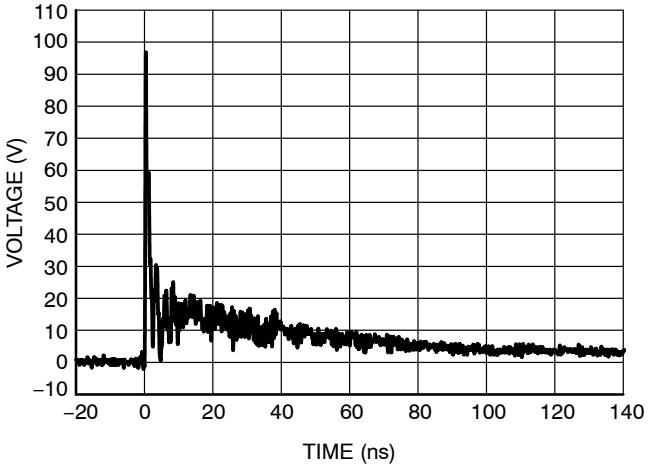



**Figure 1. ESD Clamping Voltage − Pin 1 to Pin 2 8 kV Contact per IEC61000−4−2**

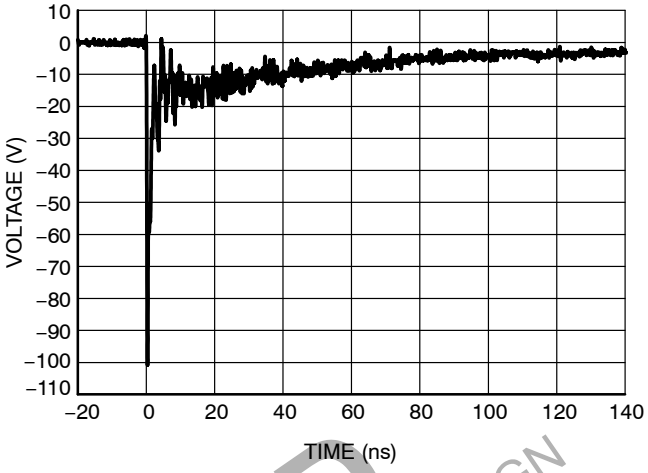



**Figure 2. ESD Clamping Voltage − Pin 2 to Pin 1 8 kV Contact per IEC61000−4−2**

## TYPICAL CHARACTERISTICS

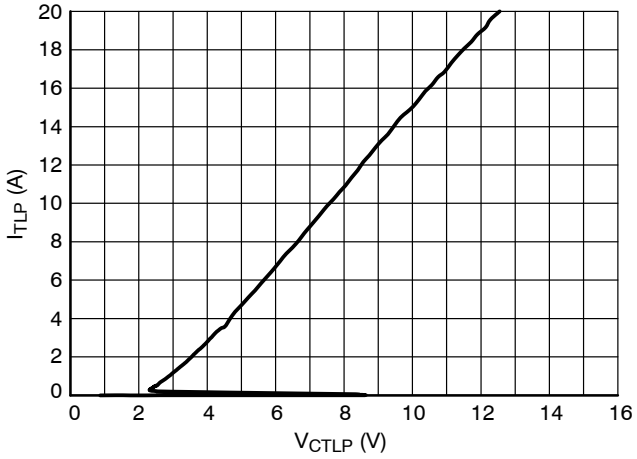



**Figure 3. 100 ns TLP I–V Curve – Pin 1 to Pin 2**

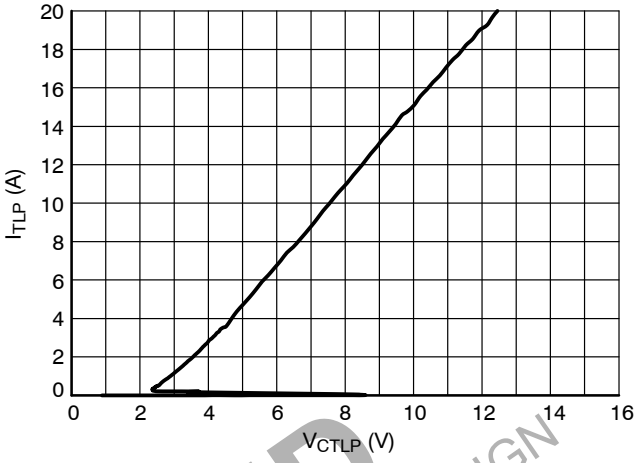



**Figure 4. 100 ns TLP I–V Curve – Pin 2 to Pin 1**

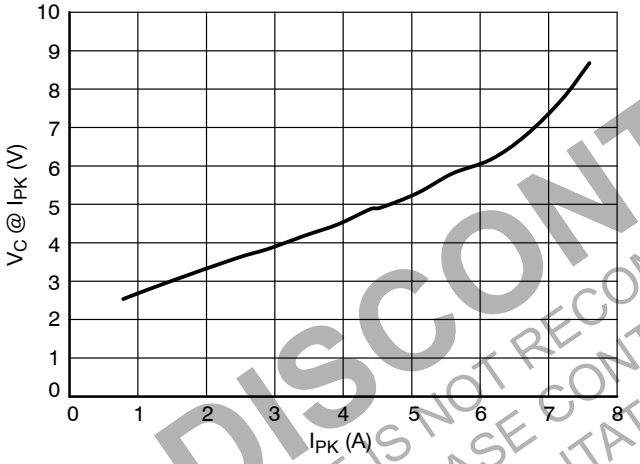



**Figure 5. Clamping Voltage vs. Peak Pulse Current – Pin 1 to Pin 2 ($t_p$ = 8/20 μs)**

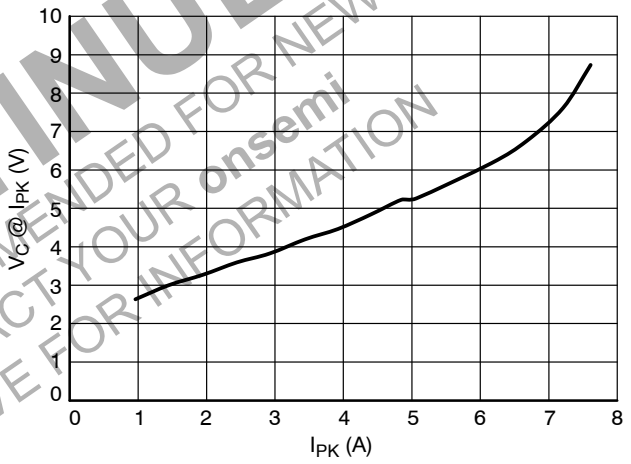



**Figure 6. Clamping Voltage vs. Peak Pulse Current – Pin 2 to Pin 1 ($t_p$ = 8/20 μs)**



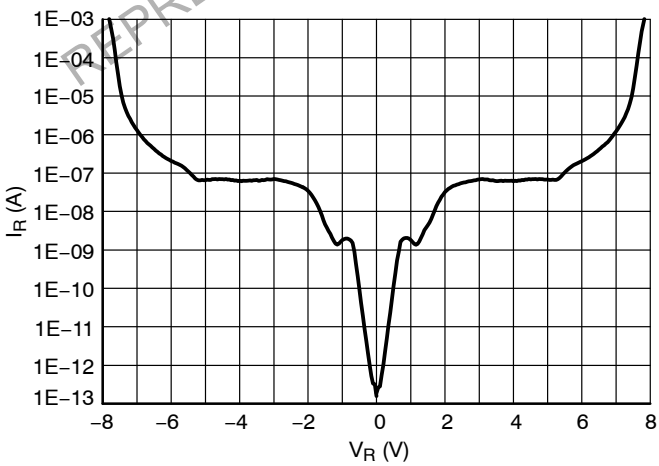



**Figure 7. Reverse Leakage Current**

## TYPICAL CHARACTERISTICS

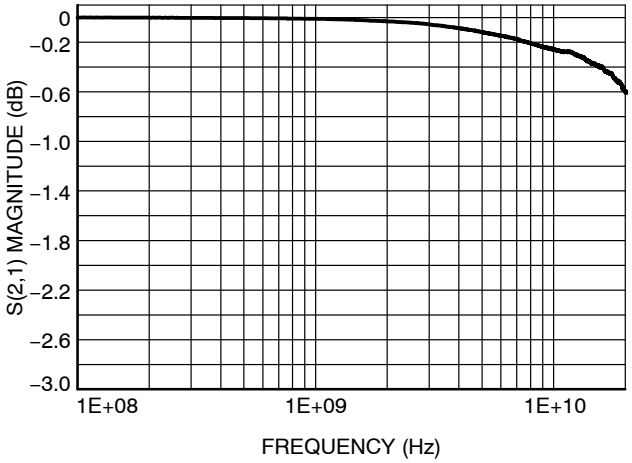



**Figure 8. Insertion Loss**

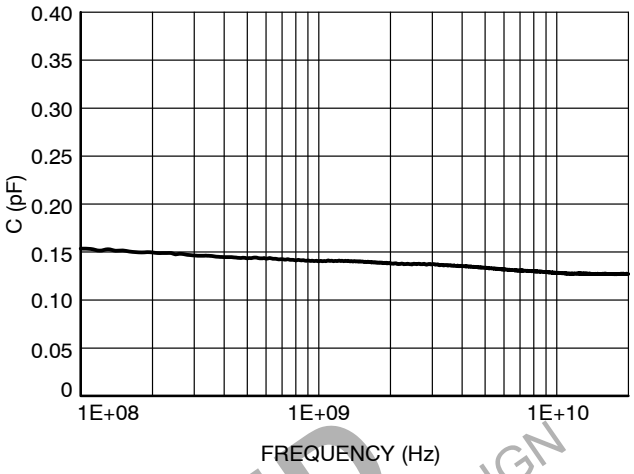



**Figure 9. Capacitance Over Frequency**

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| ESDL1531MX4T5G | X4DFN2<br>(Pb−Free) | 10,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

**IEC 61000−4−2 Spec.**

| Level | Test Voltage (kV) | First Peak Current (A) | Current at 30 ns (A) | Current at 60 ns (A) |
|---|---|---|---|---|
| 1 | 2 | 7.5 | 4 | 2 |
| 2 | 4 | 15 | 8 | 4 |
| 3 | 6 | 22.5 | 12 | 6 |
| 4 | 8 | 30 | 16 | 8 |

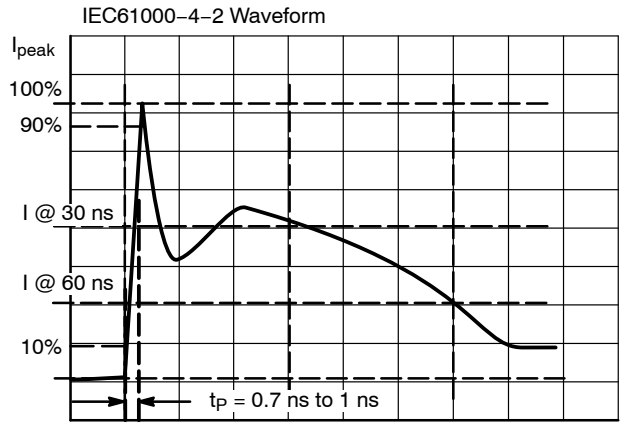



**Figure 10. IEC61000−4−2 Spec**

### Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 11. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 12 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

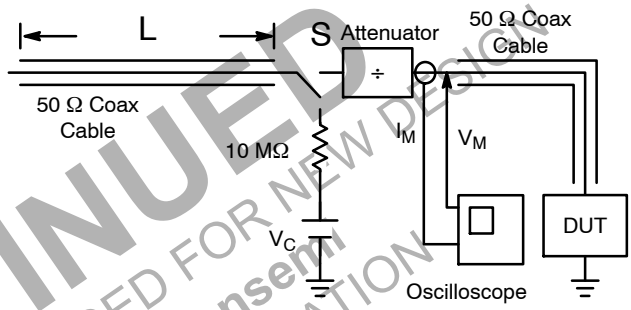



**Figure 11. Simplified Schematic of a Typical TLP System**

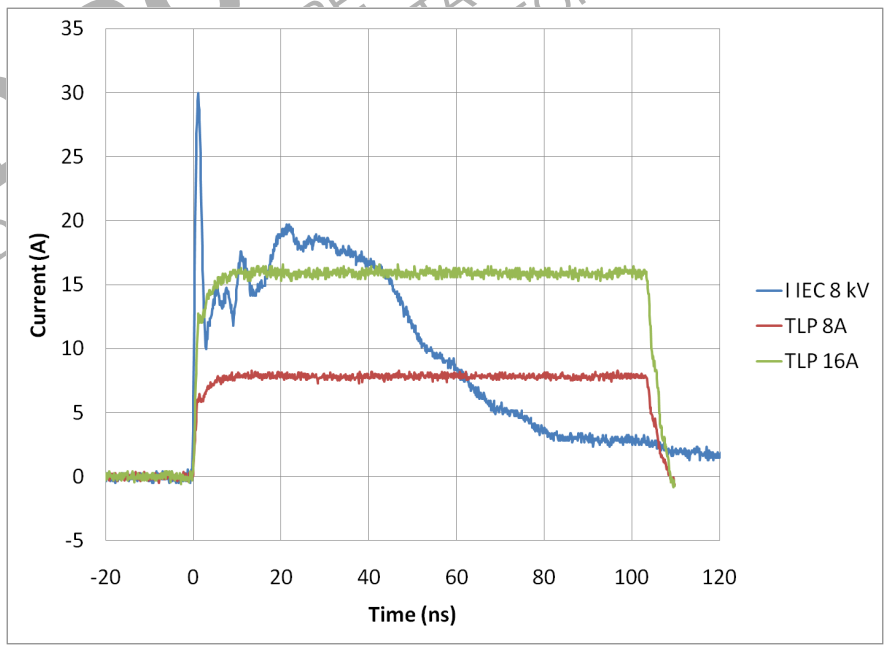
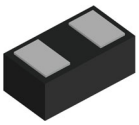
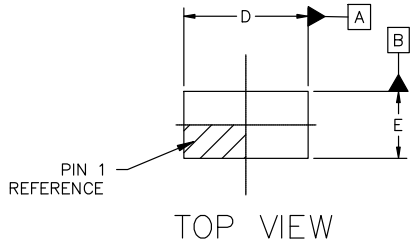



**Figure 12. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms**

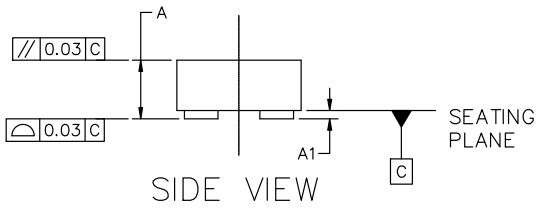


**X4DFN2, 0.44x0.24x0.18, 0.27P**
CASE 718AA
ISSUE B

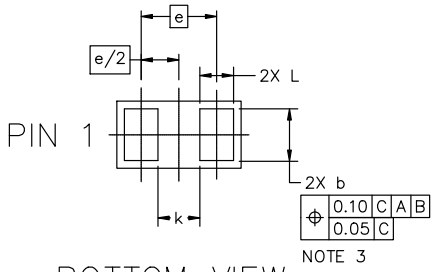
DATE 05 MAR 2025




TOP VIEW



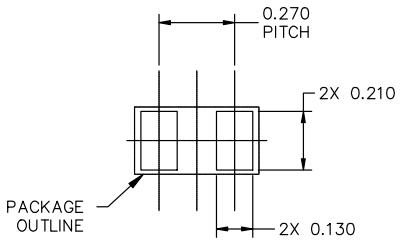

SIDE VIEW




BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. EXPOSED COPPER ALLOWED AS SHOWN.

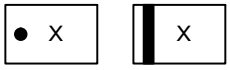
| MILLIMETERS | | | |
|---|---|---|---|
| DIM | MIN | NOM | MAX |
| A | 0.150 | 0.180 | 0.210 |
| A1 | --- | --- | 0.030 |
| b | 0.170 | 0.185 | 0.200 |
| D | 0.415 | 0.445 | 0.475 |
| E | 0.210 | 0.240 | 0.270 |
| e | 0.270 BSC | | |
| k | 0.125 | --- | --- |
| L | 0.105 | 0.120 | 0.135 |




RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

**GENERIC**
**MARKING DIAGRAMS***




X = Specific Device Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
|---|---|---|---|
| **DOCUMENT NUMBER:** | **98AON29067G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. | |
| **DESCRIPTION:** | **X4DFN2, 0.44x0.24x0.18, 0.27P** | | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

**ONLINE SUPPORT**: www.onsemi.com/support
**For additional information, please contact your local Sales Representative at** www.onsemi.com/support/sales