

# ESD Protection Diode

## Micro-Packaged Diodes for ESD Protection



### ESD9B, SZESD9B

The ESD9B Series is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in cellular phones, MP3 players, digital cameras and many other portable applications where board space comes at a premium.

#### Specification Features

- Low Capacitance 15 pF
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.039" x 0.024" (1.0 x 0.60 mm)
- Low Body Height: 0.016" (0.4 mm)
- Stand-off Voltage: 3.3 V, 5 V
- Low Leakage
- Response Time is < 1 ns
- IEC61000-4-2 Level 4 ESD Protection
- AEC-Q101 Qualified and PPAP Capable
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements
- These are Pb-Free Devices

#### Mechanical Characteristics

**CASE:** Void-free, transfer-molded, thermosetting plastic  
Epoxy Meets UL 94 V-0

**LEAD FINISH:** 100% Matte Sn (Tin)

**MOUNTING POSITION:** Any

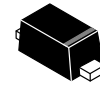
**QUALIFIED MAX REFLOW TEMPERATURE:** 260°C  
Device Meets MSL 1 Requirements

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
IEC 61000-4-2 (ESD) Contact Air		±18 ±18	kV
IEC 61000-4-4 (EFT)		40	A
Total Power Dissipation on FR-5 Board (Note 1) @ T <sub>A</sub> = 25°C	P <sub>D</sub>	300	mW
Thermal Resistance, Junction-to-Ambient	R <sub>θJA</sub>	400	°C/W
Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature - Maximum (10 Second Duration)	T <sub>L</sub>	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. FR-5 = 1.0 x 0.75 x 0.62 in.



SOD-923  
CASE 514AB

#### MARKING DIAGRAM



X = Specific Device Code  
M = Date Code

#### ORDERING INFORMATION

Device	Package	Shipping <sup>†</sup>
ESD9B3.3ST5G	SOD-923 (Pb-Free)	8000 / Tape & Reel
ESD9B5.0ST5G	SOD-923 (Pb-Free)	8000 / Tape & Reel
SZESD9B3.3ST5G	SOD-923 (Pb-Free)	8000 / Tape & Reel
SZESD9B5.0ST5G	SOD-923 (Pb-Free)	8000 / Tape & Reel

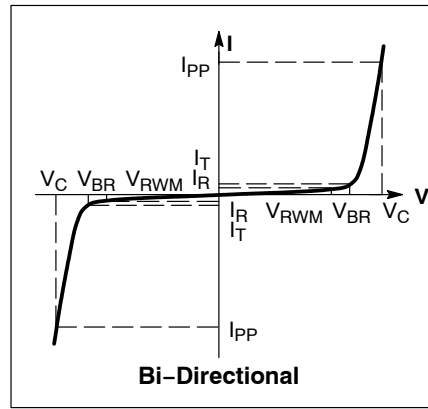
<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# ESD9B, SZESD9B

## ELECTRICAL CHARACTERISTICS

( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Symbol	Parameter
$I_{PP}$	Maximum Reverse Peak Pulse Current
$V_C$	Clamping Voltage @ $I_{PP}$
$V_{RWM}$	Working Peak Reverse Voltage
$I_R$	Maximum Reverse Leakage Current @ $V_{RWM}$
$V_{BR}$	Breakdown Voltage @ $I_T$
$I_T$	Test Current
C	Capacitance @ $V_R = 0\text{ V}$ and $f = 1.0\text{ MHz}$



## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Device	Device Marking	$V_{RWM}$ (V)	$I_R$ (nA) @ $V_{RWM}$	$V_{BR}$ (V) @ $I_T$ (Note 2)		$I_T$ (mA)	C (pF)	$V_C$ (V) Per IEC61000-4-2 (Note 3)	$V_C$ (V) Max Per 8 x 20 $\mu\text{s}$ (Note 4)	
		Max	Max	Min	Max				$I_{PP} = 1\text{ A}$	$I_{PP} = 2\text{ A}$
ESD9B3.3ST5G, SZESD9B3.3ST5G	2*	3.3	100	5.0	7.0	1.0	15	Figures 1 and 2 See Below	10.5	11.5
ESD9B5.0ST5G, SZESD9B5.0ST5G	E	5.0	100	5.8	7.8	1.0	15	Figures 1 and 2 See Below	12.5	15.0

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

\* Rotated  $270^\circ$ .

2.  $V_{BR}$  is measured with a pulse test current  $I_T$  at an ambient temperature of  $25^\circ\text{C}$ .

3. For test procedure see Figures 3 and 4 and Application Note [AND8307/D](#).

4. Surge current waveforms per Figure 5.

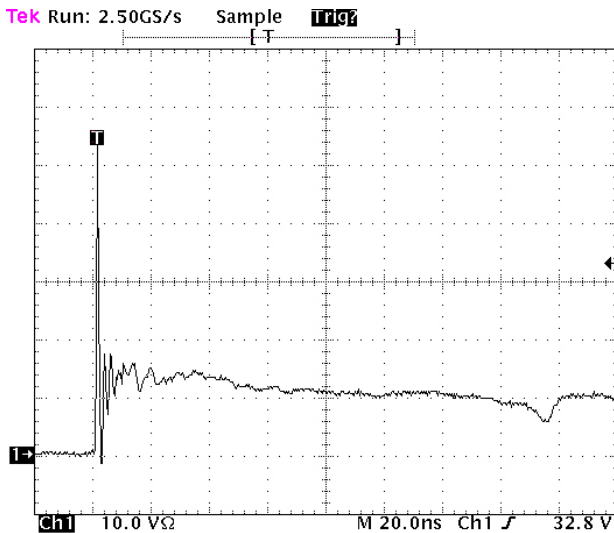


Figure 1. ESD Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000-4-2

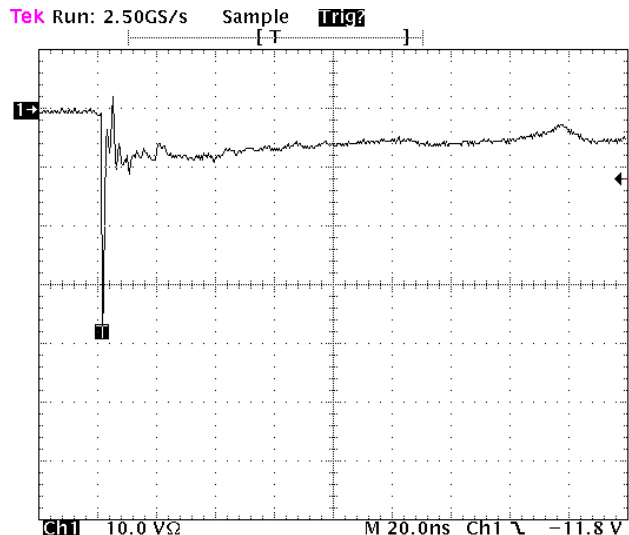


Figure 2. ESD Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000-4-2

# ESD9B, SZESD9B

## IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 3. IEC61000-4-2 Spec

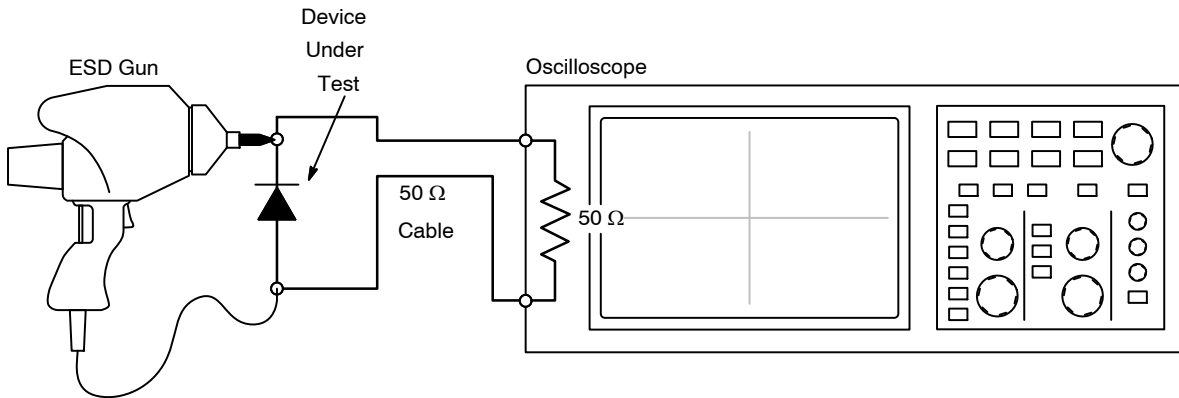


Figure 4. Diagram of ESD Test Setup

The following is taken from Application Note [AND8308/D](#) – Interpretation of Datasheet Parameters for ESD Devices.

### ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. **onsemi** has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how **onsemi** creates these screenshots and how to interpret them please refer to [AND8307/D](#).

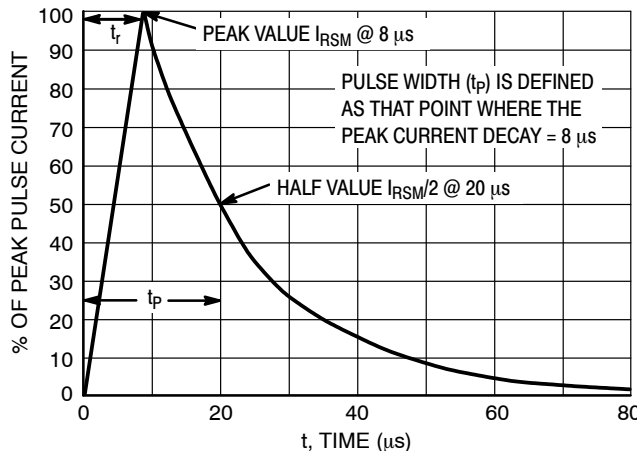
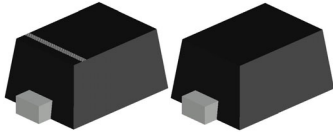
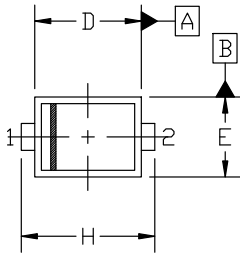


Figure 5. 8 x 20 μs Pulse Waveform



**SOD-923 0.80x0.60x0.37**  
**CASE 514AB**  
**ISSUE E**

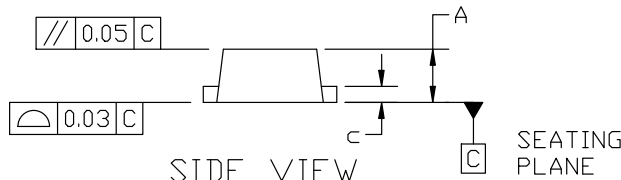
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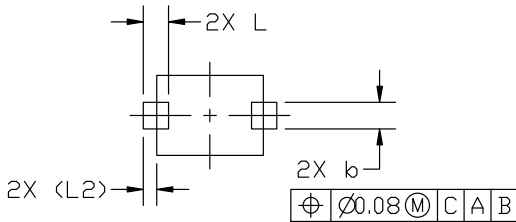
TOP VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSION L WILL NOT EXCEED 0.30mm.

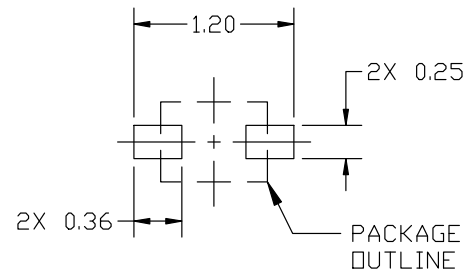


SIDE VIEW



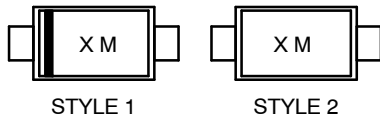
BOTTOM VIEW

MILLIMETERS			
DIM	MIN.	NOM.	MAX.
A	0.34	0.37	0.40
b	0.15	0.20	0.25
c	0.07	0.12	0.17
D	0.75	0.80	0.85
E	0.55	0.60	0.65
H	0.95	1.00	1.05
L	0.19 REF		
L2	0.05	0.10	0.15



RECOMMENDED MOUNTING FOOTPRINT

**GENERIC MARKING DIAGRAM\***



X = Specific Device Code  
M = Date Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

STYLE 1: PIN 1. CATHODE (POLARITY BAND)  
2. ANODE

STYLE 2: NO POLARITY

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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