ESD7102, SZESD7102

ESD Protection Diodes

Low Capacitance ESD Protection Diodes for High Speed Data Line

The ESD7102 transient voltage suppressor is designed to protect high speed data lines from ESD. Ultra−low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The small form factor, flow−through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance between high speed differential lines such as USB 3.0 and HDMI.

Features

- Low Capacitance (0.3 pF Typical, I/O to GND)
- Short to Battery Survivability
- Protection for the Following IEC Standards:
  IEC 61000−4−2 Level 4 (ESD)
- Low ESD Clamping Voltage (34 V Typical, +8 A TLP, I/O to GND)
- SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q101 Qualified and PPAP Capable
- These Devices are Pb−Free and are RoHS Compliant

Typical Applications

- USB2.0/3.0
- LVDS
- HDMI
- High Speed Differential Pairs

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T_J	−55 to +150	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C
IEC 61000−4−2 Contact IEC 61000−4−2 Air ISO 10605 Contact (330 pF / 330 Ω) ISO 10605 Contact (330 pF / 2 kΩ) ISO 10605 Contact (150 pF / 2 kΩ)	ESD	±8 ±15 ±8 ±20 ±27	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ON Semiconductor®

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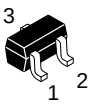
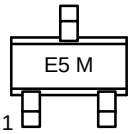
MARKING DIAGRAM

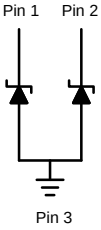


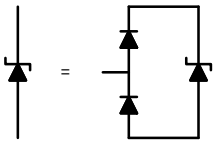
SC−75
CASE 463



E5 = Specific Device Code
M = Date Code

PIN CONFIGURATION AND SCHEMATIC





ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			16	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	16.5			V
Reverse Leakage Current	I_R	V_{RWM} = 5 V, I/O Pin to GND			1	μA
Clamping Voltage (Note 1)	V_C	IEC61000−4−2, ±8 kV Contact	See Figures 1 and 2			
Clamping Voltage TLP (Note 2)	V_C	I_{PP} = 8 A I_{PP} = 16 A I_{PP} = −8 A I_{PP} = −16 A		34 55 −5.3 −10		V
Dynamic Resistance (Note 2)	I_R	TLP Pulse		1.5		Ω
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz between I/O Pins V_R = 0 V, f = 1 MHz between I/O Pins and GND		0.2 0.3	0.4 0.5	pF
Junction Capacitance Match	ΔC_J	V_R = 0 V, f = 1 MHz between I/O1 to GND and I/O 2 to GND		5	10	%
Insertion Loss		f = 1 GHz f = 3 GHz		0.1 0.2		dB
3dB Bandwidth	f_{BW}	R_L = 50 Ω		5		GHz

1. For test procedure see Figures 5 and 6 and application note AND8307/D.
2. ANSI/ESD STM5.5.1 − Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model. TLP conditions: Z_0 = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t_1 = 30 ns to t_2 = 60 ns.

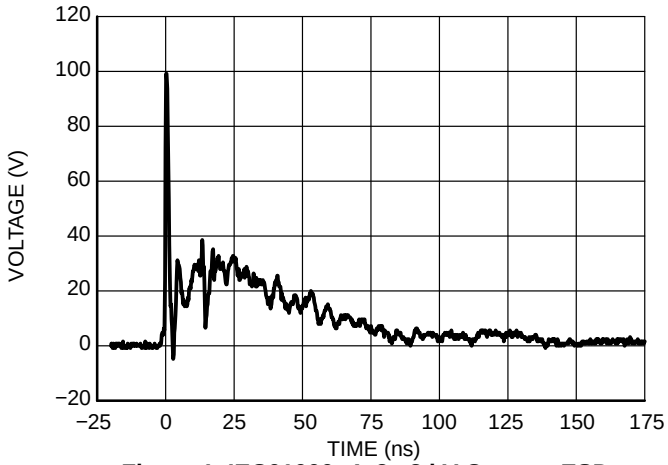


Figure 1. IEC61000−4−2 +8 kV Contact ESD Clamping Voltage

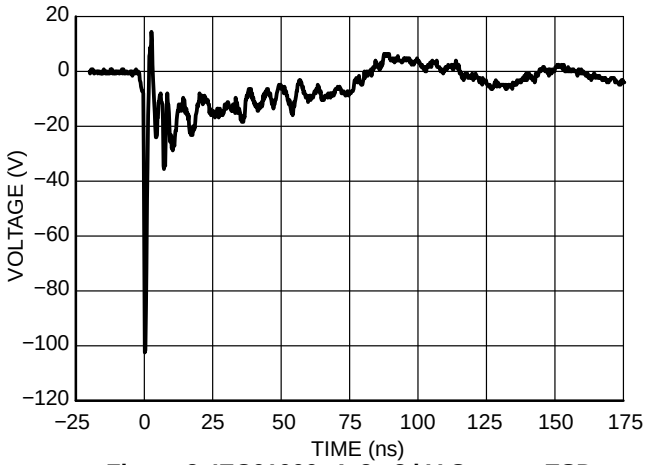


Figure 2. IEC61000−4−2 −8 kV Contact ESD Clamping Voltage

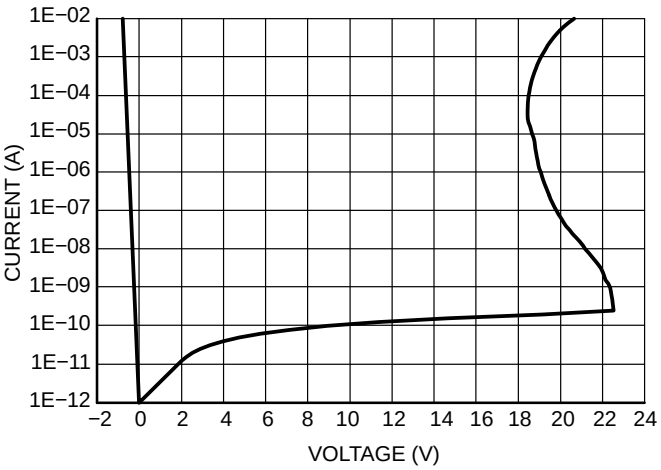


Figure 3. Typical IV Characteristic Curve

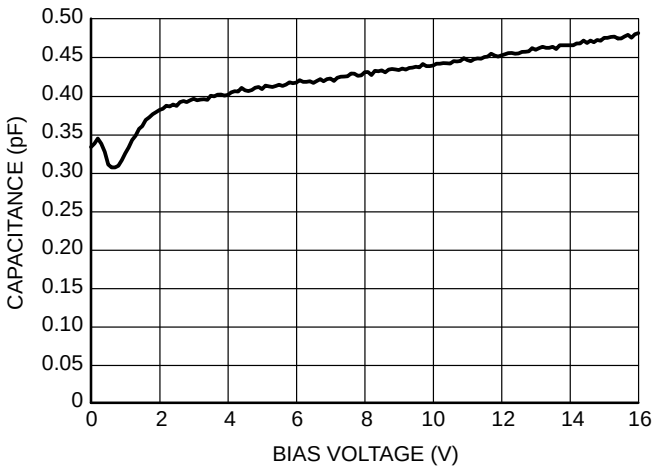


Figure 4. Typical CV Characteristic Curve

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

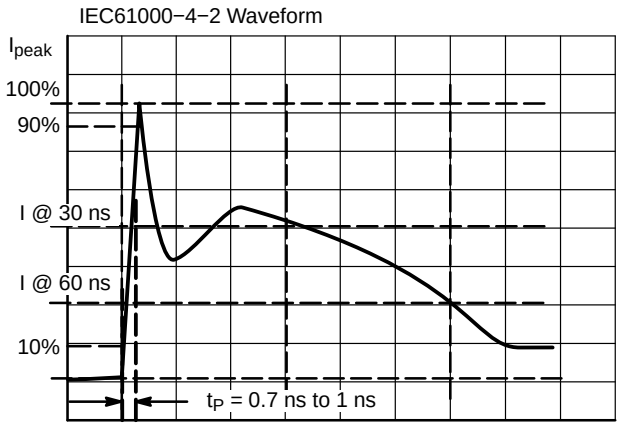


Figure 5. IEC61000−4−2 Spec

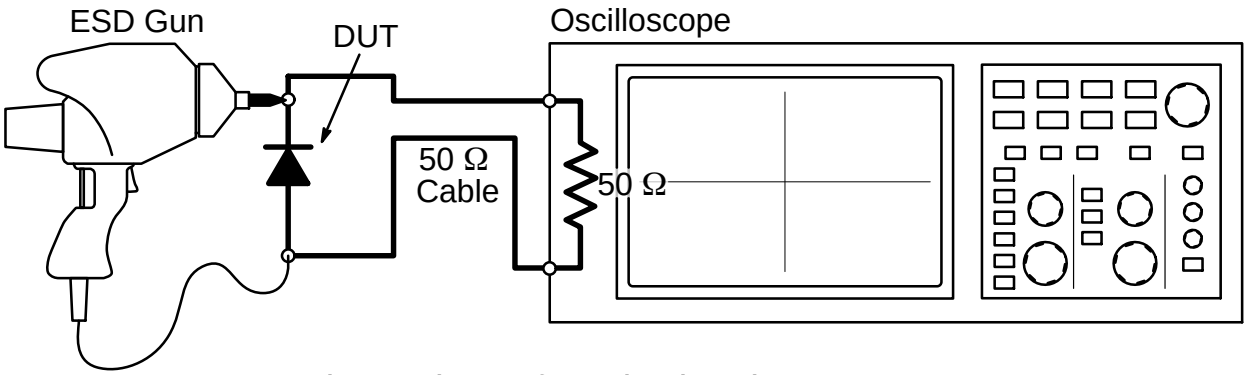


Figure 6. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

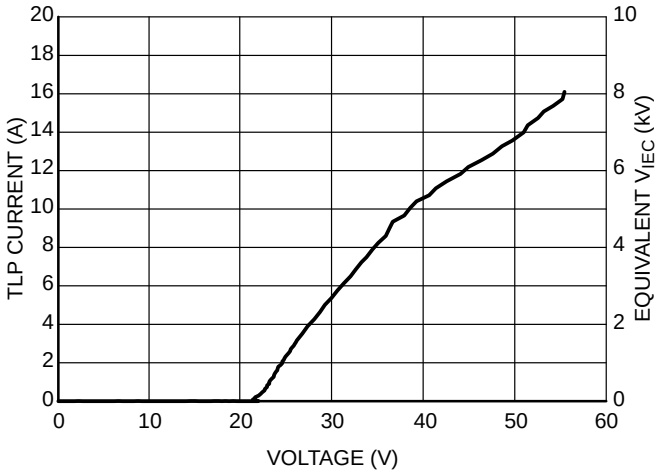


Figure 7. Positive TLP IV Curve

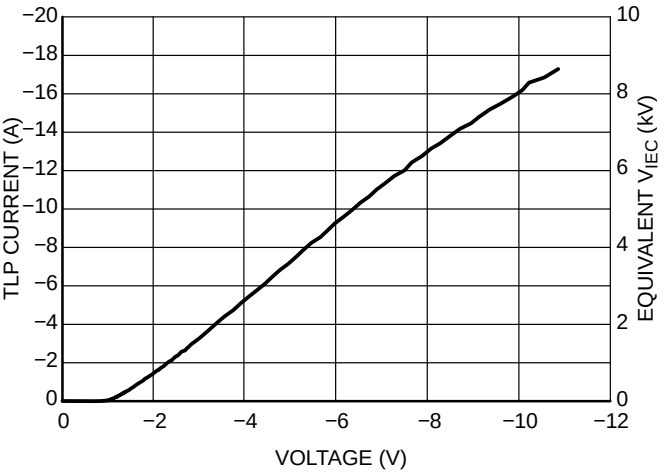


Figure 8. Negative TLP IV Curve

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

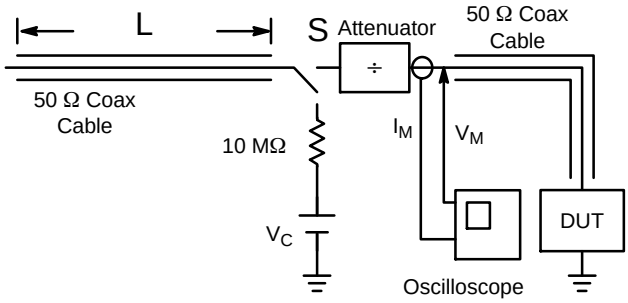


Figure 9. Simplified Schematic of a Typical TLP System

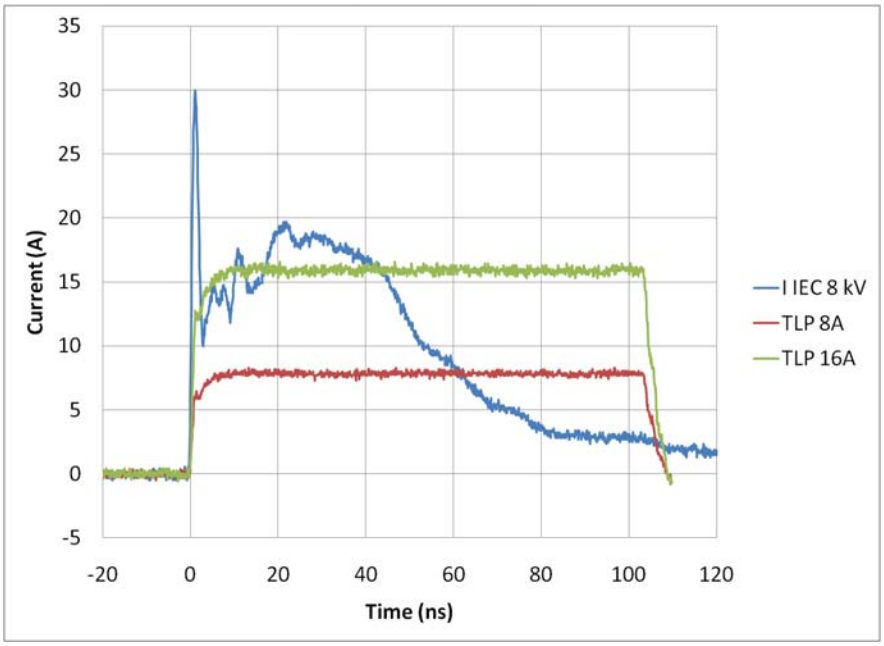


Figure 10. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

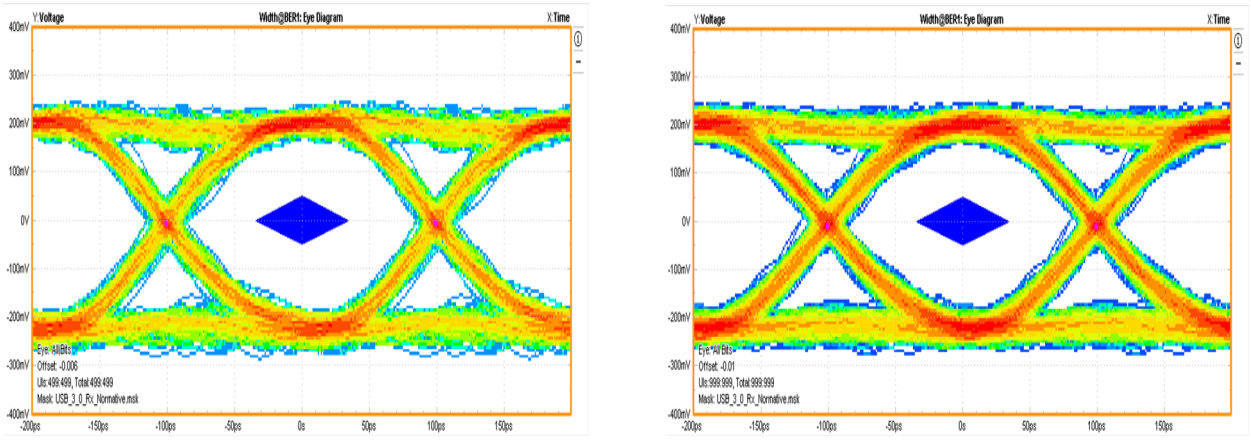


Figure 11. USB3.0 Eye Diagram with and without ESD7102 at 5 Gb/s

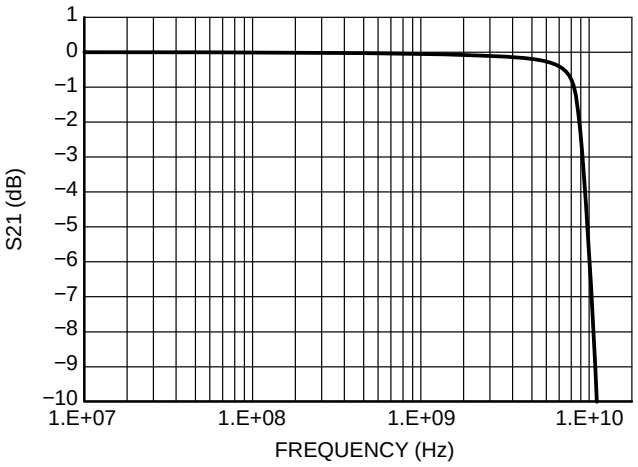


Figure 12. Typical Insertion Loss

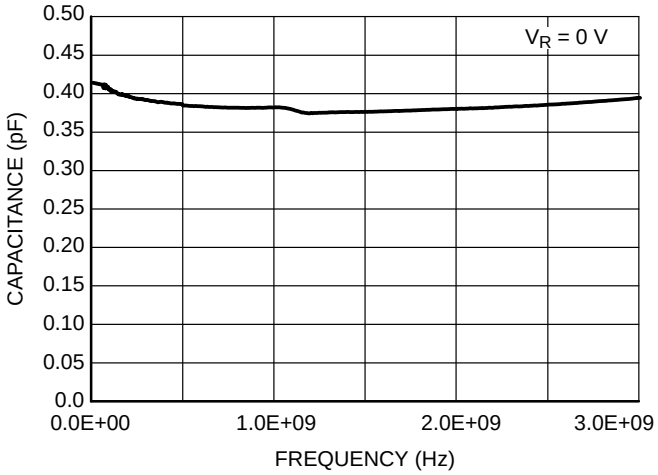


Figure 13. Typical Capacitance over Frequency

ORDERING INFORMATION

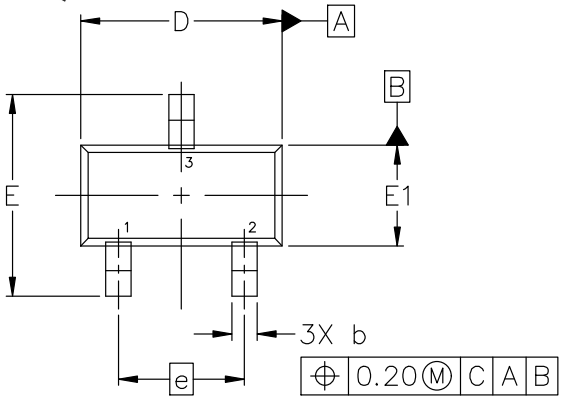
Device	Package	Shipping†
ESD7102BT1G	SC−75 (Pb−Free)	3000 / Tape & Reel
SZESD7102BT1G*	SC−75 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

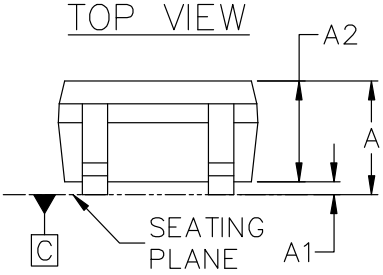
*SZ Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC−Q100 Qualified and PPAP Capable.

SC75−3 1.60x0.80x0.80, 1.00P
CASE 463
ISSUE H

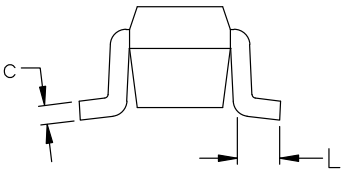
DATE 01 FEB 2024



TOP VIEW



SIDE VIEW



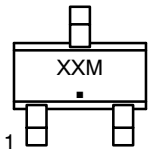
END VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5−2018.
2. ALL DIMENSION ARE IN MILLIMETERS.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.80	0.90
A1	0.00	0.05	0.10
A2		0.80 REF.	
b	0.15	0.20	0.30
c	0.10	0.15	0.25
D	1.55	1.60	1.65
E	1.50	1.60	1.70
E1	0.70	0.80	0.90
e		1.00 BSC	
L	0.10	0.15	0.20

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

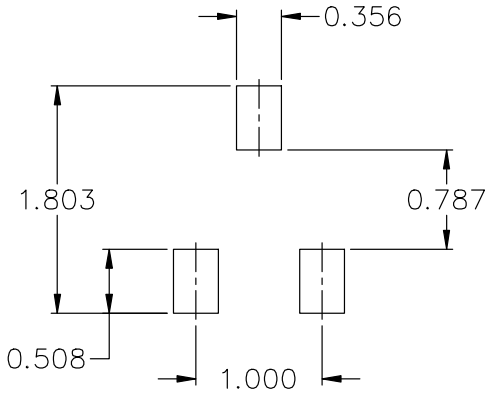
STYLE 1:
PIN 1. BASE
2. EMITTER
3. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. N/C
3. CATHODE

STYLE 3:
PIN 1. ANODE
2. ANODE
3. CATHODE

STYLE 4:
PIN 1. CATHODE
2. CATHODE
3. ANODE

STYLE 5:
PIN 1. GATE
2. SOURCE
3. DRAIN



RECOMMENDED MOUNTING FOOTPRINT*

* FOR ADDITIONAL INFORMATION ON OUR Pb−FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	**98ASB15184C**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red.	
DESCRIPTION:	**SC75−3 1.60x0.80x0.80, 1.00P**		**PAGE 1 OF 1**

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