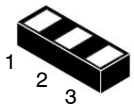
EMI Filter with ESD Protection

EMI1051



DSN3 (0301)
CASE 152AB

The EMI1051 is an R−C EMI filter array with bidirectional ESD protection that integrates a Pi−filter (C−R−C) to suppress EMI/RFI Noise. EMI1051 includes ESD protection diodes on the input and output pins, and provides a very high level of protection for sensitive electronic components against possible electrostatic discharge (ESD). The ESD diodes connected to the filter ports safely dissipate ESD strikes of ±30 kV.

Features

- Small Form Factor
- ±30 kV ESD Protection (IEC 61000−4−2, Contact Discharge)
- ±30 kV ESD Protection (IEC 61000−4−2, Air Discharge)
- Greater than 30 dB of Attenuation in the 600 MHz − 1.55 GHz Range
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

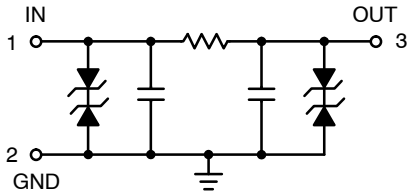
Applications

- Mobile Phones
- Tablets
- Laptops

MARKING DIAGRAM

A = Specific Device Code
M = Month Code

BLOCK DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
ESD Discharge: IEC 61000−4−2, Contact Discharge IEC 61000−4−2, Air Discharge	ESD	 ±30 ±30	 kV kV
Operating Junction Temperature Range	T_J	−40 to +125	°C
Storage Temperature Range	T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Seconds)	T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V_{RWM}	I/O Pin to GND			5.5	V
Breakdown Voltage	V_{BR}	I_T = 1 mA, I/O Pin to GND	6.1	6.8	8.0	V
Reverse Leakage Current	I_R	V_{RWM} = 5.5 V, I/O Pin to GND		0.01	0.1	μA
Clamping Voltage TLP	V_C	I_{PP} = 8 A } IEC 61000−4−2 Level 2 equivalent (±4 kV Contact, ±8 kV Air)		7.7	8.8	V
		I_{PP} = 16 A } IEC 61000−4−2 Level 2 equivalent (±8 kV Contact, ±16 kV Air)		8.5	10	
Reverse Peak Pulse Current	I_{PP}	IEC61000−4−5 (8x20 μs)	18	22.5		A
Clamping Voltage	V_C	I_{PP} = 10 A, (8/20 μs pulse) I_{PP} = 18 A		8.5 10.5	10	V
Dynamic Resistance	R_{DYN}	100 ns TLP Pulse		0.1		Ω
Series Channel Resistance	R_{CH}	Pins A1 to A3	80	100	120	Ω
Cut−off Frequency	F_C	50 Ω Termination		65		MHz
Stop Band Attenuation	F_{atten}	600 MHz	30	36		dB
		1 GHz	30	42		
		1.55 GHz	30	44		
Second Harmonic Floor	H_{F2}	f = 710 MHz, 900 MHz, 1.9 GHz, 2.5 GHz @ 5 dBm	−85			dB
		f = 710 MHz, 900 MHz, 1.9 GHz, 2.5 GHz @ 25 dBm	−40			
Third Harmonic Floor	H_{F3}	f = 710 MHz, 900 MHz, 1.9 GHz, 2.5 GHz @ 10 dBm	−110			dB
		f = 710 MHz, 900 MHz, 1.9 GHz, 2.5 GHz @ 25 dBm	−60			
Junction Capacitance	C_J	V_R = 0 V, f = 1 MHz	64	80		pF
Insertion Loss	I_L	f = 1 MHz		−6		dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

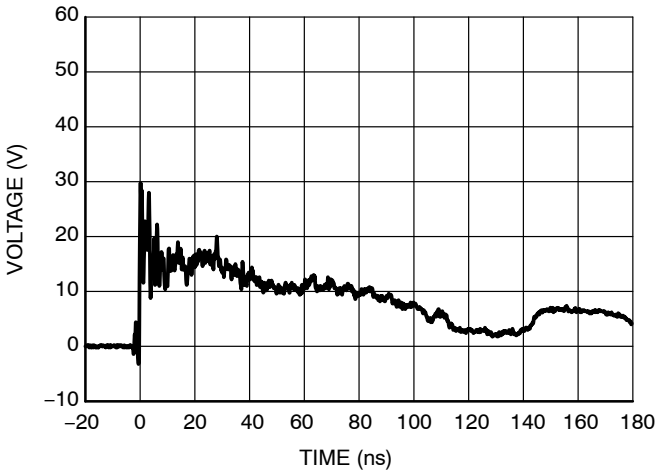


Figure 1. ESD Clamping Voltage – I/O to GND, +8 kV Contact per IEC61000−4−2

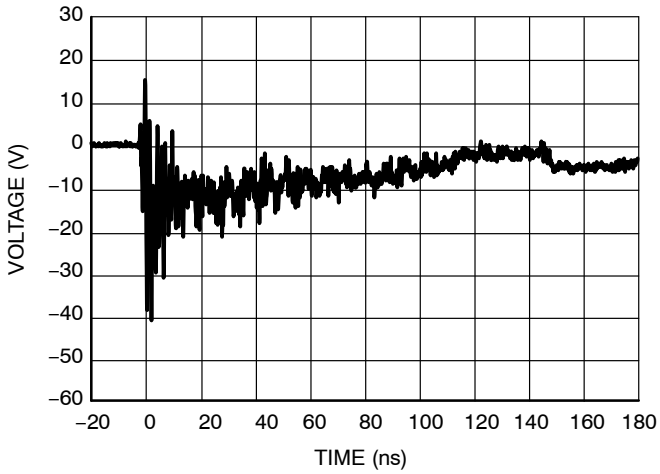


Figure 2. ESD Clamping Voltage – GND to I/O, −8 kV Contact per IEC61000−4−2

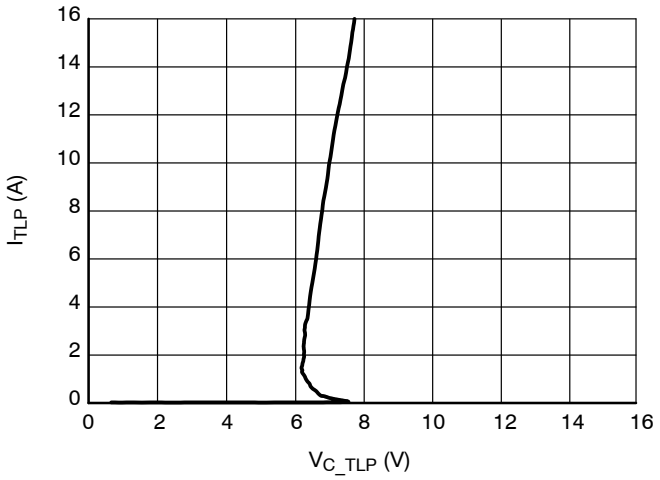


Figure 3. 100 ns TLP I−V Curve – I/O to GND

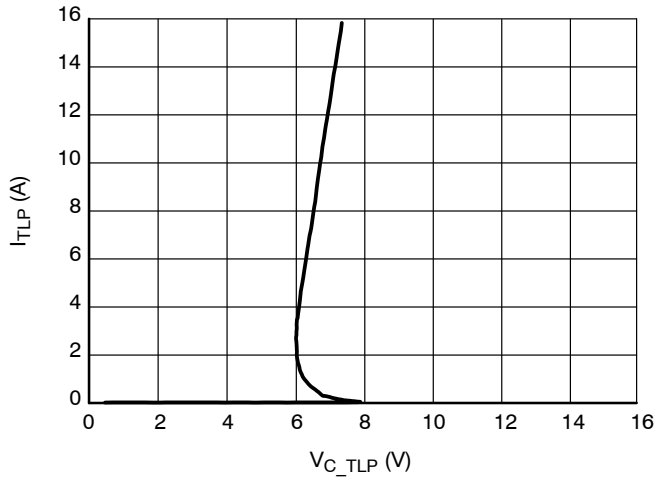


Figure 4. 100 ns TLP I−V Curve – GND to I/O

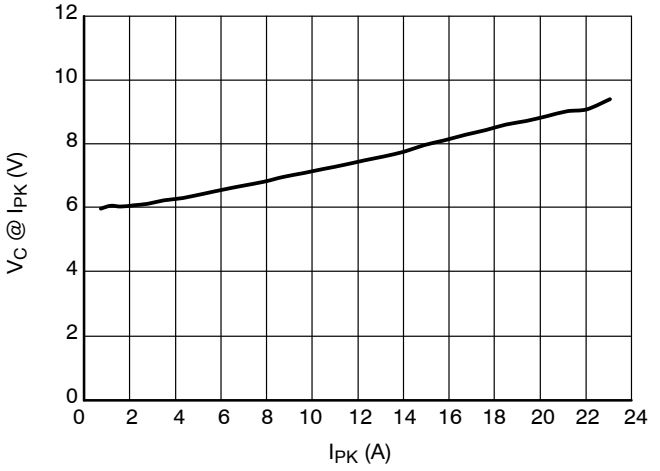


Figure 5. Clamping Voltage vs. Peak Pulse Current – I/O to Gnd (t_p = 8/20 μs)

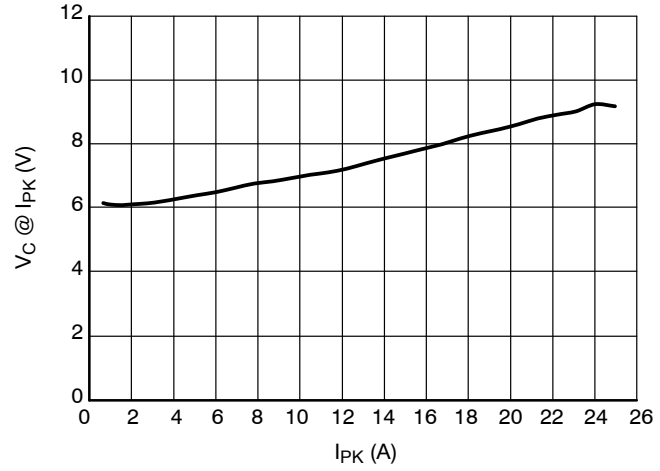


Figure 6. Clamping Voltage vs. Peak Pulse Current – Gnd to I/O (t_p = 8/20 μs)

TYPICAL CHARACTERISTICS

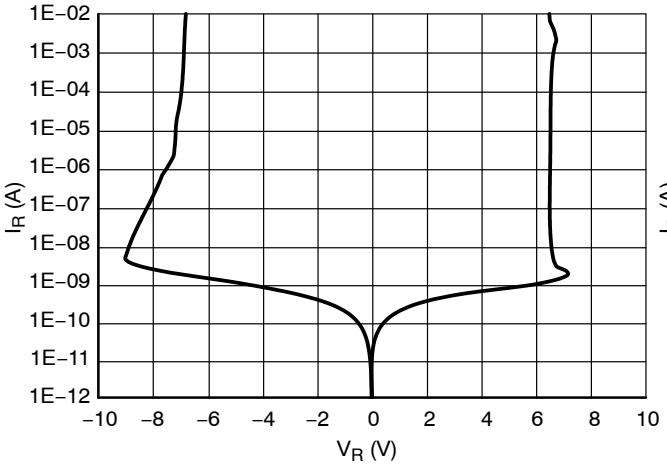


Figure 7. Breakdown Voltage − I/O to GND

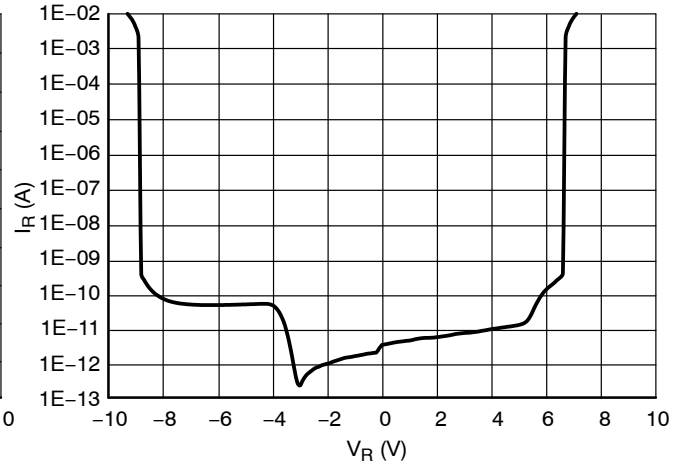


Figure 8. Reverse Leakage Current − I/O to GND

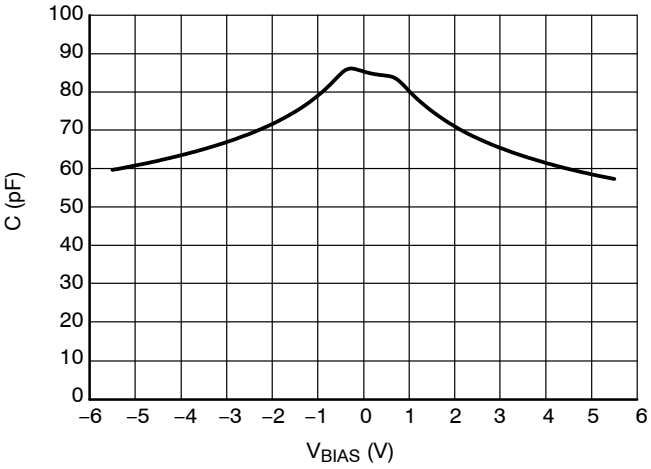


Figure 9. Line Capacitance, f = 1 MHz

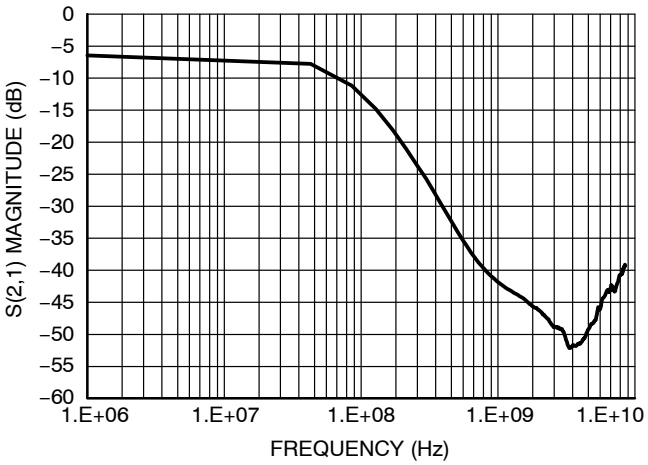


Figure 10. Attenuation

ESD VOLTAGE CLAMPING

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to On Semiconductor Application Notes AND8307/D and AND8308/D.

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

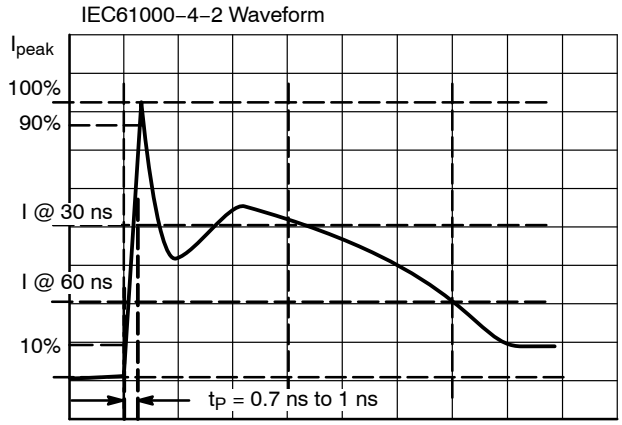


Figure 11. IEC61000−4−2 Spec

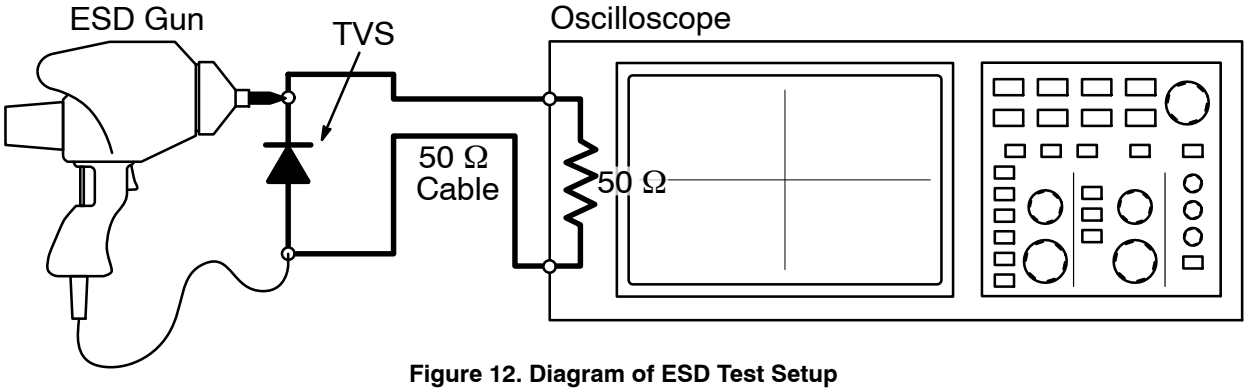


Figure 12. Diagram of ESD Test Setup

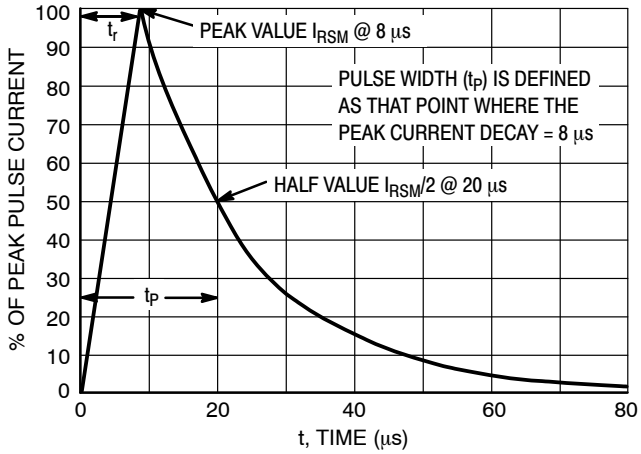


Figure 13. 8 x 20 μs Pulse Waveform

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I−V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 14. TLP I−V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 15 where an 8 kV IEC 61000−4−2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I−V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

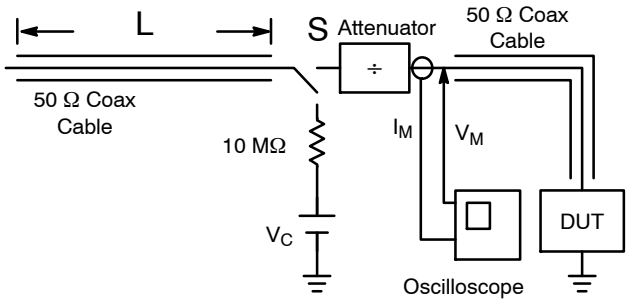


Figure 14. Simplified Schematic of a Typical TLP System

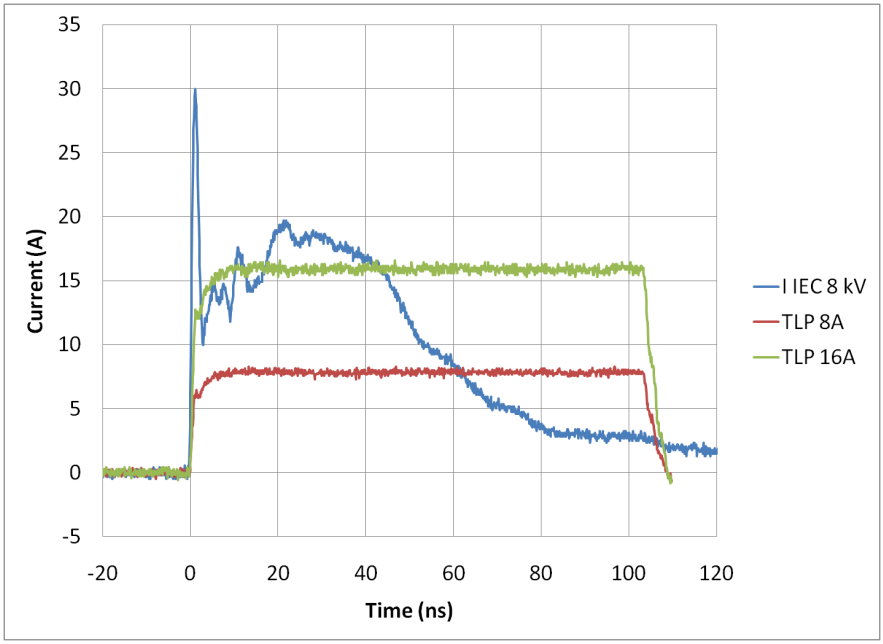


Figure 15. Comparison Between 8 kV IEC 61000−4−2 and 8 A and 16 A TLP Waveforms

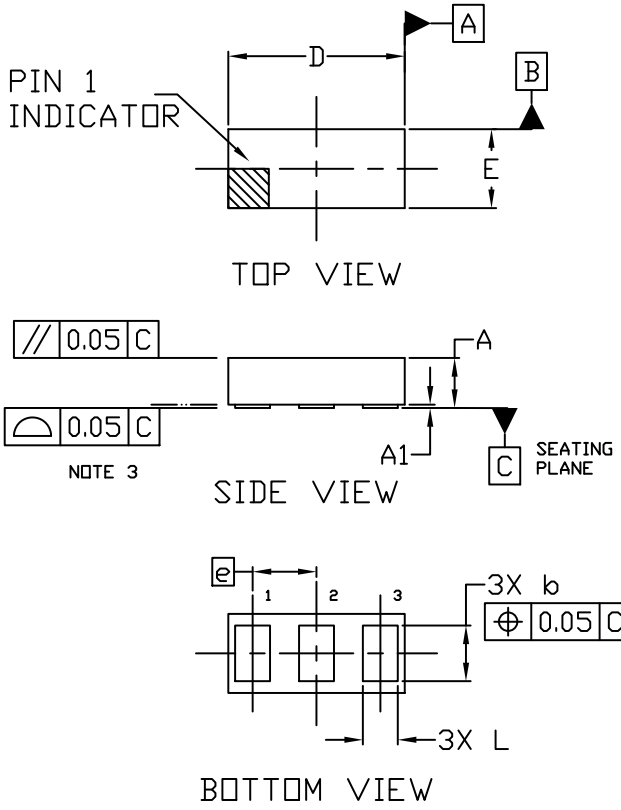
ORDERING INFORMATION

Device	Package	Shipping†
EMI1051FCT5G	DSN3 (Pb−Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS – EMI1051 (01005)

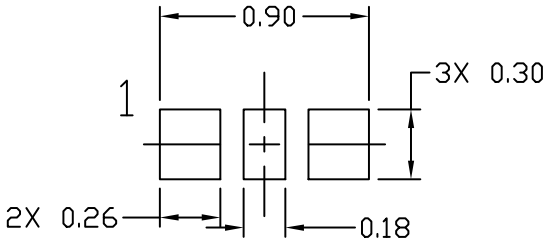
DSN3 0.76x0.34 (0301)
CASE 152BA
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO ALL PADS

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.17	0.20	0.23
A1	0.00	---	0.03
b	0.22	0.24	0.26
D	0.73	0.76	0.79
E	0.31	0.34	0.37
e	0.275 BSC		
L	0.13	0.15	0.17



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales