

# EMA6DXV5T1, EMA6DXV5T5

Preferred Devices

## Dual Common Emitter Bias Resistor Transistor

### PNP Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SOT-553 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Moisture Sensitivity Level: 1
- ESD Rating – Human Body Model: Class 1  
– Machine Model: Class B
- Available in 7 Inch Tape and Reel
- Lead-Free Solder Plating

#### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Rating                    | Symbol    | Value | Unit |
|---------------------------|-----------|-------|------|
| Collector-Base Voltage    | $V_{CBO}$ | 50    | Vdc  |
| Collector-Emitter Voltage | $V_{CEO}$ | 50    | Vdc  |
| Collector Current         | $I_C$     | 100   | mAdc |

#### THERMAL CHARACTERISTICS

| Characteristic  | Symbol          | Max  | Unit                     |
|---|-----------------|--|--------------------------|
| Total Device Dissipation<br>$T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$           | 230 (Note 1)<br>338 (Note 2)<br>1.8 (Note 1)<br>2.7 (Note 2) | mW<br>$^\circ\text{C/W}$ |
| Thermal Resistance –<br>Junction-to-Ambient   | $R_{\theta JA}$ | 540 (Note 1)<br>370 (Note 2)                                 | $^\circ\text{C/W}$       |
| Thermal Resistance –<br>Junction-to-Lead  | $R_{\theta JL}$ | 264 (Note 1)<br>287 (Note 2)                                 | $^\circ\text{C/W}$       |
| Junction and Storage<br>Temperature Range   | $T_J, T_{stg}$  | -55 to +150  | $^\circ\text{C}$         |

#### DEVICE MARKING AND RESISTOR VALUES

| Device     | Marking | R1 (K) | R2 (K)   |
|------------|---------|--------|----------|
| EMA6DXV5T1 | UD      | 47     | $\infty$ |

1. FR-4 @ Minimum Pad
2. FR-4 @ 1.0 x 1.0 inch Pad

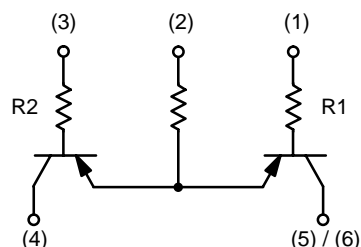


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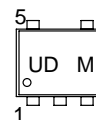
### PNP SILICON BIAS RESISTOR TRANSISTOR

EMA6 / UMA6N



1  
SOT-553  
CASE 463B

#### MARKING DIAGRAM



UD= Specific Device Code  
M = Date Code

#### ORDERING INFORMATION

| Device     | Package | Shipping                       |
|------------|---------|--------------------------------|
| EMA6DXV5T1 | SOT-553 | 4 mm pitch<br>4000/Tape & Reel |
| EMA6DXV5T5 | SOT-553 | 2 mm pitch<br>8000/Tape & Reel |

Preferred devices are recommended choices for future use and best overall value.

# EMA6DXV5T1, EMA6DXV5T5

## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic   | Symbol        | Min | Typ | Max | Unit |
|--|---------------|-----|-----|-----|------|
| <b>OFF CHARACTERISTICS</b>   |               |     |     |     |      |
| Collector–Base Cutoff Current<br>( $V_{CB} = 50\text{ V}, I_E = 0$ )               | $I_{CBO}$     | –   | –   | 100 | nAdc |
| Collector–Emitter Cutoff Current<br>( $V_{CE} = 50\text{ V}, I_B = 0$ )            | $I_{CEO}$     | –   | –   | 500 | nAdc |
| Emitter–Base Cutoff Current<br>( $V_{EB} = 6.0\text{ V}, I_C = 0$ )                | $I_{EBO}$     | –   | –   | 0.2 | mAdc |
| Collector–Base Breakdown Voltage<br>( $I_C = 10\ \mu\text{A}, I_E = 0$ )           | $V_{(BR)CBO}$ | 50  | –   | –   | Vdc  |
| Collector–Emitter Breakdown Voltage (Note 3)<br>( $I_C = 2.0\text{ mA}, I_B = 0$ ) | $V_{(BR)CEO}$ | 50  | –   | –   | Vdc  |

## ON CHARACTERISTICS (Note 3)

|  |               |      |     |      |            |
|--|---------------|------|-----|------|------------|
| DC Current Gain<br>( $V_{CE} = 10\text{ V}, I_C = 5.0\text{ mA}$ )                                 | $h_{FE}$      | 160  | 350 | –    |            |
| Collector–Emitter Saturation Voltage<br>( $I_C = 10\text{ mA}, I_B = 1.0\text{ mA}$ )              | $V_{CE(sat)}$ | –    | –   | 0.25 | Vdc        |
| Output Voltage (on)<br>( $V_{CC} = 5.0\text{ V}, V_B = 3.5\text{ V}, R_L = 1.0\text{ k}\Omega$ )   | $V_{OL}$      | –    | –   | 0.2  | Vdc        |
| Output Voltage (off)<br>( $V_{CC} = 5.0\text{ V}, V_B = 0.25\text{ V}, R_L = 1.0\text{ k}\Omega$ ) | $V_{OH}$      | 4.9  | –   | –    | Vdc        |
| Input Resistor   | R1            | 32.9 | 47  | 61.1 | k $\Omega$ |

3. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%

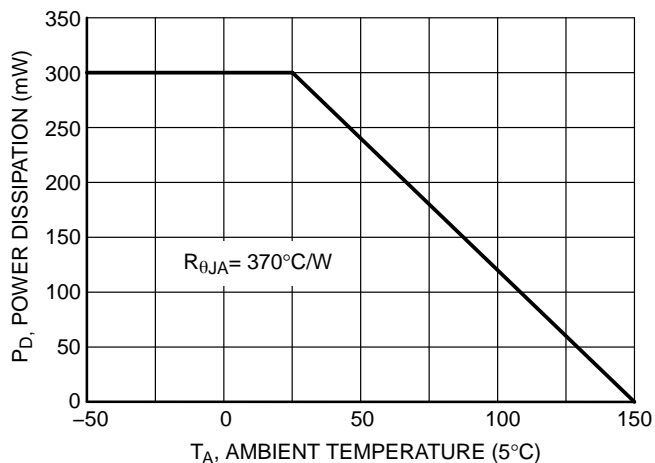


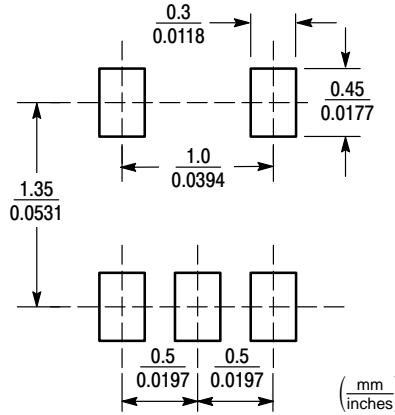
Figure 1. Derating Curve

**INFORMATION FOR USING THE SOT-553 SURFACE MOUNT PACKAGE**

**MINIMUM RECOMMENDED FOOTPRINT FOR SURFACE MOUNTED APPLICATIONS**

Surface mount board layout is a critical portion of the total design. The footprint for the semiconductor packages must be the correct size to insure proper solder connection

interface between the board and the package. With the correct pad geometry, the packages will self align when subjected to a solder reflow process.



**SOT-553**

**SOT-553 POWER DISSIPATION**

The power dissipation of the SOT-553 is a function of the pad size. This can vary from the minimum pad size for soldering to a pad size given for maximum power dissipation. Power dissipation for a surface mount device is determined by  $T_{J(max)}$ , the maximum rated junction temperature of the die,  $R_{\theta JA}$ , the thermal resistance from the device junction to ambient, and the operating temperature,  $T_A$ . Using the values provided on the data sheet for the SOT-553 package,  $P_D$  can be calculated as follows:

$$P_D = \frac{T_{J(max)} - T_A}{R_{\theta JA}}$$

The values for the equation are found in the maximum ratings table on the data sheet. Substituting these values into the equation for an ambient temperature  $T_A$  of 25°C, one can calculate the power dissipation of the device which in this case is 150 milliwatts.

$$P_D = \frac{150^\circ\text{C} - 25^\circ\text{C}}{833^\circ\text{C/W}} = 150 \text{ milliwatts}$$

The 833°C/W for the SOT-553 package assumes the use of the recommended footprint on a glass epoxy printed circuit board to achieve a power dissipation of 150 milliwatts. There are other alternatives to achieving higher power dissipation from the SOT-553 package. Another alternative would be to use a ceramic substrate or an aluminum core board such as Thermal Clad®. Using a board material such as Thermal Clad, an aluminum core board, the power dissipation can be doubled using the same footprint.

**SOLDERING PRECAUTIONS**

The melting temperature of solder is higher than the rated temperature of the device. When the entire device is heated to a high temperature, failure to complete soldering within a short time could result in device failure. Therefore, the following items should always be observed in order to minimize the thermal stress to which the devices are subjected.

- Always preheat the device.
- The delta temperature between the preheat and soldering should be 100°C or less.\*
- When preheating and soldering, the temperature of the leads and the case must not exceed the maximum temperature ratings as shown on the data sheet. When using infrared heating with the reflow soldering method, the difference shall be a maximum of 10°C.
- The soldering temperature and time shall not exceed 260°C for more than 10 seconds.
- When shifting from preheating to soldering, the maximum temperature gradient shall be 5°C or less.
- After soldering has been completed, the device should be allowed to cool naturally for at least three minutes. Gradual cooling should be used as the use of forced cooling will increase the temperature gradient and result in latent failure due to mechanical stress.
- Mechanical stress or shock should not be applied during cooling.

\* Soldering a device without preheating can cause excessive thermal shock and stress which can result in damage to the device.

Thermal Clad is a registered trademark of the Bergquist Company.

# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 4:1

### SOT-553, 5 LEAD CASE 463B ISSUE C

DATE 20 MAR 2013

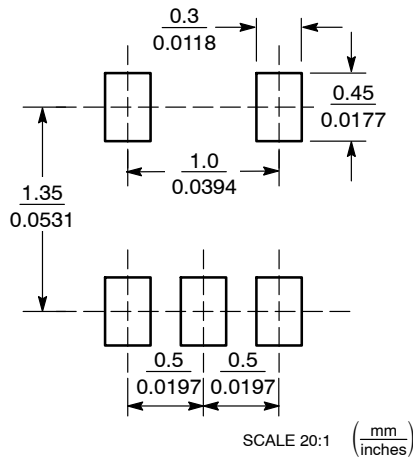


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

| DIM            | MILLIMETERS |      |      | INCHES    |       |       |
|----------------|-------------|------|------|-----------|-------|-------|
|                | MIN         | NOM  | MAX  | MIN       | NOM   | MAX   |
| A              | 0.50        | 0.55 | 0.60 | 0.020     | 0.022 | 0.024 |
| b              | 0.17        | 0.22 | 0.27 | 0.007     | 0.009 | 0.011 |
| c              | 0.08        | 0.13 | 0.18 | 0.003     | 0.005 | 0.007 |
| D              | 1.55        | 1.60 | 1.65 | 0.061     | 0.063 | 0.065 |
| E              | 1.15        | 1.20 | 1.25 | 0.045     | 0.047 | 0.049 |
| e              | 0.50 BSC    |      |      | 0.020 BSC |       |       |
| L              | 0.10        | 0.20 | 0.30 | 0.004     | 0.008 | 0.012 |
| H <sub>E</sub> | 1.55        | 1.60 | 1.65 | 0.061     | 0.063 | 0.065 |

### RECOMMENDED SOLDERING FOOTPRINT\*



### GENERIC MARKING DIAGRAM\*



- XX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 1:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 2:

- PIN 1. CATHODE
- 2. COMMON ANODE
- 3. CATHODE 2
- 4. CATHODE 3
- 5. CATHODE 4

STYLE 3:

- PIN 1. ANODE 1
- 2. N/C
- 3. ANODE 2
- 4. CATHODE 2
- 5. CATHODE 1

STYLE 4:

- PIN 1. SOURCE 1
- 2. DRAIN 1/2
- 3. SOURCE 1
- 4. GATE 1
- 5. GATE 2

STYLE 5:

- PIN 1. ANODE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. CATHODE

STYLE 6:

- PIN 1. EMITTER 2
- 2. BASE 2
- 3. EMITTER 1
- 4. COLLECTOR 1
- 5. COLLECTOR 2/BASE 1

STYLE 7:

- PIN 1. BASE
- 2. EMITTER
- 3. BASE
- 4. COLLECTOR
- 5. COLLECTOR

STYLE 8:

- PIN 1. CATHODE
- 2. COLLECTOR
- 3. N/C
- 4. BASE
- 5. EMITTER

STYLE 9:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. ANODE
- 5. ANODE

|                  |                           |  |
|------------------|---------------------------|--|
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| STATUS:          | ON SEMICONDUCTOR STANDARD |  |
| NEW STANDARD:    |                           |  |
| DESCRIPTION:     | SOT-553, 5 LEAD           | PAGE 1 OF 2  |



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