

NSBA123TDP6

Dual PNP Bias Resistor Transistors

R1 = 2.2 kΩ, R2 = ∞ kΩ

PNP Transistors with Monolithic Bias Resistor Network

This series of digital transistors is designed to replace a single device and its external resistor bias network. The Bias Resistor Transistor (BRT) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space.

Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- S and NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- This Device is Pb-Free, Halogen Free/BFR Free and is RoHS Compliant

MAXIMUM RATINGS

(T_A = 25°C, common for Q₁ and Q₂, unless otherwise noted)

| Rating | Symbol | Max | Unit |
|--------------------------------|----------------------|-----|------|
| Collector-Base Voltage | V _{CBO} | 50 | Vdc |
| Collector-Emitter Voltage | V _{CEO} | 50 | Vdc |
| Collector Current – Continuous | I _C | 100 | mAdc |
| Input Forward Voltage | V _{IN(fwd)} | 12 | Vdc |
| Input Reverse Voltage | V _{IN(rev)} | 5 | Vdc |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ORDERING INFORMATION

| Device | Package | Shipping [†] |
|----------------|---------|-----------------------|
| NSBA123TDP6T5G | SOT-963 | 8,000/Tape & Reel |

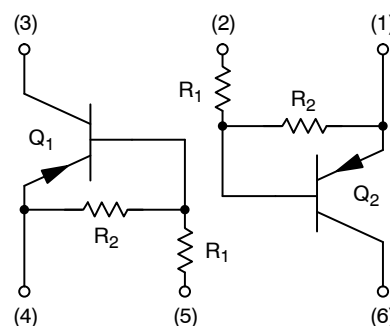
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



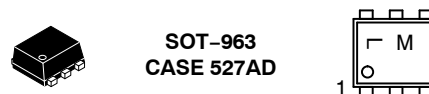
ON Semiconductor®

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PIN CONNECTIONS



MARKING DIAGRAM



L = Specific Device Code
M = Date Code*

*Date Code orientation may vary depending upon manufacturing location.

NSBA123TDP6

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|----------------|--------|-----|------|
|----------------|--------|-----|------|

NSBA123TDP6 (SOT-963) ONE JUNCTION HEATED

| | | | |
|---|-----------------|--------------------------|--------------------------------|
| Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) (Note 2) Derate above 25°C (Note 1) (Note 2) | P_D | 231 269 1.9 2.2 | MW mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction to Ambient (Note 1) (Note 2) | $R_{\theta JA}$ | 540 464 | $^\circ\text{C}/\text{W}$ |

NSBA123TDP6 (SOT-963) BOTH JUNCTION HEATED (Note 3)

| | | | |
|---|-----------------|--------------------------|--------------------------------|
| Total Device Dissipation $T_A = 25^\circ\text{C}$ (Note 1) (Note 2) Derate above 25°C (Note 1) (Note 2) | P_D | 339 408 2.7 3.3 | MW mW/ $^\circ\text{C}$ |
| Thermal Resistance, Junction to Ambient (Note 1) (Note 2) | $R_{\theta JA}$ | 369 306 | $^\circ\text{C}/\text{W}$ |
| Junction and Storage Temperature Range | T_J, T_{stg} | -55 to +150 | $^\circ\text{C}$ |

1. FR-4 @ 100 mm², 1 oz. copper traces, still air.
2. FR-4 @ 500 mm², 1 oz. copper traces, still air.
3. Both junction heated values assume total power is sum of two equally powered channels.

NSBA123TDP6

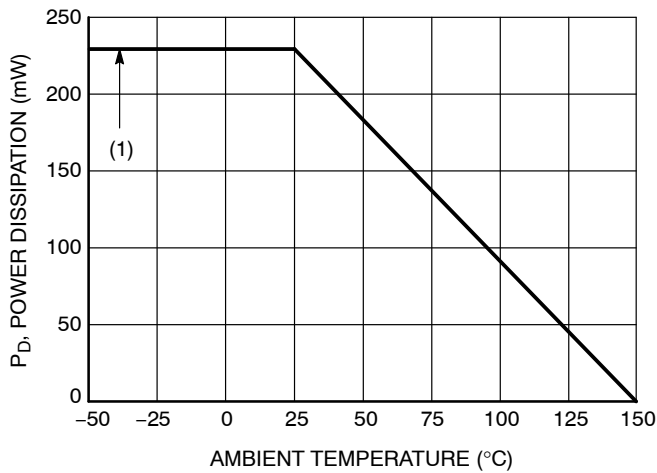
ELECTRICAL CHARACTERISTICS (T_A = 25°C, common for Q₁ and Q₂, unless otherwise noted)

| Characteristic | Symbol | Min | Typ | Max | Unit |
|---|----------------------|-----|-----|-----|------|
| OFF CHARACTERISTICS | | | | | |
| Collector-Base Cutoff Current (V _{CB} = 50 V, I _E = 0) | I _{CBO} | - | - | 100 | nAdc |
| Collector-Emitter Cutoff Current (V _{CE} = 50 V, I _B = 0) | I _{CEO} | - | - | 500 | nAdc |
| Emitter-Base Cutoff Current (V _{EB} = 6.0 V, I _C = 0) | I _{EBO} | - | - | 4.0 | mAdc |
| Collector-Base Breakdown Voltage (I _C = 10 μA, I _E = 0) | V _{(BR)CBO} | 50 | - | - | Vdc |
| Collector-Emitter Breakdown Voltage (Note 4) (I _C = 2.0 mA, I _B = 0) | V _{(BR)CEO} | 50 | - | - | Vdc |

ON CHARACTERISTICS

| | | | | | |
|--|--------------------------------|-----|-----|------|-----|
| DC Current Gain (Note 4) (I _C = 5.0 mA, V _{CE} = 10 V) | h _{FE} | 160 | 350 | - | |
| Collector-Emitter Saturation Voltage (Note 4) (I _C = 10 mA, I _B = 0.3 mA) | V _{CE(sat)} | - | - | 0.25 | V |
| Input Voltage (Off) (V _{CE} = 5.0 V, I _C = 100 μA) | V _{i(off)} | - | 0.6 | - | Vdc |
| Input Voltage (On) (V _{CE} = 0.2 V, I _C = 10 mA) | V _{i(on)} | - | 0.9 | - | Vdc |
| Output Voltage (On) (V _{CC} = 5.0 V, V _B = 2.5 V, R _L = 1.0 kΩ) | V _{OL} | - | - | 0.2 | Vdc |
| Output Voltage (Off) (V _{CC} = 5.0 V, V _B = 0.5 V, R _L = 1.0 kΩ) | V _{OH} | 4.9 | - | - | Vdc |
| Input Resistor | R1 | 1.5 | 2.2 | 2.9 | kΩ |
| Resistor Ratio | R ₁ /R ₂ | - | - | - | |

4. Pulsed Condition: Pulse Width = 300 ms, Duty Cycle ≤ 2%.



(1) SOT-963; 100 mm², 1 oz. Copper Trace

Figure 1. Derating Curve

NSBA123TDP6

TYPICAL CHARACTERISTICS NSBA123TDP6

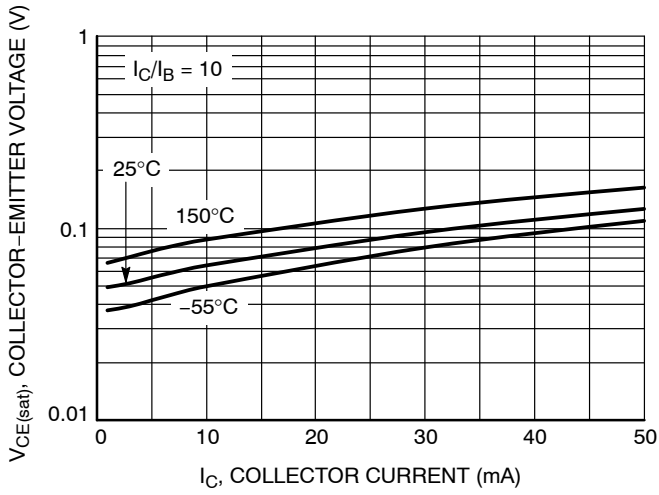


Figure 2. $V_{CE(sat)}$ vs. I_C

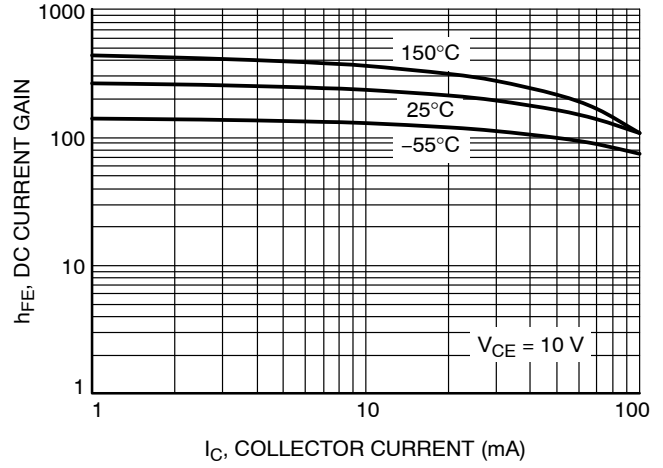


Figure 3. DC Current Gain

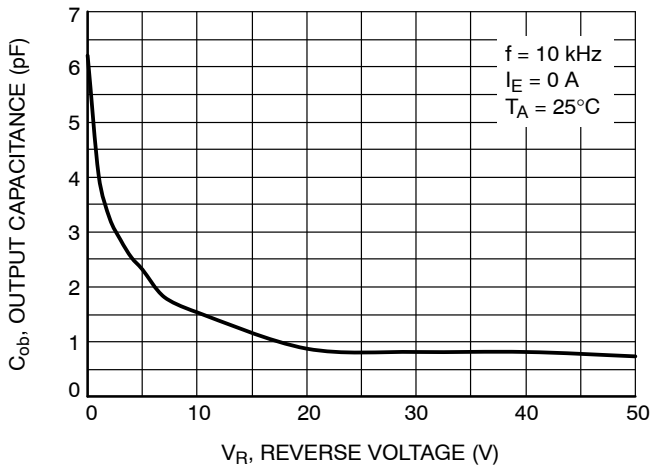


Figure 4. Output Capacitance

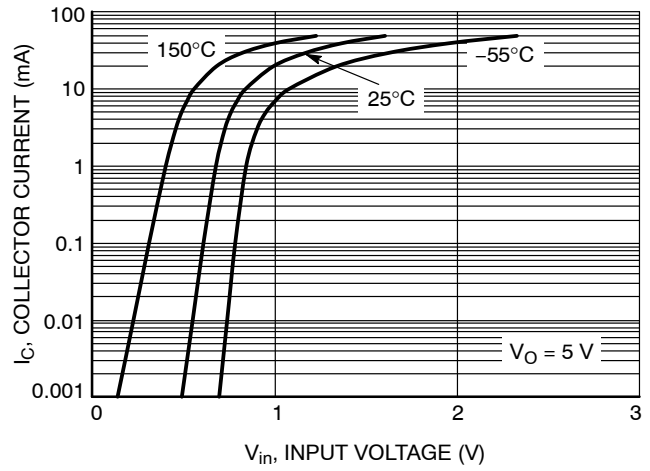


Figure 5. Output Current vs. Input Voltage

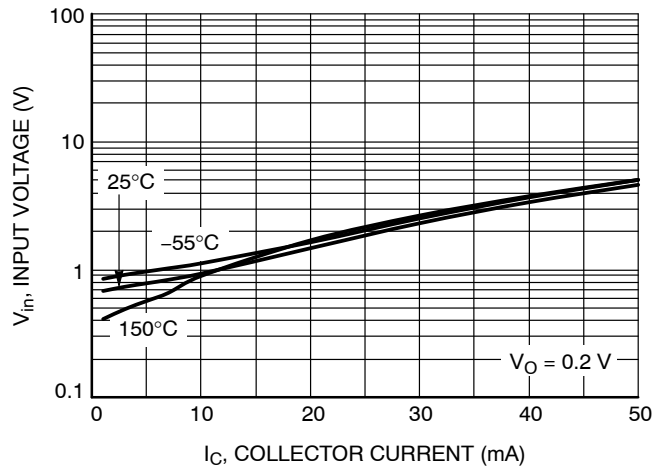
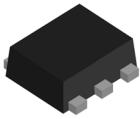


Figure 6. Input Voltage vs. Output Current

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

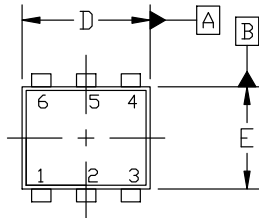


SOT-963 1.00x1.00x0.37, 0.35P
CASE 527AD
ISSUE F

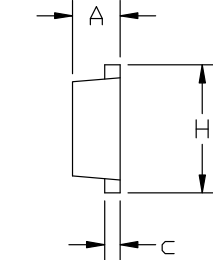
DATE 20 FEB 2024

NOTES:

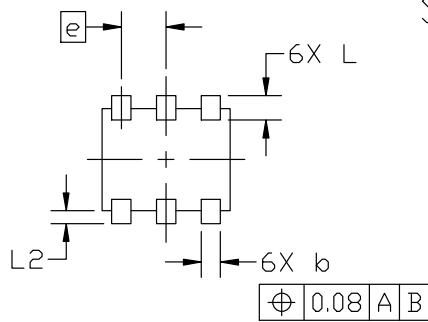
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.



TOP VIEW

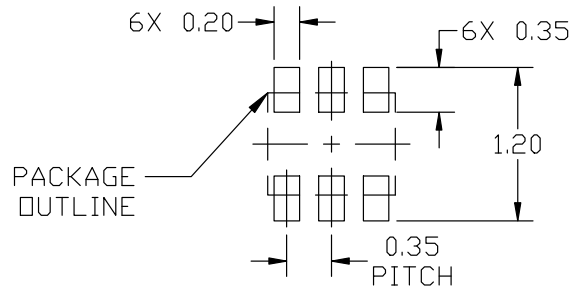


SIDE VIEW



BOTTOM VIEW

| DIM | MILLIMETERS | | |
|-----|-------------|------|------|
| | MIN. | NOM. | MAX. |
| A | 0.34 | 0.37 | 0.40 |
| b | 0.10 | 0.15 | 0.20 |
| c | 0.07 | 0.12 | 0.17 |
| D | 0.95 | 1.00 | 1.05 |
| E | 0.75 | 0.80 | 0.85 |
| e | 0.35 BSC | | |
| H | 0.95 | 1.00 | 1.05 |
| L | 0.19 REF | | |
| L2 | 0.05 | 0.10 | 0.15 |

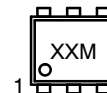


RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference manual, SOLDERRM/D.

- | | | |
|--|---|--|
| <p>STYLE 1: PIN 1. EMITTER 1 2. BASE 1 3. COLLECTOR 2 4. EMITTER 2 5. BASE 2 6. COLLECTOR 1</p> | <p>STYLE 2: PIN 1. EMITTER 1 2. EMITTER2 3. BASE 2 4. COLLECTOR 2 5. BASE 1 6. COLLECTOR 1</p> | <p>STYLE 3: PIN 1. CATHODE 1 2. CATHODE 1 3. ANODE/ANODE 2 4. CATHODE 2 5. CATHODE 2 6. ANODE/ANODE 1</p> |
| <p>STYLE 4: PIN 1. COLLECTOR 2. COLLECTOR 3. BASE 4. EMITTER 5. COLLECTOR 6. COLLECTOR</p> | <p>STYLE 5: PIN 1. CATHODE 2. CATHODE 3. ANODE 4. ANODE 5. CATHODE 6. CATHODE</p> | <p>STYLE 6: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE</p> |
| <p>STYLE 7: PIN 1. CATHODE 2. ANODE 3. CATHODE 4. CATHODE 5. ANODE 6. CATHODE</p> | <p>STYLE 8: PIN 1. DRAIN 2. DRAIN 3. GATE 4. SOURCE 5. DRAIN 6. DRAIN</p> | <p>STYLE 9: PIN 1. SOURCE 1 2. GATE 1 3. DRAIN 2 4. SOURCE 2 5. GATE 2 6. DRAIN 1</p> |
| <p>STYLE 10: PIN 1. CATHODE 1 2. N/C 3. CATHODE 2 4. ANODE 2 5. N/C 6. ANODE 1</p> | | |

GENERIC MARKING DIAGRAM*



XX = Specific Device Code
 M = Month Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

| | | |
|-------------------------|--------------------------------------|--|
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| DESCRIPTION: | SOT-963 1.00x1.00x0.37, 0.35P | PAGE 1 OF 1 |

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