# CM1263-02SE

# Low Capacitance ESD Protection for High-Speed Serial Interfaces

#### **Features**

- 2 Channels of ESD Protection
- 0.85 pF Loading Capacitance per Channel Typical
- Provides ESD Protection to IEC61000-4-2 Level 4:
  - ±8 kV Contact Discharge
  - ±15 kV Air Discharge
- 5-Pin SOT-553 Package
- These Devices are Pb-Free and are RoHS Compliant

#### **Applications**

- LCD and Camera Data Lines in Wireless Handsets that Use High-speed Serial Interfaces such as MDDI, MIPI, MVI and MPL
- I/O Port Protection for Mobile Handsets, Notebook Computers, PDAs, etc.
- Wireless Handsets
- Handheld PCs/PDAs
- LCD and Camera Modules



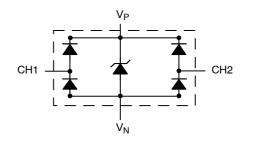
# ON Semiconductor®

http://onsemi.com



SOT-553 SE SUFFIX CASE 463B

#### **BLOCK DIAGRAM**



#### **MARKING DIAGRAM**



L63 = Specific Device Code M = Date Code

#### **ORDERING INFORMATION**

Device	Package	Shipping <sup>†</sup>
CM1263-02SE	SOT-553 (Pb-Free)	5000/Tape & Reel

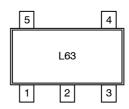
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

# CM1263-02SE

**Table 1. PIN DESCRIPTIONS** 

5-Pin, SOT-553 Package				
Pin	Pin Description			
1	V <sub>P</sub>			
2	V <sub>N</sub>			
3	NC			
4	(CH1) ESD Channel #1			
5	(CH2) ESD Channel #2			

#### **PACKAGE / PINOUT DIAGRAM**



## **SPECIFICATIONS**

**Table 2. ABSOLUTE MAXIMUM RATINGS** 

Parameter	Rating	Units
Operating Supply Voltage (V <sub>P</sub> – V <sub>N</sub> )	6.0	V
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	$(V_N - 0.5)$ to $(V_P + 0.5)$	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## CM1263-02SE

Table 3. ELECTRICAL OPERATING CHARACTERISTICS (Note 1)

Symbol	Parameter	Conditions	Min	Тур	Max	Units
V <sub>P</sub>	Operating Supply Voltage (V <sub>P</sub> – V <sub>N</sub> )			3.3	5.5	V
l <sub>P</sub>	Operating Supply Current	$(V_P - V_N) = 3.3 \text{ V}$			8.0	μΑ
V <sub>F</sub>	Diode Forward Voltage Top Diode Bottom Diode	I <sub>F</sub> = 8 mA; T <sub>A</sub> = 25°C	0.60 0.60	0.80 0.80	0.95 0.95	٧
I <sub>LEAK</sub>	Channel Leakage Current	$T_A = 25^{\circ}C; V_P = 5 \text{ V}, V_N = 0 \text{ V}, V_{TEST} = 0 \text{ to } 5 \text{ V}$		0.1	1.0	μΑ
C <sub>IN</sub>	Channel Input Capacitance	At 1 MHz, V <sub>P</sub> = 3.3 V, V <sub>N</sub> = 0 V, V <sub>IN</sub> = 1.65 V		0.85	1.2	pF
$\Delta C_{IN}$	Channel Input Capacitance Matching	At 1 MHz, V <sub>P</sub> = 3.3 V, V <sub>N</sub> = 0 V, V <sub>IN</sub> = 1.65 V		0.02		pF
V <sub>ESD</sub>	ESD Protection Peak Discharge Voltage at any channel input, in system: a) Contact Discharge per IEC 61000-4-2 standard b) Air Discharge per IEC 61000-4-2 standard	T <sub>A</sub> = 25°C; (Notes 2 and 3) T <sub>A</sub> = 25°C; (Note 3)	±8 ±15			kV
V <sub>CL</sub>	Channel Clamp Voltage Positive Transients Negative Transients	$T_A = 25^{\circ}C$ , $I_{PP} = 1$ A, $t_P = 8/20 \ \mu S$ (Note 3)		+9.96 -1.6		V
R <sub>DYN</sub>	Dynamic Resistance Positive Transients Negative Transients	$\begin{split} I_{PP} = 1 & \text{A, t}_P = 8/20 \ \mu\text{S} \\ \text{Any I/O pin to Ground;} \\ \text{(Note 3)} \end{split}$		0.96 0.5		Ω

<sup>1.</sup> All parameters specified at  $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  unless otherwise noted.
2. Standard IEC 61000–4–2 with  $C_{Discharge} = 150\text{pF}$ ,  $R_{Discharge} = 330~\Omega$ ,  $V_P = 3.3~V$ ,  $V_N$  grounded.
3. These measurements performed with no external capacitor on  $V_P$  ( $V_P$  floating).

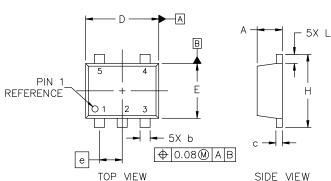






#### SOT-553-5 1.60x1.20x0.55, 0.50P CASE 463B ISSUE D

**DATE 21 FEB 2024** 



#### NOTES:

- DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5-2018.
- ALL DIMENSION ARE IN MILLIMETERS.
- MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

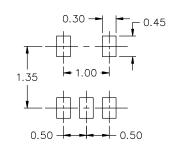
DIM	MILLIMETERS			
DIM	MIN.	NOM.	MAX.	
А	0.50	0.55	0.60	
b	0.17	0.22	0.27	
С	0.08	0.13	0.18	
D	1.55	1.60	1.65	
Е	1.15	1.20	1.25	
е	0.50 BSC			
Н	1.55	1.60	1.65	
L	0.10	0.20	0.30	

STYLE 5:

PIN 1. ANODE 2. EMITTER

3. BASE 4. COLLECTOR

5. CATHODE



#### RECOMMENDED MOUNTING FOOTPRINT\*

\* FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE
DOWNLOAD THE ON SEMICONDUCTOR SOLDERING
AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

## **GENERIC MARKING DIAGRAM\***



XX = Specific Device Code

M = Date Code

3. BASE 4. COLLECTOR

5. COLLECTOR

= Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may

not follow the Generic Marking. STYLE 1: STYLE 2: PIN 1. CATHODE 2. COMMON ANODE PIN 1. BASE 2. EMITTER

STYLE 6: STYLE 9: STYLE 7 STYLE 8: PIN 1. EMITTER 2 PIN 1. CATHODE 2. COLLECTOR PIN 1. ANODE 2. CATHODE PIN 1. BASE 2. EMITTER 2. BASE 2 3. EMITTER 1 3. BASE 4. COLLECTOR 3. N/C 4. BASE 3. ANODE 4. ANODE 4. COLLECTOR 1

3. CATHODE 2 4. CATHODE 3

CATHODE 4

COLLECTOR 2/BASE 1 5. EMITTER ANODE Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. **DOCUMENT NUMBER:** 98AON11127D

**DESCRIPTION:** SOT-553-5 1.60x1.20x0.55, 0.50P PAGE 1 OF 1

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STYLE 3:

PIN 1. ANODE 1 2. N/C

3. ANODE 2 4. CATHODE 2

CATHODE 1

STYLE 4:

PIN 1. SOURCE 1

5. GATE 2

2. DRAIN 1/2

3. SOURCE 1 4. GATE 1

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