

# BUL45G

## NPN Silicon Power Transistor

### High Voltage Switch-mode Series

Designed for use in electronic ballast (light ballast) and in switch-mode power supplies up to 50 W.

#### Features

- Improved Efficiency Due to:
  - ◆ Low Base Drive Requirements (High and Flat DC Current Gain  $h_{FE}$ )
  - ◆ Low Power Losses (On-State and Switching Operations)
  - ◆ Fast Switching:  $t_{fi} = 100$  ns (typ) and  $t_{si} = 3.2$   $\mu$ s (typ)
  - ◆ @  $I_C = 2.0$  A,  $I_{B1} = I_{B2} = 0.4$  A
- Full Characterization at 125°C
- Tight Parametric Distributions Consistent Lot-to-Lot
- These Devices are Pb-Free and are RoHS Compliant\*

#### MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector-Emitter Sustaining Voltage	$V_{CEO}$	400	Vdc
Collector-Base Breakdown Voltage	$V_{CES}$	700	Vdc
Emitter-Base Voltage	$V_{EBO}$	9.0	Vdc
Collector Current - Continuous - Peak (Note 1)	$I_C$ $I_{CM}$	5.0 10	Adc
Base Current	$I_B$	2.0	Adc
Total Device Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C	$P_D$	75 0.6	W W/°C
Operating and Storage Temperature	$T_J, T_{stg}$	-65 to 150	°C

#### THERMAL CHARACTERISTICS

Characteristics	Symbol	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	1.65	°C/W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	62.5	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

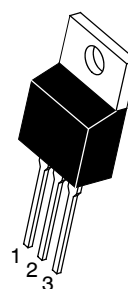
1. Pulse Test: Pulse Width = 5 ms, Duty Cycle  $\leq$  10%.



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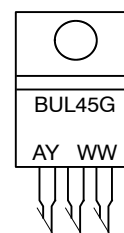
<http://onsemi.com>

**POWER TRANSISTOR**  
**5.0 AMPERES, 700 VOLTS,**  
**35 AND 75 WATTS**



TO-220AB  
CASE 221A-09  
STYLE 1

#### MARKING DIAGRAM



BUL45 = Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

#### ORDERING INFORMATION

Device	Package	Shipping
BUL45G	TO-220 (Pb-Free)	50 Units / Rail

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# BUL45G

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Collector-Emitter Sustaining Voltage (I <sub>C</sub> = 100 mA, L = 25 mH)	V <sub>CEO(sus)</sub>	400	-	-	Vdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEO</sub> , I <sub>B</sub> = 0)	I <sub>CEO</sub>	-	-	100	μAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CES</sub> , V <sub>EB</sub> = 0) (T <sub>C</sub> = 125°C)	I <sub>CES</sub>	-	-	10 100	μAdc
Emitter Cutoff Current (V <sub>EB</sub> = 9.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	-	-	100	μAdc

### ON CHARACTERISTICS

Base-Emitter Saturation Voltage (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.2 Adc) (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.4 Adc)	V <sub>BE(sat)</sub>	-	0.84 0.89	1.2 1.25	Vdc
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 1.0 Adc, I <sub>B</sub> = 0.2 Adc) (T <sub>C</sub> = 125°C)	V <sub>CE(sat)</sub>	-	0.175 0.150	0.25 -	Vdc
Collector-Emitter Saturation Voltage (I <sub>C</sub> = 2.0 Adc, I <sub>B</sub> = 0.4 Adc) (T <sub>C</sub> = 125°C)	V <sub>CE(sat)</sub>	-	0.25 0.275	0.4 -	Vdc
DC Current Gain (I <sub>C</sub> = 0.3 Adc, V <sub>CE</sub> = 5.0 Vdc) (I <sub>C</sub> = 2.0 Adc, V <sub>CE</sub> = 1.0 Vdc) (I <sub>C</sub> = 10 mAdc, V <sub>CE</sub> = 5.0 Vdc)	h <sub>FE</sub>	14 - 7.0 5.0 10	- 32 14 12 22	34 - - - -	-

### DYNAMIC CHARACTERISTICS

Current Gain Bandwidth (I <sub>C</sub> = 0.5 Adc, V <sub>CE</sub> = 10 Vdc, f = 1.0 MHz)	f <sub>T</sub>	-	12	—	MHz		
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)	C <sub>ob</sub>	-	50	75	pF		
Input Capacitance (V <sub>EB</sub> = 8.0 Vdc)	C <sub>ib</sub>	-	920	1200	pF		
Dynamic Saturation Voltage: Determined 1.0 μs and 3.0 μs respectively after rising I <sub>B1</sub> reaches 90% of final I <sub>B1</sub> (see Figure 18)	V <sub>CE</sub> (Dyn sat)	(I <sub>C</sub> = 1.0 Adc I <sub>B1</sub> = 100 mAdc V <sub>CC</sub> = 300 V)	1.0 μs (T <sub>C</sub> = 125°C)	-	1.75	-	Vdc
			3.0 μs (T <sub>C</sub> = 125°C)	-	4.4	-	
		(I <sub>C</sub> = 2.0 Adc I <sub>B1</sub> = 400 mAdc V <sub>CC</sub> = 300 V)	1.0 μs (T <sub>C</sub> = 125°C)	-	0.5	-	
			3.0 μs (T <sub>C</sub> = 125°C)	-	1.0	-	

### SWITCHING CHARACTERISTICS: Resistive Load

Turn-On Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = I <sub>B2</sub> = 0.4 Adc Pulse Width = 20 μs, (T <sub>C</sub> = 125°C)	t <sub>on</sub>	-	75 120	110 -	ns
Turn-Off Time	Duty Cycle < 20% V <sub>CC</sub> = 300 V (T <sub>C</sub> = 125°C)	t <sub>off</sub>	-	2.8 3.5	3.5 -	μs

### SWITCHING CHARACTERISTICS: Inductive Load (V<sub>CC</sub> = 15 Vdc, L<sub>C</sub> = 200 μH, V<sub>clamp</sub> = 300 Vdc)

Fall Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = 0.4 Adc I <sub>B2</sub> = 0.4 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	70 -	- 200	170 -	ns
Storage Time		t <sub>si</sub>	2.6 -	- 4.2	3.8 -	μs
Crossover Time	(T <sub>C</sub> = 125°C)	t <sub>c</sub>	- -	230 400	350 -	ns
Fall Time	(I <sub>C</sub> = 1.0 Adc, I <sub>B1</sub> = 100 mAdc I <sub>B2</sub> = 0.5 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	- -	110 100	150 -	ns
Storage Time		t <sub>si</sub>	- -	1.1 1.5	1.7 -	μs
Crossover Time	(T <sub>C</sub> = 125°C)	t <sub>c</sub>	- -	170 170	250 -	ns
Fall Time	(I <sub>C</sub> = 2.0 Adc, I <sub>B1</sub> = 250 mAdc I <sub>B2</sub> = 2.0 Adc) (T <sub>C</sub> = 125°C)	t <sub>fi</sub>	-	80	120	ns
Storage Time		t <sub>si</sub>	-	0.6	0.9	μs
Crossover Time	(T <sub>C</sub> = 125°C)	t <sub>c</sub>	-	175	300	ns

# BUL45G

## TYPICAL STATIC CHARACTERISTICS

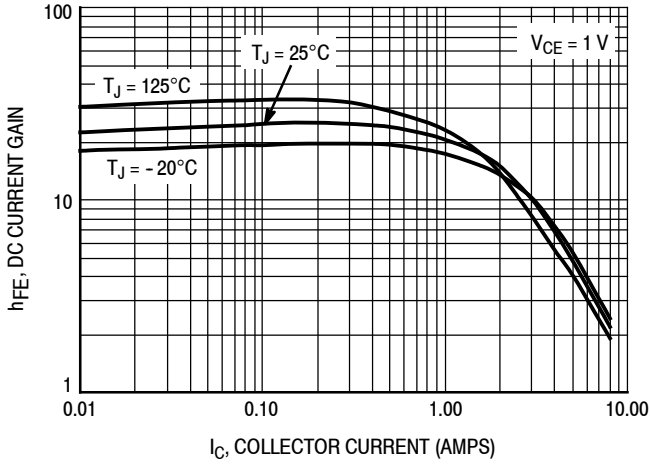


Figure 1. DC Current Gain @ 1 Volt

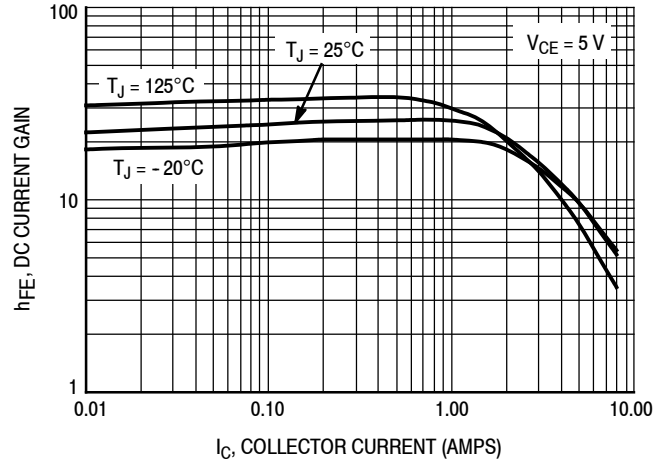


Figure 2. DC Current Gain at @ 5 Volts

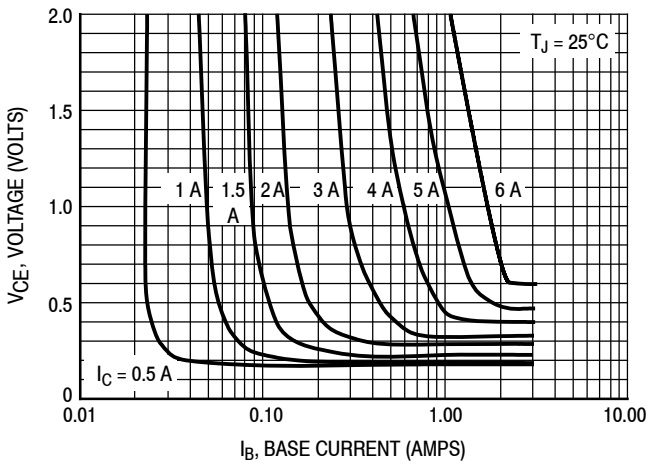


Figure 3. Collector-Emitter Saturation Region

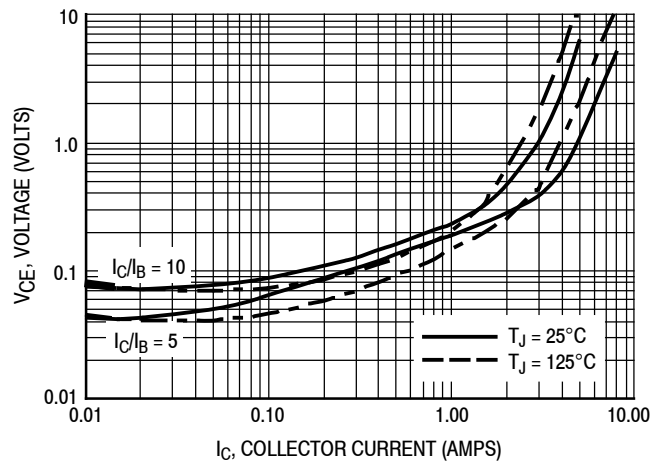


Figure 4. Collector-Emitter Saturation Voltage

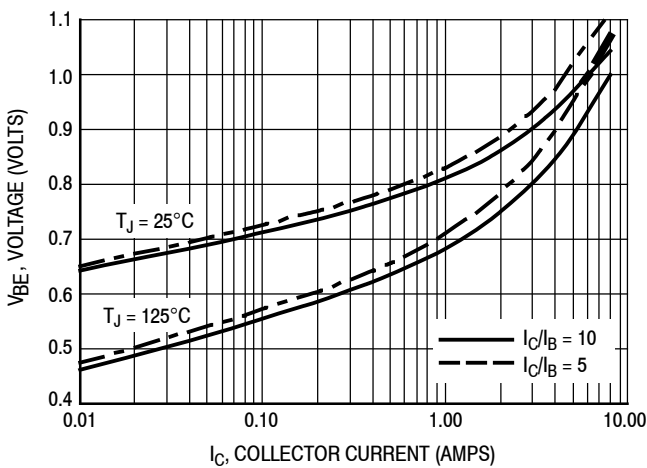


Figure 5. Base-Emitter Saturation Region

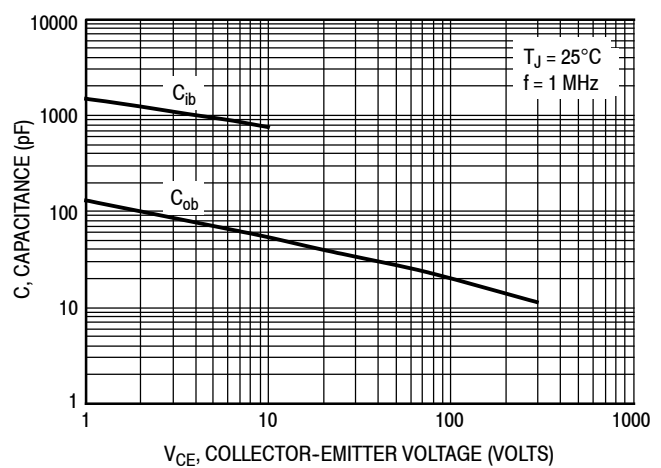


Figure 6. Capacitance

**TYPICAL SWITCHING CHARACTERISTICS**  
( $I_{B2} = I_C/2$  for all switching)

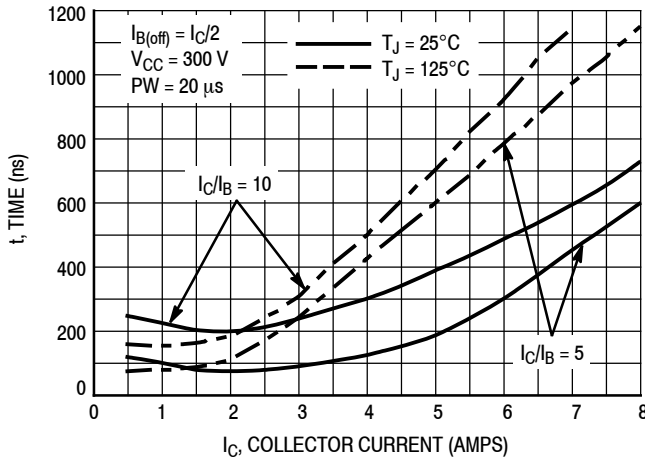


Figure 7. Resistive Switching,  $t_{on}$

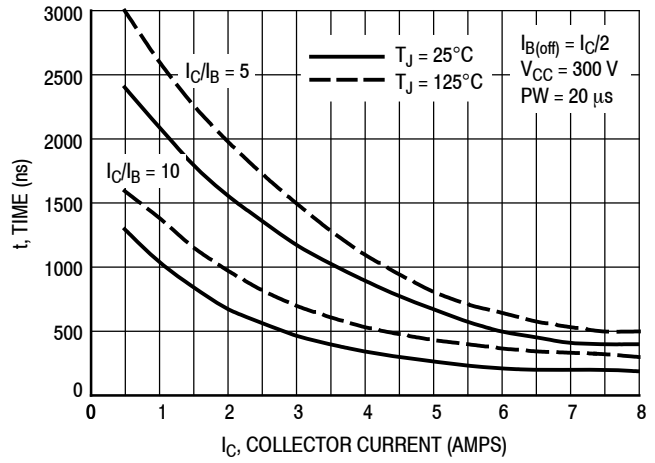


Figure 8. Resistive Switching,  $t_{off}$

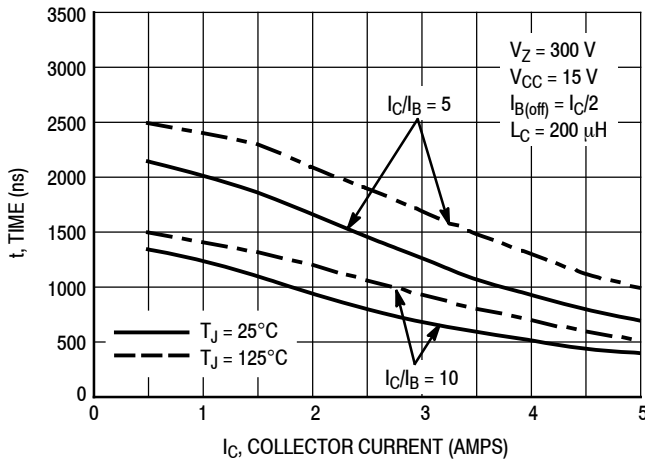


Figure 9. Inductive Storage Time,  $t_{si}$

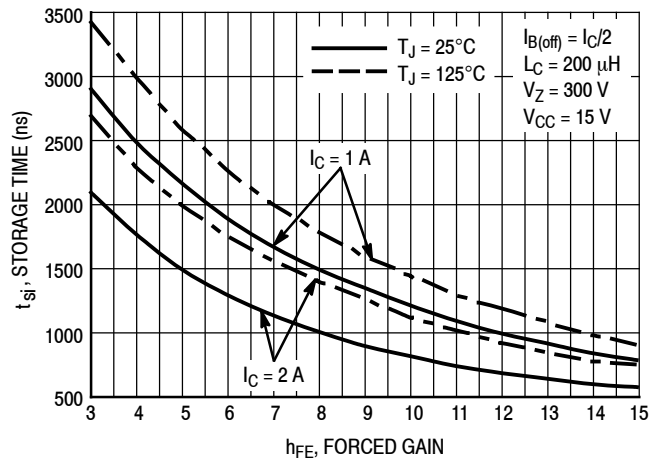


Figure 10. Inductive Storage Time,  $t_{si}(h_{FE})$

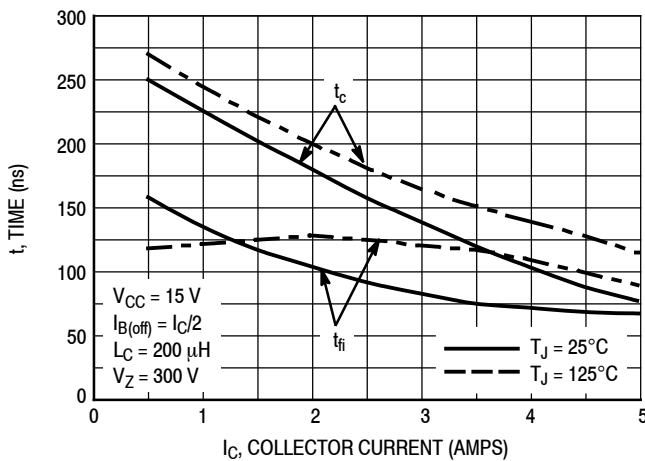


Figure 11. Inductive Switching,  $t_c$  &  $t_{fi}$ ,  $I_C/I_B = 5$

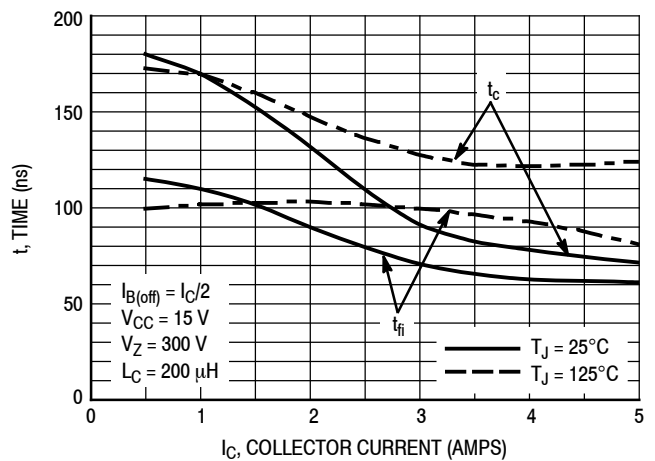


Figure 12. Inductive Switching,  $t_c$  &  $t_{fi}$ ,  $I_C/I_B = 10$

**TYPICAL SWITCHING CHARACTERISTICS**  
( $I_{B2} = I_C/2$  for all switching)

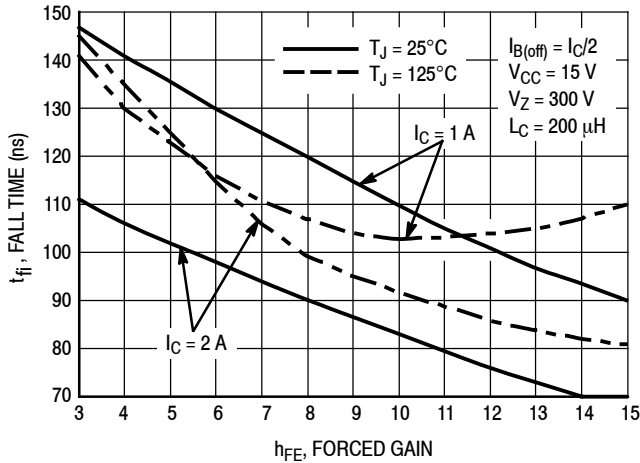


Figure 13. Inductive Fall Time,  $t_{fi}(h_{FE})$

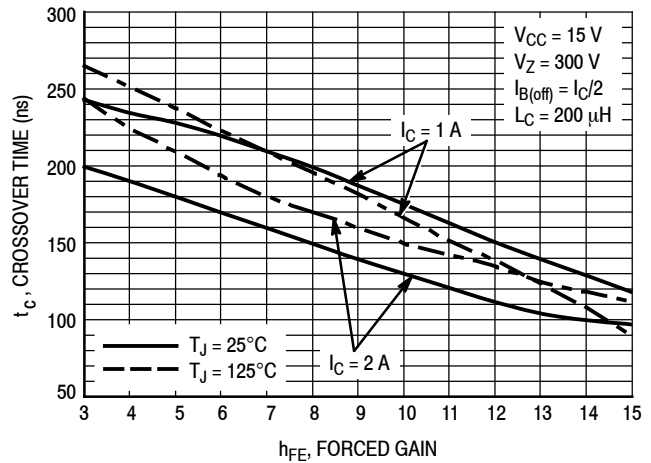


Figure 14. Crossover Time

**GUARANTEED SAFE OPERATING AREA INFORMATION**

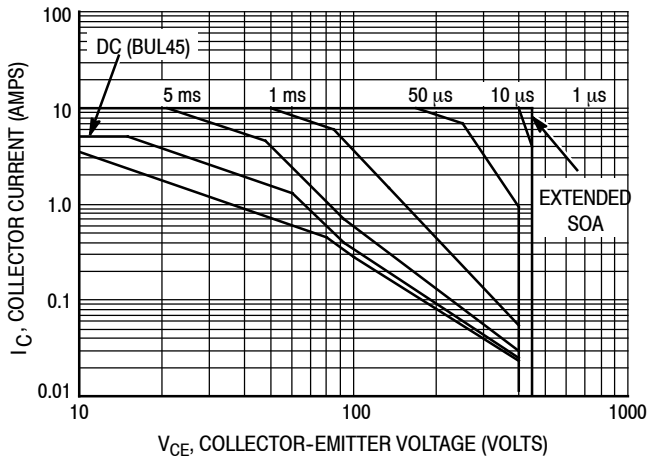


Figure 15. Forward Bias Safe Operating Area

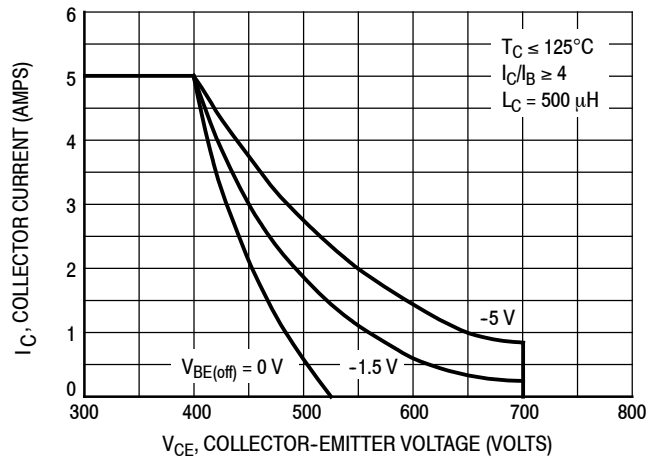


Figure 16. Reverse Bias Switching Safe Operating Area

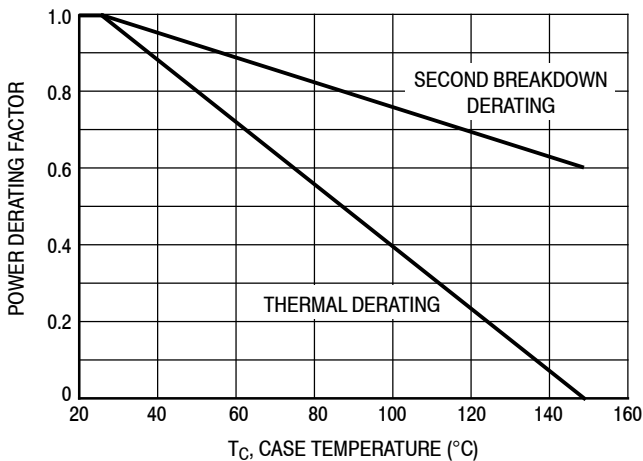


Figure 17. Forward Bias Power Derating

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 15 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown in Figure 15 may be found at any case temperature by using the appropriate curve on Figure 17.  $T_{J(pk)}$  may be calculated from the data in Figures 20. At any case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown. For inductive loads, high voltage and current must be sustained simultaneously during turn-off with the base-to-emitter junction reverse-biased. The safe level is specified as a reverse-biased safe operating area (Figure 16). This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode.

# BUL45G

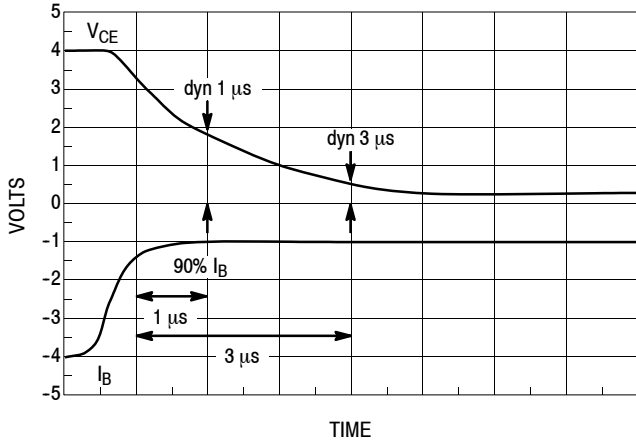


Figure 18. Dynamic Saturation Voltage Measurements

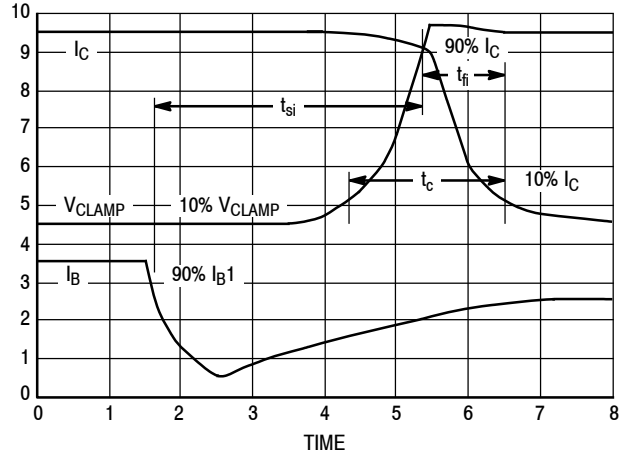
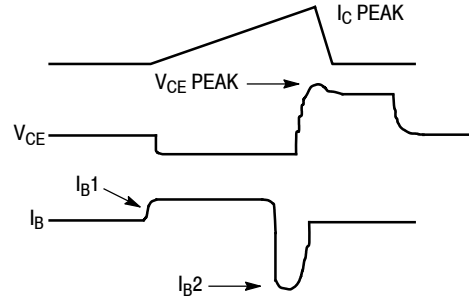
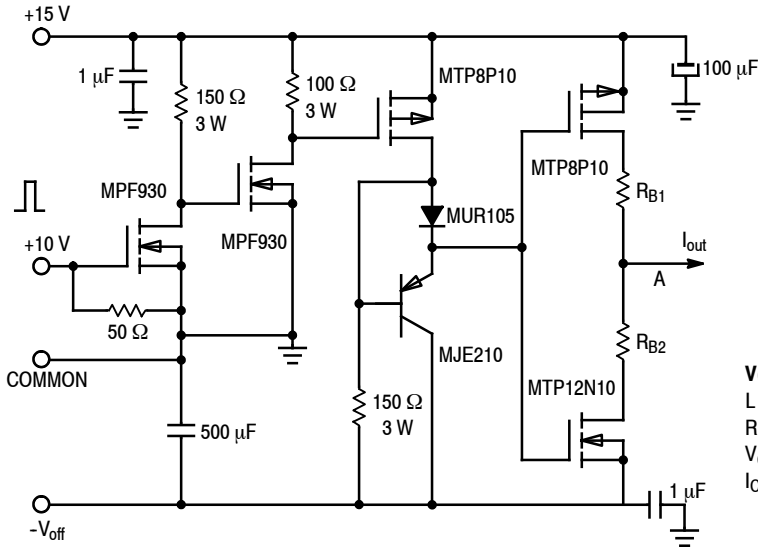


Figure 19. Inductive Switching Measurements



V(BR)CEO(sus)	INDUCTIVE SWITCHING	RBSOA
L = 10 mH	L = 200 μH	L = 500 μH
RB2 = ∞	RB2 = 0	RB2 = 0
VCC = 20 VOLTS	VCC = 15 VOLTS	VCC = 15 VOLTS
IC(pk) = 100 mA	RB1 SELECTED FOR DESIRED IB1	RB1 SELECTED FOR DESIRED IB1

Table 1. Inductive Load Switching Drive Circuit

## TYPICAL THERMAL RESPONSE

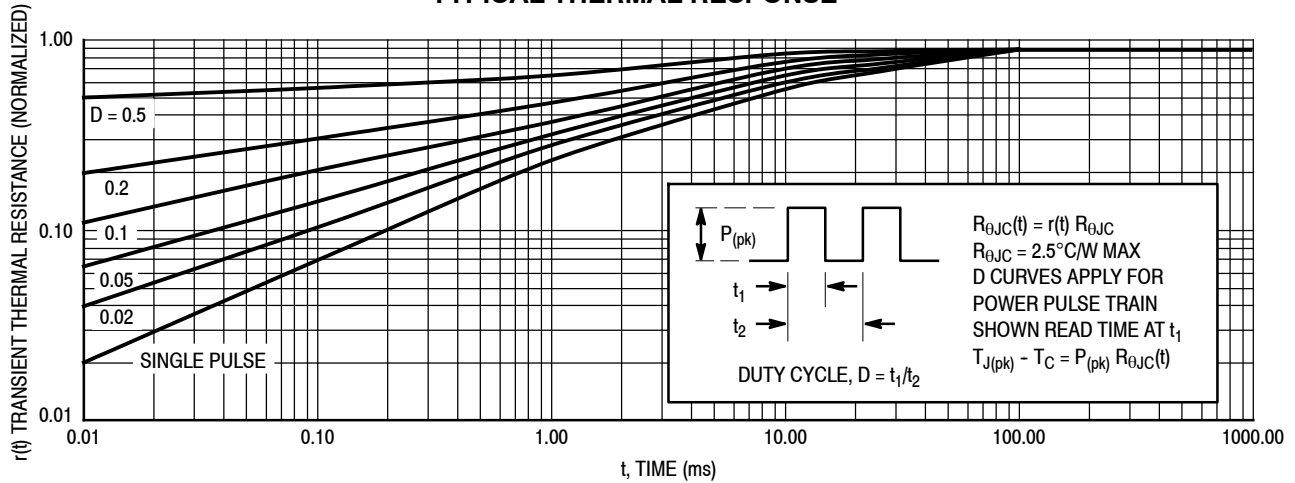
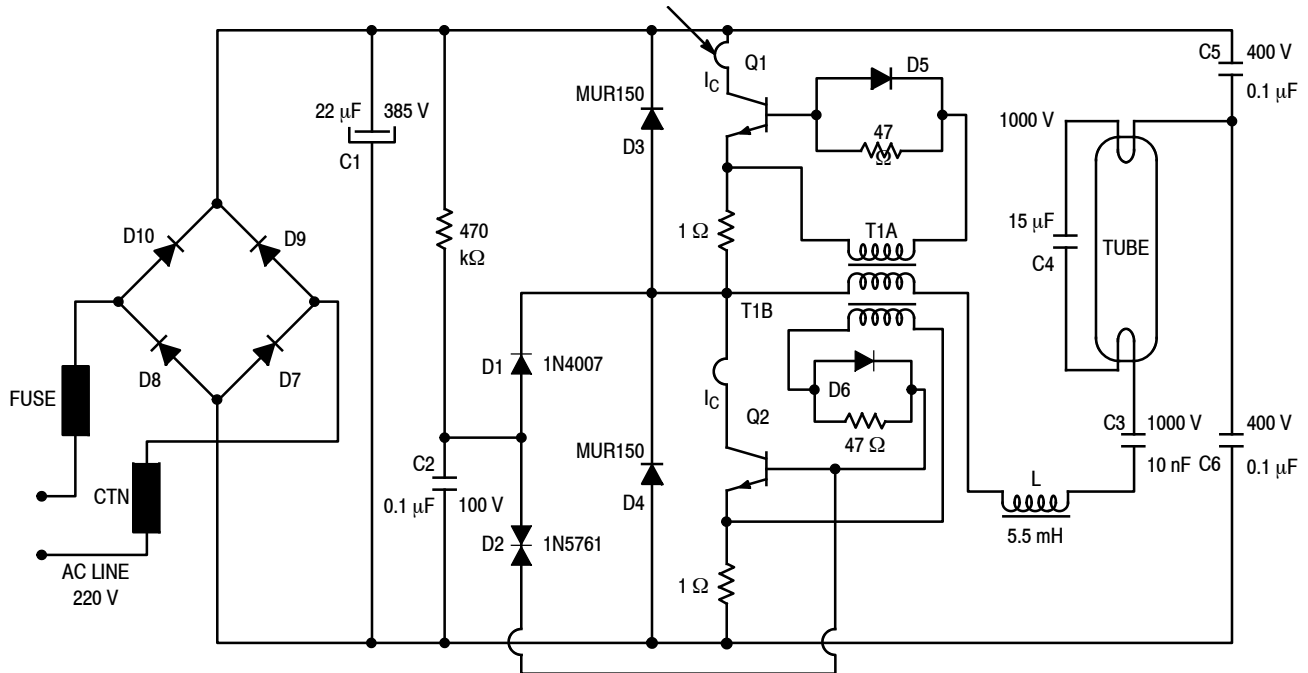


Figure 20. Typical Thermal Response ( $Z_{\theta JC}(t)$ ) for BUL45

## BUL45G

The BUL45 Bipolar Power Transistors were specially designed for use in electronic lamp ballasts. A circuit designed by ON Semiconductor applications was built to

demonstrate how well these devices operate. The circuit and detailed component list are provided below.



### Components Lists

Q1 = Q2 = BUL45 Transistor  
 D1 = 1N4007 Rectifier  
 D2 = 1N5761 Rectifier  
 D3 = D4 = MUR150  
 D5 = D6 = MUR105  
 D7 = D8 = D9 = D10 = 1N400

CTN = 47 Ω @ 25°C

L = RM10 core, A1 = 400, B51 (LCC) 75 turns,  
 wire  $\varnothing$  = 0.6 mm

T1 = FT10 toroid, T4A (LCC)

Primary: 4 turns

Secondaries: T1A: 4 turns

T1B: 4 turns

All resistors are 1/4 Watt,  $\pm 5\%$

R1 = 470 kΩ

R2 = R3 = 47 Ω

R4 = R5 = 1 Ω (these resistors are optional, and  
 might be replaced by a short circuit)

C1 = 22 μF/385 V

C2 = 0.1 μF

C3 = 10 nF/1000 V

C4 = 15 nF/1000 V

C5 = C6 = 0.1 μF/400 V

### NOTES:

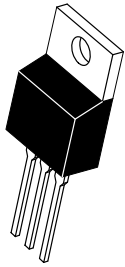
1. Since this design does not include the line input filter, it cannot be used "as-is" in a practical industrial circuit.
2. The windings are given for a 55 Watt load. For proper operation they must be re-calculated with any other loads.

**Figure 21. Application Example**

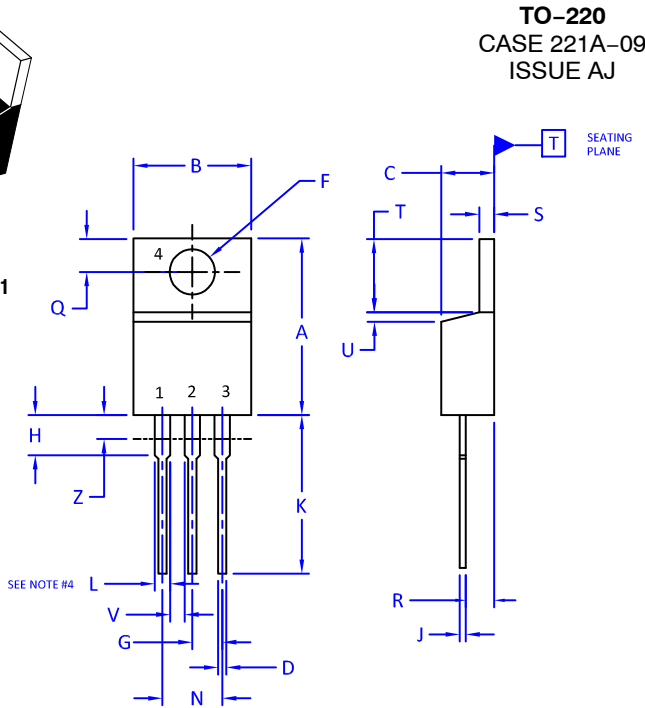
# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



SCALE 1:1



DATE 05 NOV 2019

**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.570	0.620	14.48	15.75
B	0.380	0.415	9.66	10.53
C	0.160	0.190	4.07	4.83
D	0.025	0.038	0.64	0.96
F	0.142	0.161	3.60	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.161	2.80	4.10
J	0.014	0.024	0.36	0.61
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.41
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

**STYLE 1:**

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

**STYLE 2:**

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

**STYLE 3:**

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

**STYLE 4:**

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

**STYLE 5:**

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

**STYLE 6:**

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

**STYLE 7:**

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

**STYLE 8:**

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

**STYLE 9:**

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

**STYLE 10:**

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

**STYLE 11:**

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

**STYLE 12:**

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

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