

# BDW42G (NPN), BDW46G, BDW47G (PNP)

## Darlington Complementary Silicon Power Transistors

This series of plastic, medium-power silicon NPN and PNP Darlington transistors are designed for general purpose and low speed switching applications.

### Features

- High DC Current Gain –  $h_{FE} = 2500$  (typ) @  $I_C = 5.0$  Adc.
- Collector Emitter Sustaining Voltage @ 30 mAdc:  
 $V_{CE(sus)} = 80$  Vdc (min) – BDW46  
100 Vdc (min) – BDW42/BDW47
- Low Collector Emitter Saturation Voltage  
 $V_{CE(sat)} = 2.0$  Vdc (max) @  $I_C = 5.0$  Adc  
3.0 Vdc (max) @  $I_C = 10.0$  Adc
- Monolithic Construction with Built-In Base Emitter Shunt resistors
- TO-220 Compact Package
- These Devices are Pb-Free and are RoHS Compliant\*

### MAXIMUM RATINGS

| Rating  | Symbol         | Value       | Unit                     |
|---|----------------|-------------|--------------------------|
| Collector-Emitter Voltage<br>BDW46<br>BDW42, BDW47  | $V_{CEO}$      | 80<br>100   | Vdc                      |
| Collector-Base Voltage<br>BDW46<br>BDW42, BDW47   | $V_{CB}$       | 80<br>100   | Vdc                      |
| Emitter-Base Voltage  | $V_{EB}$       | 5.0         | Vdc                      |
| Collector Current   | $I_C$          | 15          | Adc                      |
| Base Current  | $I_B$          | 0.5         | Adc                      |
| Total Device Dissipation<br>@ $T_C = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$          | 85<br>0.68  | W<br>W/ $^\circ\text{C}$ |
| Operating and Storage Junction<br>Temperature Range                                       | $T_J, T_{stg}$ | -55 to +150 | $^\circ\text{C}$         |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Characteristic                          | Symbol          | Max  | Unit                      |
|---|-----------------|------|---------------------------|
| Thermal Resistance,<br>Junction-to-Case | $R_{\theta JC}$ | 1.47 | $^\circ\text{C}/\text{W}$ |

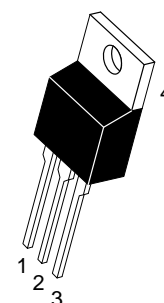
\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



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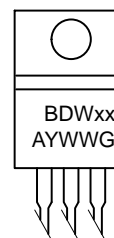
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## 15 AMP DARLINGTON COMPLEMENTARY SILICON POWER TRANSISTORS 80-100 VOLT, 85 WATT



TO-220  
CASE 221A  
STYLE 1

### MARKING DIAGRAM



BDWxx = Device Code  
x = 42, 46, or 47  
A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

### ORDERING INFORMATION

| Device | Package             | Shipping      |
|--------|---------------------|---------------|
| BDW42G | TO-220<br>(Pb-Free) | 50 Units/Rail |
| BDW46G | TO-220<br>(Pb-Free) | 50 Units/Rail |
| BDW47G | TO-220<br>(Pb-Free) | 50 Units/Rail |

## BDW42G (NPN), BDW46G, BDW47G (PNP)

### ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|----------------|--------|-----|-----|------|
|----------------|--------|-----|-----|------|

#### OFF CHARACTERISTICS

|   |                      |                |           |            |      |
|---|----------------------|----------------|-----------|------------|------|
| Collector Emitter Sustaining Voltage (Note 1)<br>( $I_C = 30\text{ mAdc}$ , $I_B = 0$ )                           | BDW46<br>BDW42/BDW47 | $V_{CEO(sus)}$ | 80<br>100 | –<br>–     | Vdc  |
| Collector Cutoff Current<br>( $V_{CE} = 40\text{ Vdc}$ , $I_B = 0$ )<br>( $V_{CE} = 50\text{ Vdc}$ , $I_B = 0$ )  | BDW46<br>BDW42/BDW47 | $I_{CEO}$      | –<br>–    | 2.0<br>2.0 | mAdc |
| Collector Cutoff Current<br>( $V_{CB} = 80\text{ Vdc}$ , $I_E = 0$ )<br>( $V_{CB} = 100\text{ Vdc}$ , $I_E = 0$ ) | BDW46<br>BDW42/BDW47 | $I_{CBO}$      | –<br>–    | 1.0<br>1.0 | mAdc |
| Emitter Cutoff Current<br>( $V_{BE} = 5.0\text{ Vdc}$ , $I_C = 0$ )   |                      | $I_{EBO}$      | –         | 2.0        | mAdc |

#### ON CHARACTERISTICS (Note 1)

|   |               |             |            |     |
|---|---------------|-------------|------------|-----|
| DC Current Gain<br>( $I_C = 5.0\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )<br>( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )                | $h_{FE}$      | 1000<br>250 | –<br>–     |     |
| Collector–Emitter Saturation Voltage<br>( $I_C = 5.0\text{ Adc}$ , $I_B = 10\text{ mAdc}$ )<br>( $I_C = 10\text{ Adc}$ , $I_B = 50\text{ mAdc}$ ) | $V_{CE(sat)}$ | –<br>–      | 2.0<br>3.0 | Vdc |
| Base–Emitter On Voltage<br>( $I_C = 10\text{ Adc}$ , $V_{CE} = 4.0\text{ Vdc}$ )  | $V_{BE(on)}$  | –           | 3.0        | Vdc |

#### SECOND BREAKDOWN (Note 2)

|  |                            |     |   |     |
|--|----------------------------|-----|---|-----|
| Second Breakdown Collector<br>Current with Base Forward Biased | $I_{S/b}$                  |     |   | Adc |
| BDW42  | $V_{CE} = 28.4\text{ Vdc}$ | 3.0 | – |     |
|  | $V_{CE} = 40\text{ Vdc}$   | 1.2 | – |     |
| BDW46/BDW47  | $V_{CE} = 22.5\text{ Vdc}$ | 3.8 | – |     |
|  | $V_{CE} = 36\text{ Vdc}$   | 1.2 | – |     |

#### DYNAMIC CHARACTERISTICS

|  |          |        |            |     |
|--|----------|--------|------------|-----|
| Magnitude of common emitter small signal short circuit current transfer ratio<br>( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ , $f = 1.0\text{ MHz}$ ) | $f_T$    | 4.0    | –          | MHz |
| Output Capacitance<br>( $V_{CB} = 10\text{ Vdc}$ , $I_E = 0$ , $f = 0.1\text{ MHz}$ )  | $C_{ob}$ | –<br>– | 200<br>300 | pF  |
| Small–Signal Current Gain<br>( $I_C = 3.0\text{ Adc}$ , $V_{CE} = 3.0\text{ Vdc}$ , $f = 1.0\text{ kHz}$ )   | $h_{fe}$ | 300    | –          |     |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Pulse Test: Pulse Width = 300  $\mu\text{s}$ , Duty Cycle = 2.0%.
2. Pulse Test non repetitive: Pulse Width = 250 ms.

# BDW42G (NPN), BDW46G, BDW47G (PNP)

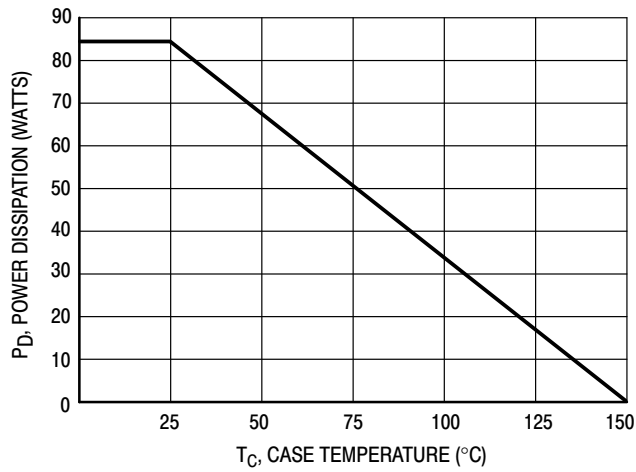


Figure 1. Power Temperature Derating Curve

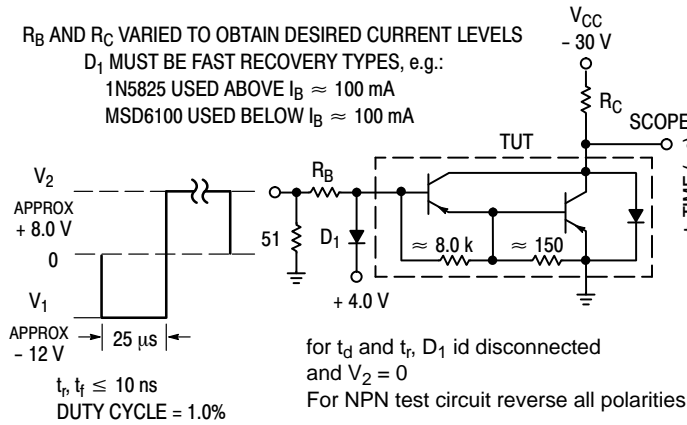


Figure 2. Switching Times Test Circuit

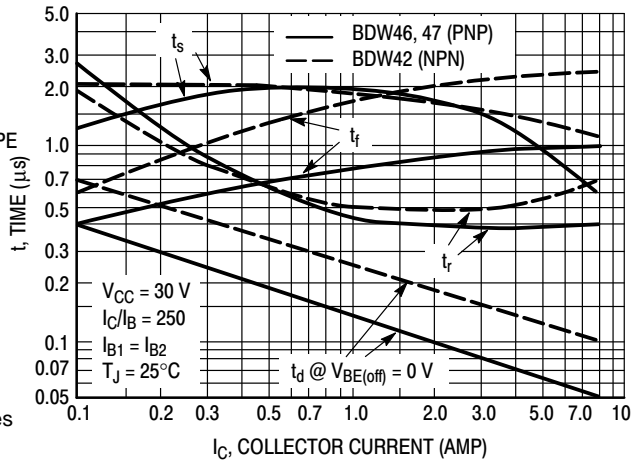


Figure 3. Switching Times

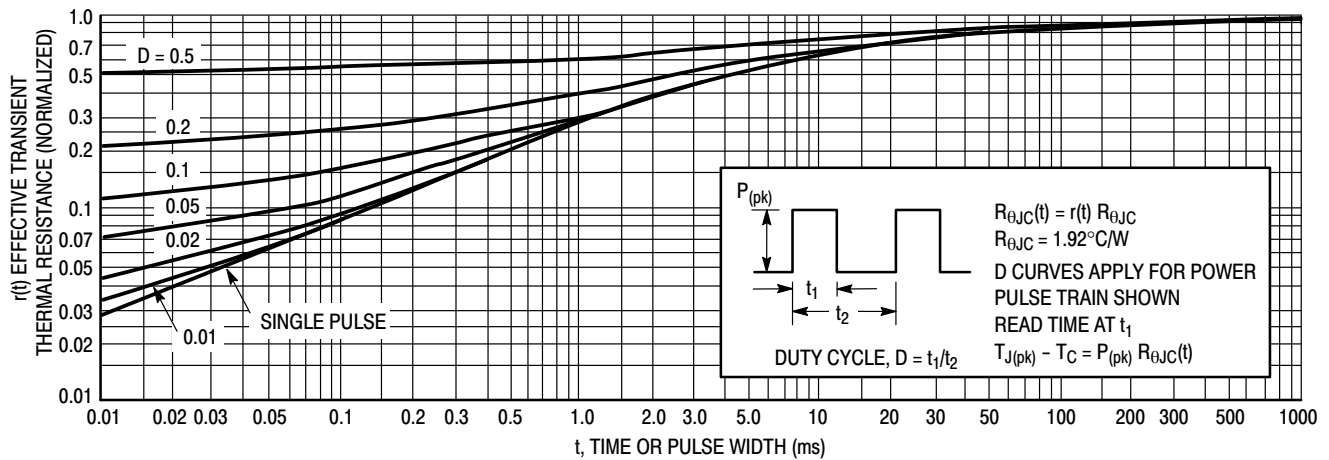


Figure 4. Thermal Response

# BDW42G (NPN), BDW46G, BDW47G (PNP)

## ACTIVE-REGION SAFE OPERATING AREA

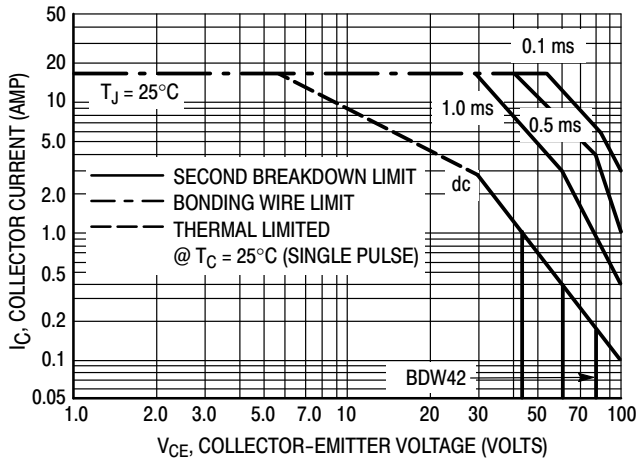


Figure 5. BDW42



Figure 6. BDW46 and BDW47

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate. The data of Figure 5 and 6 is based on  $T_{J(pk)} = 200^\circ\text{C}$ ;  $T_C$  is variable depending on conditions.

Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 200^\circ\text{C}$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

\*Linear extrapolation

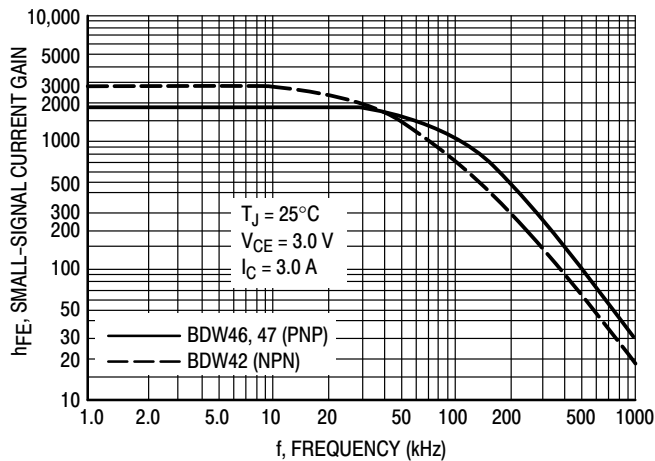


Figure 7. Small-Signal Current Gain

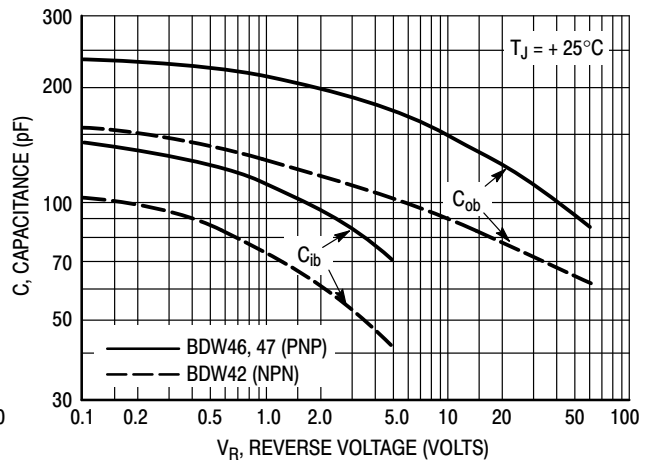
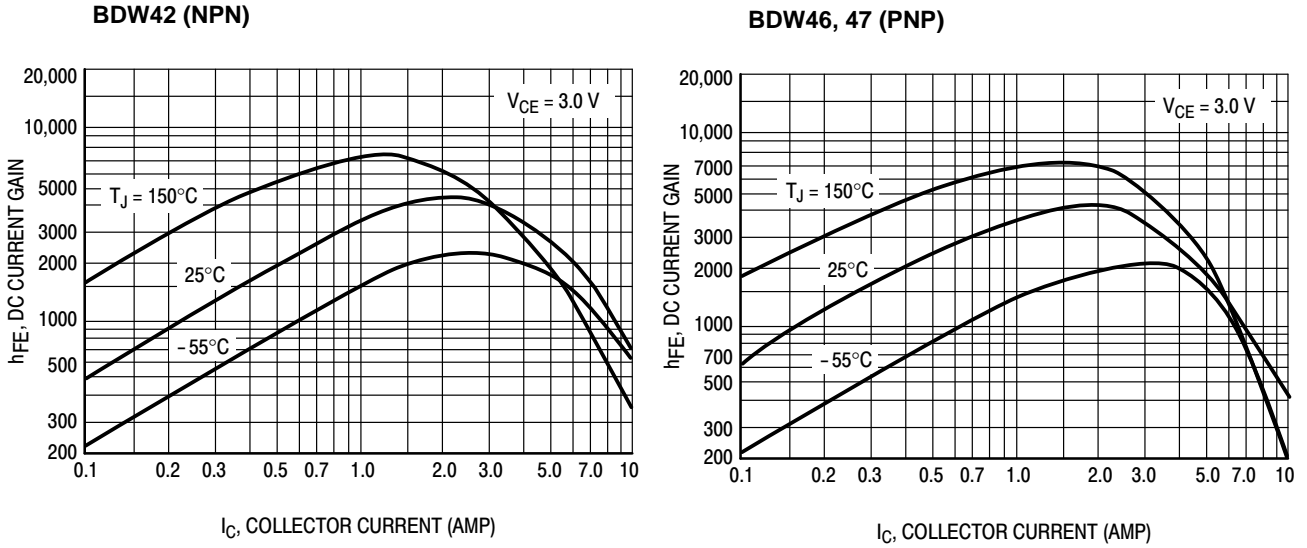
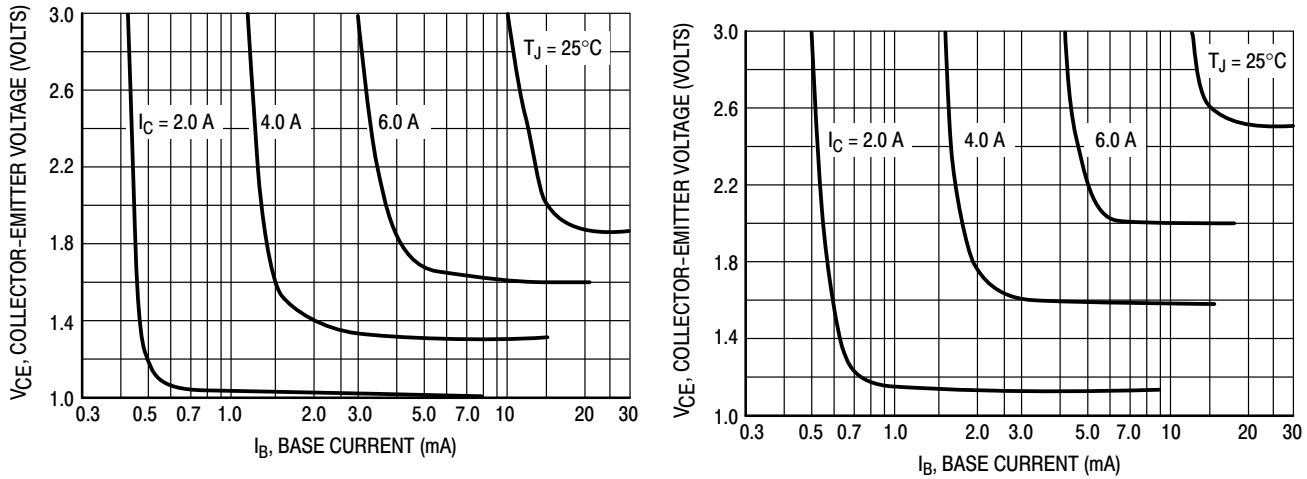


Figure 8. Capacitance

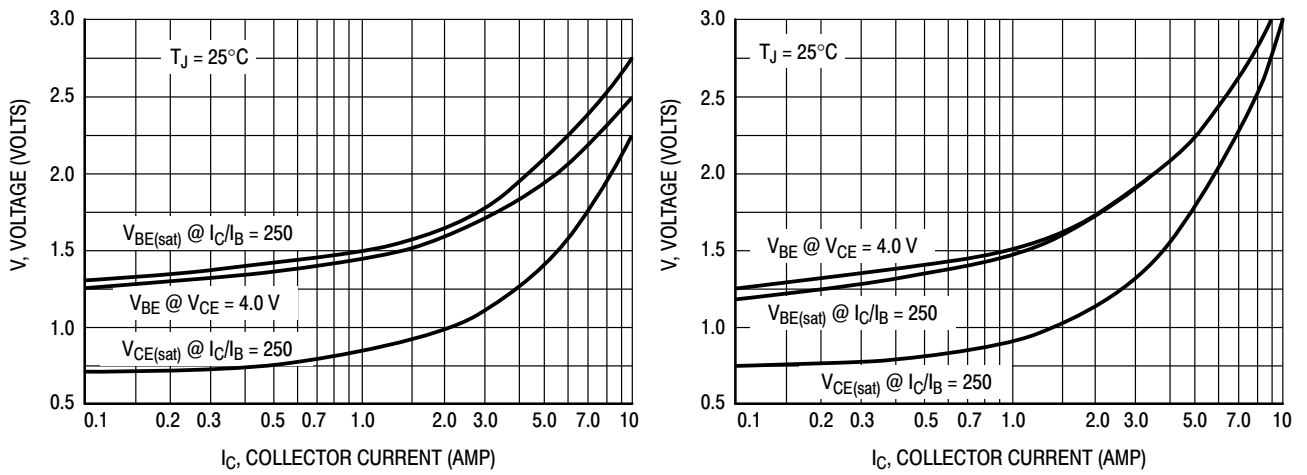
# BDW42G (NPN), BDW46G, BDW47G (PNP)



**Figure 9. DC Current Gain**



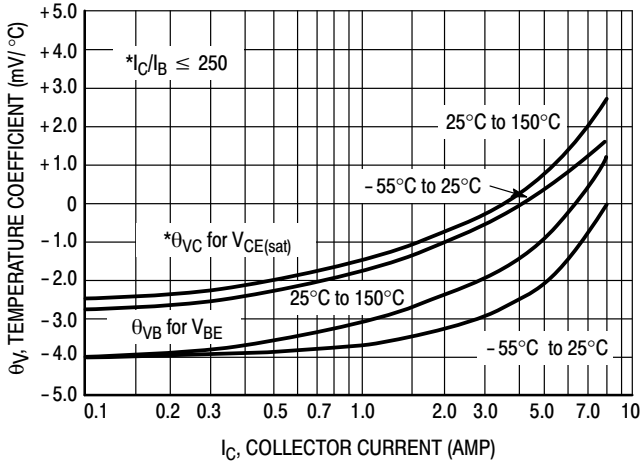
**Figure 10. Collector Saturation Region**



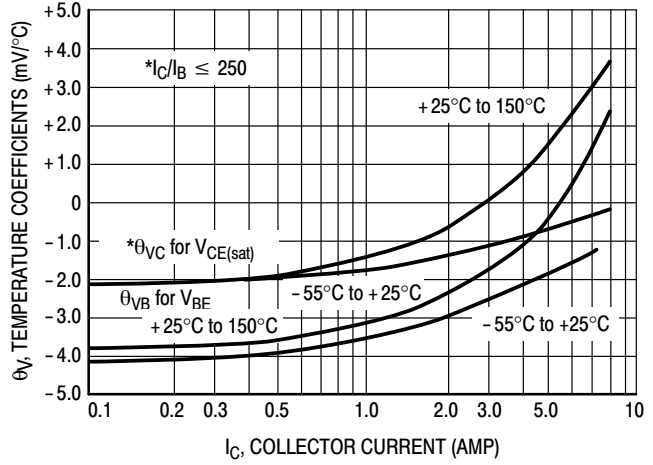
**Figure 11. "On" Voltages**

# BDW42G (NPN), BDW46G, BDW47G (PNP)

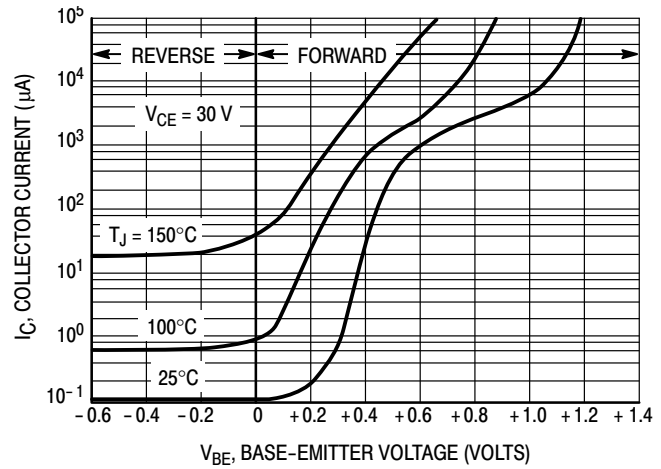
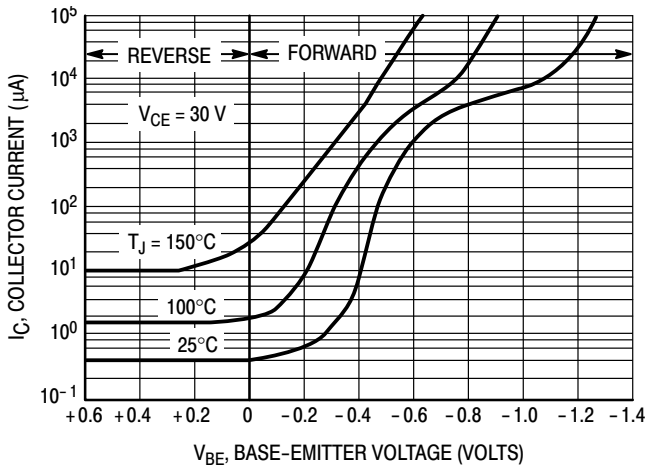
**BDW42 (NPN)**



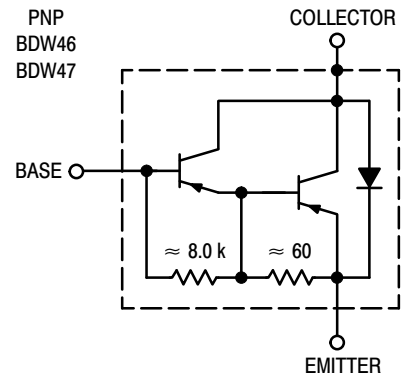
**BDW46, 47 (PNP)**



**Figure 12. Temperature Coefficients**

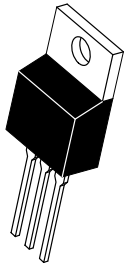


**Figure 13. Collector Cut-Off Region**



**Figure 14. Darlington Schematic**

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



SCALE 1:1



## TO-220 CASE 221A ISSUE AK

DATE 13 JAN 2022

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.
4. MAX WIDTH FOR F102 DEVICE = 1.35MM

| DIM | INCHES |       | MILLIMETERS |       |
|-----|--------|-------|-------------|-------|
|     | MIN.   | MAX.  | MIN.        | MAX.  |
| A   | 0.570  | 0.620 | 14.48       | 15.75 |
| B   | 0.380  | 0.415 | 9.66        | 10.53 |
| C   | 0.160  | 0.190 | 4.07        | 4.83  |
| D   | 0.025  | 0.038 | 0.64        | 0.96  |
| F   | 0.142  | 0.161 | 3.60        | 4.09  |
| G   | 0.095  | 0.105 | 2.42        | 2.66  |
| H   | 0.110  | 0.161 | 2.80        | 4.10  |
| J   | 0.014  | 0.024 | 0.36        | 0.61  |
| K   | 0.500  | 0.562 | 12.70       | 14.27 |
| L   | 0.045  | 0.060 | 1.15        | 1.52  |
| N   | 0.190  | 0.210 | 4.83        | 5.33  |
| Q   | 0.100  | 0.120 | 2.54        | 3.04  |
| R   | 0.080  | 0.110 | 2.04        | 2.79  |
| S   | 0.045  | 0.055 | 1.15        | 1.41  |
| T   | 0.235  | 0.255 | 5.97        | 6.47  |
| U   | 0.000  | 0.050 | 0.00        | 1.27  |
| V   | 0.045  | ---   | 1.15        | ---   |
| Z   | ---    | 0.080 | ---         | 2.04  |

STYLE 1:

- PIN 1. BASE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 2:

- PIN 1. BASE
- 2. EMITTER
- 3. COLLECTOR
- 4. EMITTER

STYLE 3:

- PIN 1. CATHODE
- 2. ANODE
- 3. GATE
- 4. ANODE

STYLE 4:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. MAIN TERMINAL 2

STYLE 5:

- PIN 1. GATE
- 2. DRAIN
- 3. SOURCE
- 4. DRAIN

STYLE 6:

- PIN 1. ANODE
- 2. CATHODE
- 3. ANODE
- 4. CATHODE

STYLE 7:

- PIN 1. CATHODE
- 2. ANODE
- 3. CATHODE
- 4. ANODE

STYLE 8:

- PIN 1. CATHODE
- 2. ANODE
- 3. EXTERNAL TRIP/DELAY
- 4. ANODE

STYLE 9:

- PIN 1. GATE
- 2. COLLECTOR
- 3. EMITTER
- 4. COLLECTOR

STYLE 10:

- PIN 1. GATE
- 2. SOURCE
- 3. DRAIN
- 4. SOURCE

STYLE 11:

- PIN 1. DRAIN
- 2. SOURCE
- 3. GATE
- 4. SOURCE

STYLE 12:

- PIN 1. MAIN TERMINAL 1
- 2. MAIN TERMINAL 2
- 3. GATE
- 4. NOT CONNECTED

|                  |             |  |
|------------------|-------------|--|
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