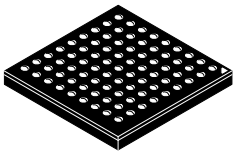
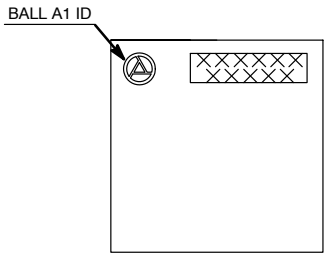
High-Dynamic Range (HDR) Image Signal Processor (ISP)

AP0101CS



VFBGA81, 6.5x6.5
CASE 138AG

MARKING DIAGRAM



XXXXXXXXXXX = Laser Marking

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

General Description

The **onsemi** AP0101CS is a high−performance, ultra−low power in−line, digital image processor optimized for use with High Dynamic Range (HDR) sensors. The AP0101CS provides full auto−functions support (AWB and AE) and Adaptive Local Tone Mapping (ALTM) to enhance HDR images and advanced noise reduction which enables excellent low−light performance.

Table 1. KEY PERFORMANCE PARAMETERS

Parameter	Value	
Primary camera interface	Parallel	
Primary camera input format	RAW12 Linear/Companded Bayer data	
Output interface	Up to 20−bit Parallel (Note 1)	
Output format	YUV422 8−bit, 10−bit, and SMPTE296M 10−, 12−bit tone−mapped Bayer	
Maximum resolution	1280 x 960 (1.2 Mp)	
Input clock range (Note 2)	6−30 MHz	
Maximum frame rate (Note 3)	45 fps at 1.2 Mp, 60 fps at 720 p	
Maximum output clock frequency	Parallel clock up to 84 MHz	
Supply voltage	V_{DD}IO_S	1.8 or 2.8 V nominal
	V_{DD}IO_H	2.5 or 3.3 V nominal
	V_{DD}_REG	1.8 V nominal
	V_{DD}IO_OTPM	2.5 or 3.3 V nominal
Operating temperature (ambient − T_A)	−30°C to + 70°C	
Typical power consumption (Note 4)	130 mW	

1. 20−bit in one pixel clock format is only available in SMPTE mode with the use of four GPIOs.
2. With input clock below 10 MHz, the two wire serial interface is supported only up to 100 KHz.
3. Maximum frame rate depends on output interface and data format configuration used.
4. 720 p HDR 60 fps 74.25 MHz YCbCr_422_16

Features

- Supports **onsemi** sensors with up to 1.2 Mp (1280 x 960)
- 45 fps at 1.2 Mp, 60 fps at 720 p
- Optimized for operation with HDR sensors
- Color and gamma correction
- Auto exposure, auto white balance, 50/60 Hz flicker avoidance
- Adaptive Local Tone Mapping (ALTM)
- Test Pattern Generator
- Two−wire serial programming interface
- Interface to low−cost Flash or EPROM through SPI bus (to configure and load patches)
- High−level host command interface
- Standalone operation supported
- Up to 5 GPIO
- Fail−safe IO
- Multi−Camera synchronization support
- Dual Band IR filter support

Applications

- SMPTE296 HDCCTV cameras
- Surveillance network IP cameras

ORDERING INFORMATION

Table 2. AVAILABLE PART NUMBERS

Part Number	Product Description	Orderable Product Attribute Description
AP0101CS2L00SPGA0−DR1	1Mp Co−Processor, 100−ball VFBGA	Drypack
AP0101CS2L00SPGAD3−GEVK	AP0101CS Demo Kit	
AP0101CS2L00SPGAH−GEVB	AP0101CS Head Board	

5. See the **onsemi** Device Nomenclature document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

FUNCTIONAL OVERVIEW

Figure 1 shows the typical configuration of the AP0101CS in a camera system. On the host side, a two−wire serial interface is used to control the operation of the AP0101CS, and image data is transferred using the parallel bus between the AP0101CS and the host. The AP0101CS interface to the sensor also uses a parallel interface.

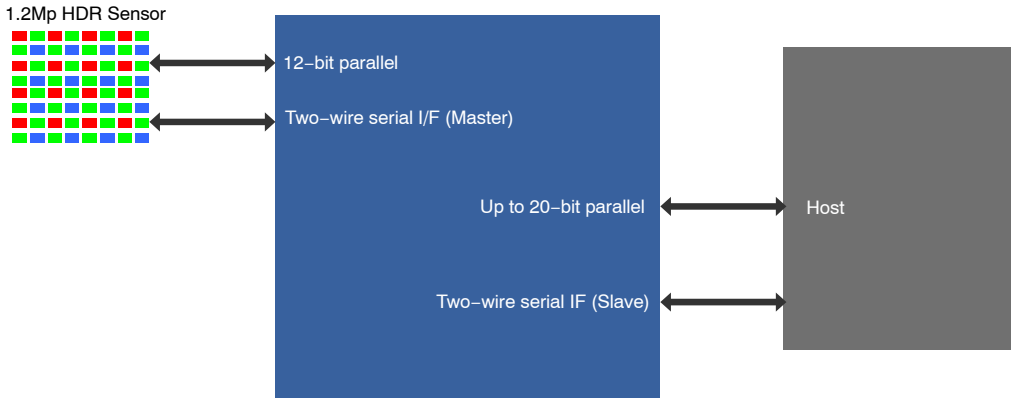
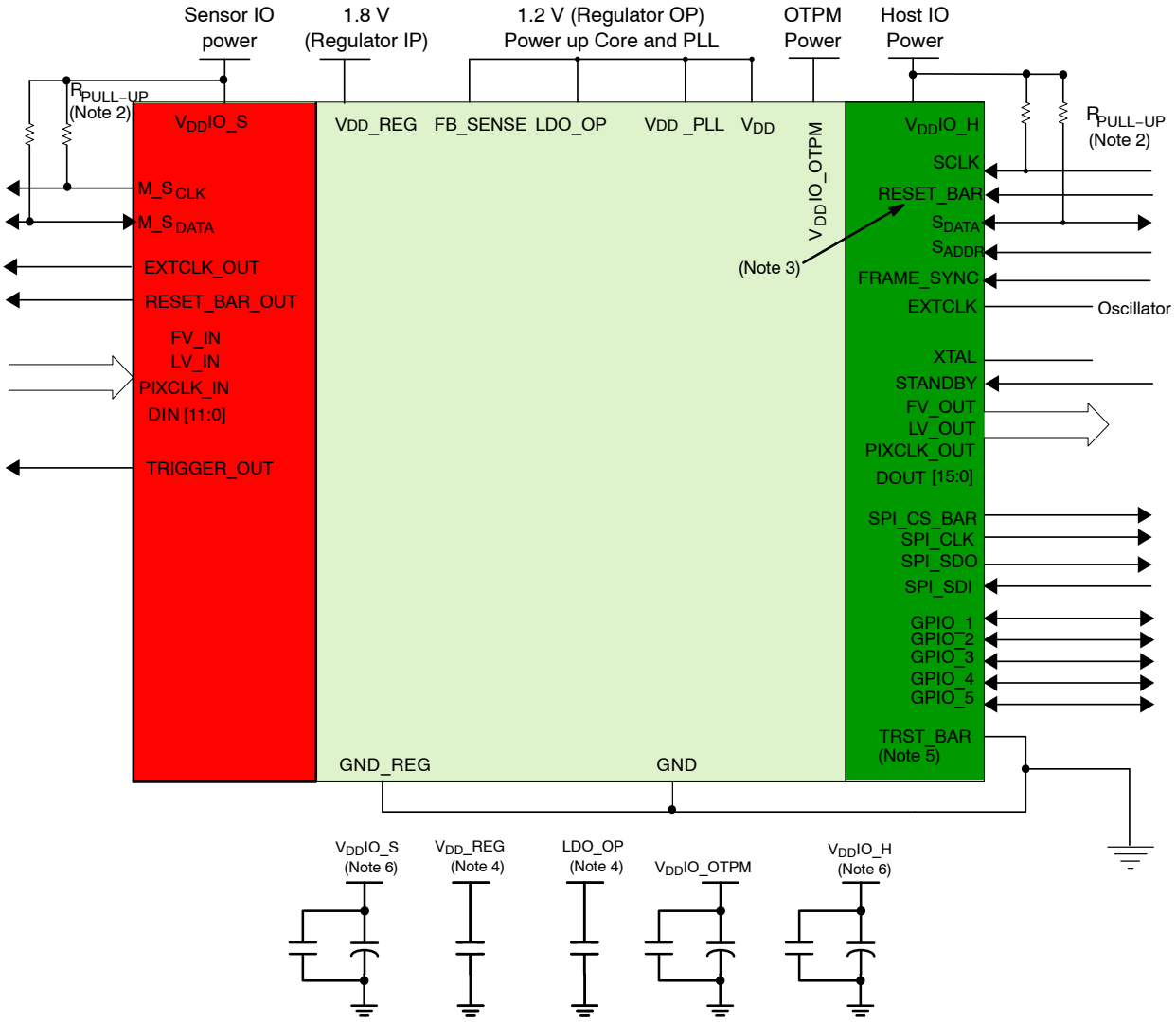


Figure 1. AP0101CS Connectivity

SYSTEM INTERFACES

Figure 2 shows typical AP0101CS device connections. All power supply rails must be decoupled from ground using capacitors as close as possible to the package. The AP0101CS signals to the sensor and host interfaces can be at different supply voltage levels to optimize power consumption and maximize flexibility. Table 4 provides the signal descriptions for the AP0101CS.



1. This typical configuration shows only one scenario out of multiple possible variations for this sensor.
2. **onsemi** recommends a 1.5 kΩ resistor value for the two−wire serial interface $R_{PULL-UP}$; however, greater values may be used for slower transmission speed.
3. RESET_BAR has an internal pull−up resistor and can be left floating if not used.
4. The decoupling capacitors for the regulator input and output should have a value of 1.0 μF. The capacitors should be ceramic and need to have X5R or X7R dielectric.
5. TRST_BAR connects to GND for normal operation.
6. **onsemi** recommends that 0.1 μF and 1 μF decoupling capacitors for each power supply are mounted as close as possible to the pin. Actual values and numbers may vary depending on layout and design consideration.

Figure 2. Typical Configuration

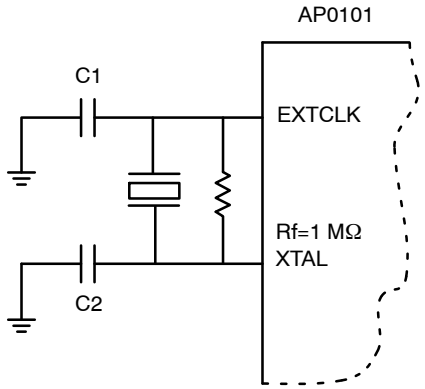
The following table summarizes the key signals when using the internal regulator. (The internal regulator has to be used for AP0101AT.)

Table 3. KEY SIGNALS WHEN USING THE REGULATOR

Signal Name	Internal Regulator
V_{DD}_REG	1.8 V
FB_SENSE	1.2 V (input)
LDO_OP	1.2 V (output)

Crystal Usage

As an alternative to using an external oscillator, a crystal may be connected between EXTCLK and XTAL. Two small loading capacitors and a feedback resistor should be added, as shown in Figure 3.



NOTE: Rf represents the feedback resistor, an Rf value of 1 MΩ would be sufficient for AP0101CS. C1 and C2 are decided according to the crystal or resonator CL specification. In the steady state of oscillation, CL is defined as (C1 x C2)/(C1+C2). In fact, the I/O ports, the bond pad, package pin and PCB traces all contribute the parasitic capacitance to C1 and C2. Therefore, CL can be rewritten to be (C1* x C2*)/(C1*+C2*), where C1*=(C1+Cin, stray) and C2*=(C2+Cout, stray). The stray capacitance for the IO ports, bond pad and package pin are known which means the formulas can be rewritten as C1*=(C1+1.5pF+Cin, PCB) and C2*=(C2+1.3pF+Cout, PCB).

Figure 3. Using a Crystal Instead of External Oscillator

Table 4. PIN DESCRIPTIONS

Name	Type	Description
EXTCLK	Input	Master input clock, nominally 27 MHz. This can either be a square−wave generated from an oscillator (in which case the XTAL input must be left unconnected) or direct connection to a crystal.
XTAL	Output	If EXTCLK is connected to one pin of a crystal, this signal is connected to the other pin, otherwise this signal must be left unconnected.
RESET_BAR	Input/PU	Master reset signal, active LOW. This signal has an internal pull up.
S_{CLK}	Input	Two−wire serial interface clock (host interface).
S_{DATA}	Input/Output	Two−wire serial interface data (host interface).
S_{ADDR}	Input	Selects device address for the two−wire slave serial interface. When connected to GND, the device ID is 0x90. When wired to V_{DD}IO_H, a device ID of 0xBA is selected.
FRAME_SYNC	Input	This input can be used to set the output timing of the AP0101CS. This signal should be connected to GND if not used.
STANDBY	Input	Standby mode control, active HIGH.
SPI_S_{CLK}	Output	Clock output for interfacing to an external SPI flash or EEPROM memory
SPI_SDI	Input	Data in from SPI flash or EEPROM memory. When no SPI device is fitted, this signal is used to determine whether the AP0101CS should auto−configure: 0: Do not auto−configure; two−wire interface will be used to configure the device (host−config mode) 1: Auto−configure. This signal has an internal pull−up resistor
SPI_SDO	Output	Data out to SPI flash or EEPROM memory
SPI_CS_BAR	Output	Chip select out to SPI flash or EEPROM memory.
FV_OUT	Output	Host frame valid output (synchronous to PIXCLK_OUT).
LV_OUT	Output	Host line valid output (synchronous to PIXCLK_OUT).
PIXCLK_OUT	Output	Host pixel clock output.
DOUT [15:0]	Output	Host pixel data output (synchronous to PIXCLK_OUT) DOUT[15:0]. Note 20−bit output (SMPTE) also uses GPIO[5:2].
GPIO [5:1]	I/O	General purpose digital I/O. Note: 20−bit output (SMPTE) also uses GPIO[5:2]
TRST_BAR	Input	Must be tied to GND in normal operation.

Table 4. PIN DESCRIPTIONS (continued)

Name	Type	Description
EXT_CLK_BAR	Output	Clock to external sensor.
RESET_BAR_OUT	Output	Reset signal to external sensor.
M_S_{CLK}	Output	Two−wire serial interface interface clock (Master).
M_S_{DATA}	I/O	Two−wire serial interface interface clock (Master).
FV_IN	Input	Sensor frame valid input.
LV_IN	Input	Sensor line valid input.
PIXCLK_IN	Input	Sensor pixel clock output.
DIN [11:0]	Input	Sensor pixel data input D_{IN} [11:0].
TRIGGER_OUT	Output	Trigger signal for external sensor.
$V_{DD}IO\_S$	Supply	Sensor I/O power supply.
GND	Supply	Ground for sensor IO, host IO, PLL, $V_{DD}IO\_OTPM$, and V_{DD}.
V_{DD}_REG	Supply	Input to on−chip 1.8 V to 1.2 V regulator.
LDO_OP	Output	Output from on−chip 1.8 V to 1.2 V regulator. Note: The regulator on the AP0101CS must be used.
FB_SENSE	Input	On−chip regulator sense signal.
GND_REG	Supply	Ground for on−chip regulator.
V_{DD}_PLL	Supply	PLL supply.
V_{DD}	Supply	Core supply.
$V_{DD}IO\_OTPM$	Supply	OTPM power supply.
$V_{DD}IO\_H$	Supply	Host I/O power Supply.

Table 5. PACKAGE PINOUT

	1	2	3	4	5	6	7	8	9
A	EXTCLK	XTAL	S_{CLK}	SPI_SDO	$D_{OUT}[15]$	$D_{OUT}[13]$	$D_{OUT}[10]$	$D_{OUT}[9]$	$D_{OUT}[8]$
B	V_{DD}	$V_{DD}IO\_H$	S_{DATA}	SPI_SDI	$D_{OUT}[14]$	$D_{OUT}[12]$	$D_{OUT}[11]$	$D_{OUT}[7]$	$D_{OUT}[6]$
C	EXT_CLK _OUT	$V_{DD}IO\_S$	S_{ADDR}	SPI_CS_BAR	GND	PIXCLK _OUT	FV_OUT	$D_{OUT}[5]$	$D_{OUT}[4]$
D	RESET_BAR _OUT	V_{DD}	GND	SPI_SCLK	GND	TRST_BAR	LV_OUT	$D_{OUT}[3]$	$D_{OUT}[2]$
E	$D_{IN}[3]$	$D_{IN}[7]$	GND	FB_SENSE	GND	GND	V_{DD}_PLL	$D_{OUT}[1]$	$D_{OUT}[0]$
F	$D_{IN}[11]$	$D_{IN}[2]$	LDO_OP	GND_REG	GND	GND	V_{DD}_PLL	V_{DD}_PLL	$V_{DD}IO$ _OTPM
G	$D_{IN}[6]$	$D_{IN}[1]$	$D_{IN}[4]$	V_{DD}_REG	$V_{DD}IO\_S$	V_{DD}	RESET_BAR	GPIO[4]	GPIO[5]
H	$D_{IN}[10]$	$D_{IN}[0]$	$D_{IN}[8]$	FV_IN	M_S_{DATA}	$V_{DD}IO\_H$	FRAME _SYNC	GPIO[2]	GPIO[3]
J	$D_{IN}[5]$	$D_{IN}[9]$	PIXCLK_IN	LV_IN	M_S_{CLK}	V_{DD}	STANDBY	TRIGGER _OUT	GPIO[1]

Power−Up and Down Sequence

Powering up and down the AP0101CS requires voltages to be applied in a particular order, as seen in Figure 4. The timing requirements are shown in Table 6. The AP0101CS includes a power−on reset feature that initiates a reset upon power up of the AP0101CS.

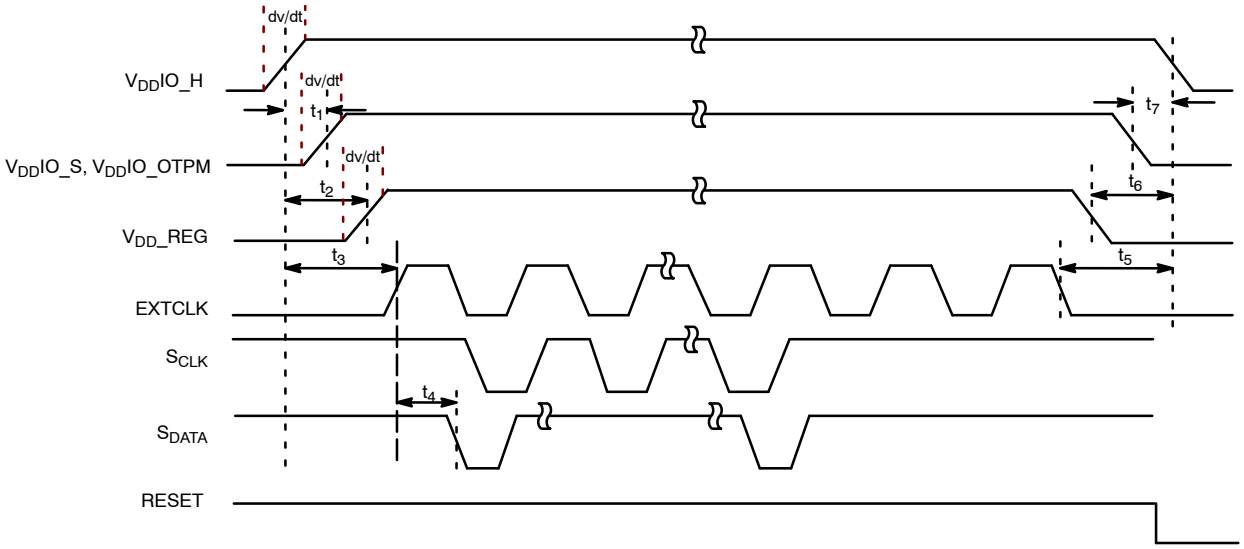


Figure 4. Power−Up and Power−Down Sequence

Table 6. POWER−UP AND POWER−DOWN SIGNAL TIMING

Symbol	Parameter	Min	Typ	Max	Unit
t1	Delay from V_{DD}IO_H to V_{DD}IO_S, V_{DD}IO_OTPM	0	−	50	ms
t2	Delay from V_{DD}IO_H to V_{DD}_REG	0	−	50	ms
t3	EXTCLK activation	t2+1	−	−	ms
t4	First serial command	100	−	−	EXTCLK cycles
t5	EXTCLK cutoff	t6	−	−	ms
t6	Delay from V_{DD}_REG to V_{DD}IO_H	0	−	50	ms
t7	Delay from V_{DD}IO_S, V_{DD}IO_OTPM to V_{DD}IO_H	0	−	50	ms
dv/dt	Power supply ramp time (slew rate)	−	−	0.1	V/μs

6. If the system cannot support this power supply slew rate, then power supplies must be designed to overcome inrush currents in Table 25.

Reset

The AP0101CS has three types of reset available:

- A hard reset is issued by toggling the RESET_BAR signal.
- A soft reset is issued by writing commands through the two−wire serial interface.
- An internal power−on reset.

Table 7 shows the output states when the part is in various states.

Table 7. OUTPUT STATES

Name	Hardware States		Firmware States				Notes
	Reset State	Default State	Hard Standby	Soft Standby	Streaming	Idle	
EXTCLK	(clock running or stopped)	(clock running)	(clock running or stopped)	(clock running)	(clock running)	(clock running)	Input
XTAL	n/a	n/a	n/a	n/a	n/a	n/a	Input
RESET_BAR	(asserted)	(negated)	(negated)	(negated)	(negated)	(negated)	Input

Table 7. OUTPUT STATES (continued)

Name	Hardware States		Firmware States				Notes
	Reset State	Default State	Hard Standby	Soft Standby	Streaming	Idle	
S_{CLK}	n/a	n/a	(clock running or stopped)	(clock running or stopped)	(clock running or stopped)	(clock running or stopped)	Input. Must always be driven to a valid logical level.
S_{DATA}	High−impedance	High−impedance	High−impedance	High−impedance	High−impedance	High−impedance	Input/Output. A valid logic level should be established by pull−up.
S_{ADDR}	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logical level.
FRAME_SYNC	n/a	n/a	n/a	n/a	n/a	n/a	Input. Must always be driven to a valid logical level.
STANDBY	n/a	(negated)	(negated)	(negated)	(negated)	(negated)	Input. Must always be driven to a valid logical level.
SPI_SCLK	High−impedance	driven, logic 0	driven, logic 0	driven, logic 0			Output
SPI_SDI	Internal pull−up enabled	Internal pull−up enabled	Internal pull−up enabled	Internal pull−up enabled			Input. Internal pull−up permanently enabled.
SPI_SDO	High−impedance	driven, logic 0	driven, logic 0	driven, logic 0			Output
SPI_CS_BAR	High−impedance	driven, logic 1	driven, logic 1	driven, logic 1			Output
EXT_CLK _OUT	driven, logic 0	driven, logic 0	driven, logic 0	driven, logic 0			Output
RESET_BAR _OUT	driven, logic 0	driven, logic 0	driven, logic 1	driven, logic 1			Output. Firmware will release sensor reset.
M_S_{CLK}	High−impedance	High−impedance	High−impedance	High−impedance			Input/Output. A valid logic level should be established by pull−up.
M_S_{DATA}	High−impedance	High−impedance	High−impedance	High−impedance			Input/Output. A valid logic level should be established by pull−up.
FV_IN, LV_IN, PIXCLK_IN, DIN [11:0]	n/a	n/a	n/a	n/a		n/a	Input. Must always be driven to a valid logical level.
FV_OUT, LV_OUT, PIXCLK_OUT, DOUT [15:0]	High−impedance	Varied	Driven if used	Driven if used	Driven if used	Driven if used	Output. Default state dependent on configuration.
TX_CLK, RX_CLK, GTX_CLK	High−impedance	Varied	Driven if used	Driven if used	Driven if used	Driven if used	Output. Default state dependent on configuration
GPIO[5:2]	High−impedance	Input, then high−impedance	Driven if used	Driven if used	Driven if used	Driven if used	Input/Output. After reset these pins are sampled as inputs as part of auto−configuration.
GPIO1	High−impedance	High−impedance	High−impedance	High−impedance	High−impedance	High−impedance	
TRIGGER _OUT	High−impedance	High−impedance	Driven if used	Driven if used	Driven if used	Driven if used	
TRST_BAR	n/a	n/a	(negated)	(negated)	(negated)	(negated)	Input. Must always be driven to a valid logic level.

Hard Reset

The AP0101CS enters the reset state when the external RESET_BAR signal is asserted LOW, as shown in Figure 5. All the output signals will be in High−Z state.

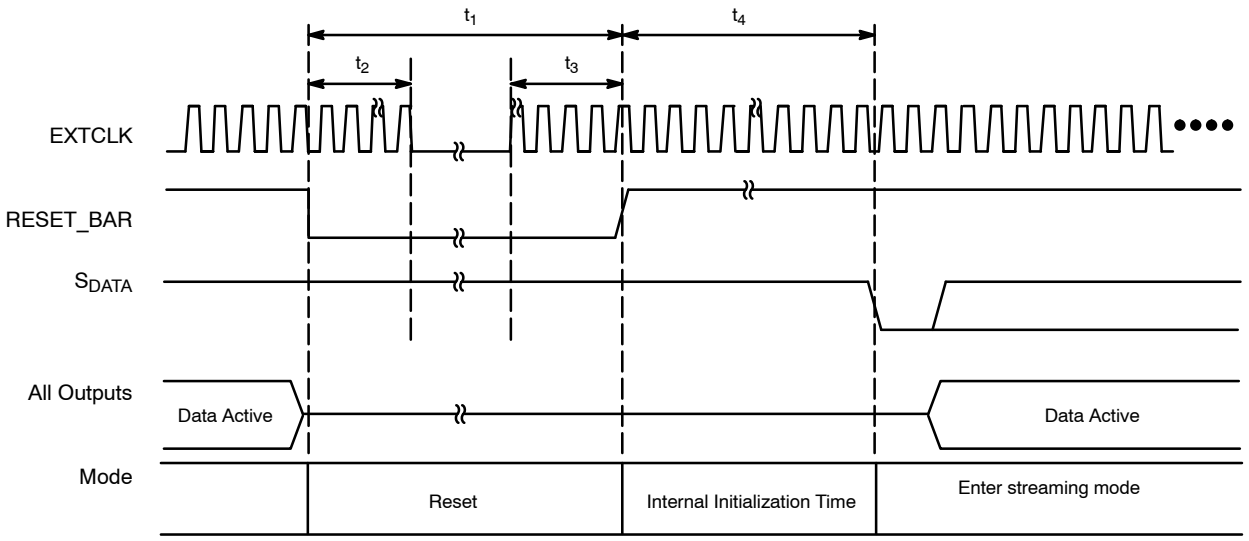


Figure 5. Hard Reset Operation

Table 8. HARD RESET

Symbol	Parameter	Min	Typ	Max	Unit
t_1	RESET_BAR pulse width	50	–	–	EXTCLK cycles
t_2	Active EXTCLK required after RESET_BAR asserted	10	–	–	
t_3	Active EXTCLK required before RESET_BAR de−asserted	10	–	–	
t_4	First two−wire serial interface communication after RESET_BAR is HIGH	100	–	–	

Soft Reset

A soft reset sequence to the AP0101CS can be activated by writing to a register through the two−wire serial interface.

Hard Standby Mode

The AP0101CS can enter hard standby mode by using the external STANDBY signal, as shown in Figure 6.

Entering Standby Mode

1. Assert STANDBY signal HIGH.

Exiting Standby Mode

1. De−assert STANDBY signal LOW.

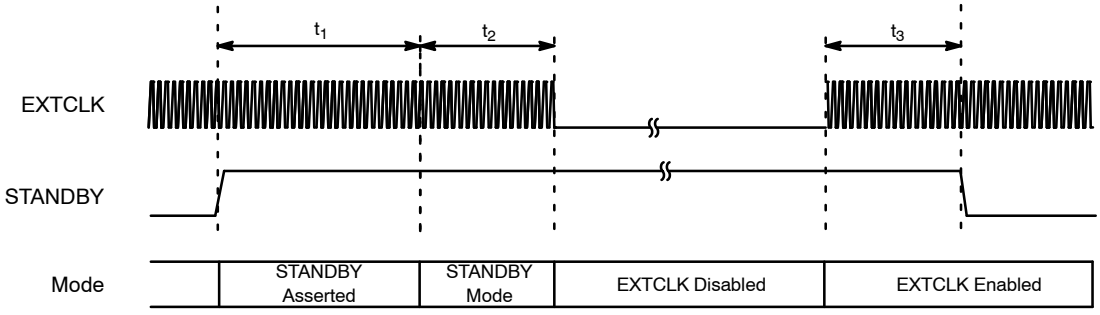


Figure 6. Hard Standby Operation

Table 9. HARD STANDBY SIGNAL TIMING

Symbol	Parameter	Min	Typ	Max	Unit
t_1	Standby entry complete	–	–	2 Frames	Lines
t_2	Active EXTCLK required after going into STANDBY mode	10	–	–	EXTCLKs
t_3	Active EXTCLK required before STANDBY de−asserted	10	–	–	EXTCLKs

MULTI−CAMERA SYNCHRONIZATION SUPPORT

The AP0101CS supports multi−camera synchronization via the FRAME_SYNC pin. The host (or controlling entity) 'broadcasts' a sync−pulse to all cameras within the system that triggers streaming start. The AP0101CS will propagate the signal to the TRIGGER_OUT pin to the sensor's TRIGGER pin.

The AP0101CSsupports two different trigger modes. The first mode supported is 'single−shot'; this is when the trigger pulse will cause one frame to be output from the image sensor and AP0101CS (see Figure 7).

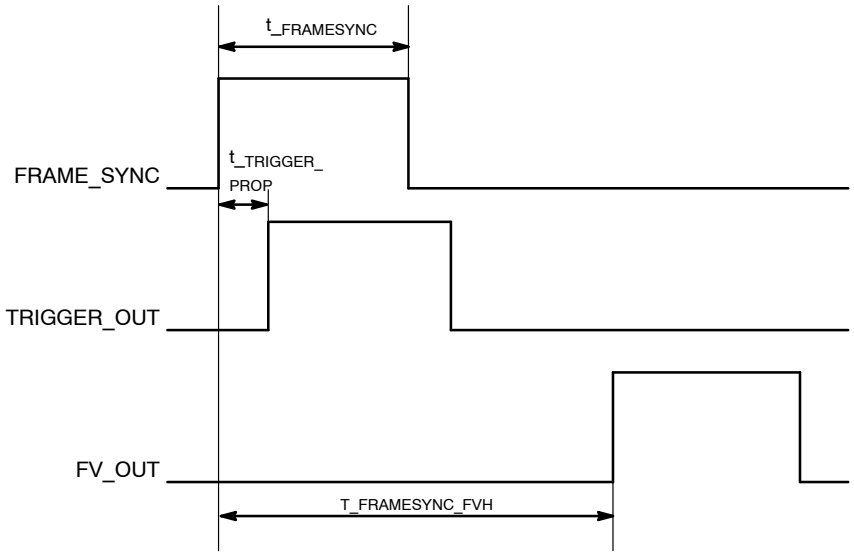
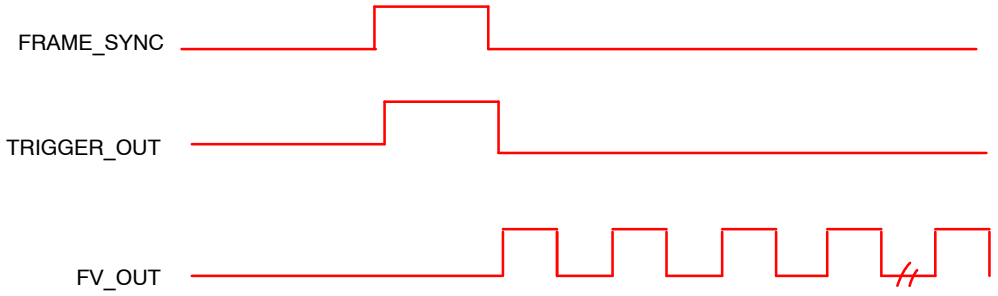


Figure 7. Single−Shot Mode

Table 10. TRIGGER TIMING

Parameter	Name	Conditions	Min	Typ	Max	Unit
FRAME_SYNC to FV_OUT	$t_{FRMSYNC\_FVH}$		8 lines + exposure time + sensor delay	–	–	Lines
FRAME_SYNC to TRIGGER_OUT	$t_{TRIGGER\_PROP}$		–	–	9	ns
t_{FRAME_SYNC}	t_{FRAME_SYNC}		3	–	–	EXTCLK cycles

The second mode supported is called 'continuous'; this is when a trigger pulse will cause the part to continuously output frames, see Figure 8. This mode would be especially useful for applications which have multiple sensors and need to have their video streams synchronized (for example, surround view or panoramic view applications).



NOTE: This diagram is not to scale.

Figure 8. Continuous Mode

When two or more cameras have a signal applied to the FRAME_SYNC input at the same time, the respective FV_OUT signals would be synchronized within five PIXCLK_OUT cycles. This assumes that all cameras have the same configuration settings and that the exposure time is the same.

IMAGE FLOW PROCESSOR

Image and color processing in the AP0101CS is implemented as an image flow processor (IFP) coded in hardware logic. During normal operation, the embedded microcontroller will automatically adjust the operating parameters. For normal operation of the AP0101CS, a stream of raw image data from the attached image sensor is fed into the color pipeline. The user also has the option to select a number of test patterns to be input instead of sensor data. The test pattern is fed to the IFP for testing the image pipeline without sensor operation.

The test patterns can be selected by programming variables. To select enter test pattern mode, set R0xC88F to 0x02 and issue a Change−Config request; to exit this mode, set R0xC88F to 0x00.

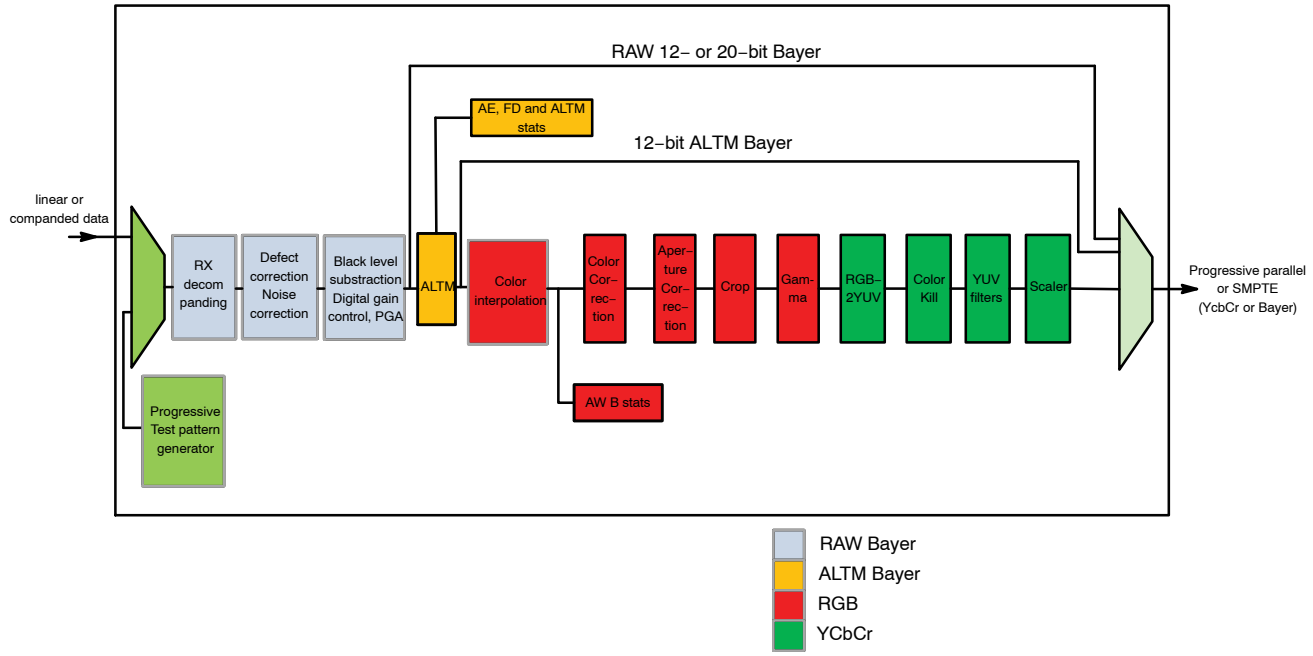
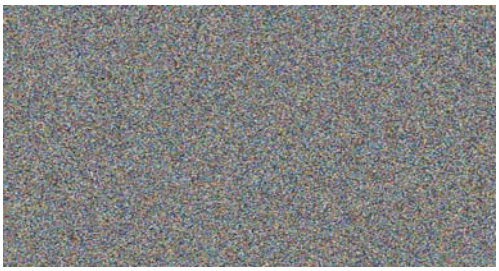
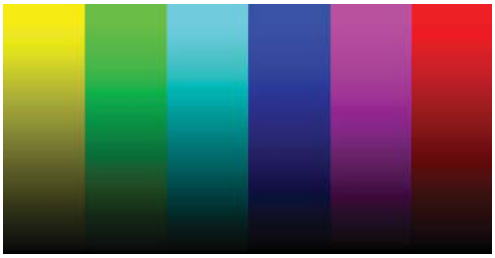
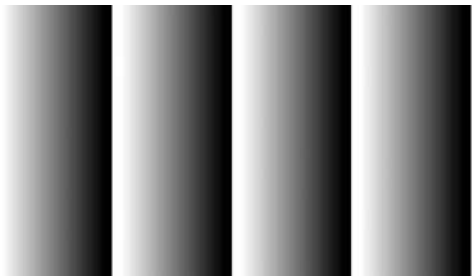


Figure 9. Continuous Mode

Test Patterns

Table 11. TRIGGER TIMING

Test Pattern	Example
FLAT FIELD FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x01 FIELD_WR= CAM_MODE_TEST_PATTERN_RED, 0x000FFFFF FIELD_WR= CAM_MODE_TEST_PATTERN_GREEN, 0x000FFFFF FIELD_WR= CAM_MODE_TEST_PATTERN_BLUE, 0x000FFFFF Load = Change−Config Changing the values in R0xC890−R0xC898 will change the color of the test pattern.	
100% Color Bar FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x02 Load = Change−Config	
Pseudo−Random FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x05 Load = Change−Config	
Fade−to−Gray FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x08 Load = Change−Config	
Linear Ramp FIELD_WR= CAM_MODE_SELECT, 0x02 FIELD_WR= CAM_MODE_TEST_PATTERN_SELECT, 0x09 Load = Change−Config	

Defect Correction

After data decompanding the image stream processing starts with defect correction.

To obtain defect free images, the pixels marked defective during sensor readout and the pixels determined defective by the defect correction algorithms are replaced with values derived from the non−defective neighboring pixels. This image processing technique is called defect correction.

AdaCD (Adaptive Color Difference)

Automotive applications require good performance in extremely low light, even at high temperature conditions. In these stringent conditions the image sensor is prone to higher noise levels, and so efficient noise reduction techniques are required to circumvent this sensor limitation and deliver a high quality image to the user.

The AdaCD Noise Reduction Filter is able to adapt its noise filtering process to local image structure and noise level, removing most objectionable color noise while preserving edge details.

Black Level Subtraction and Digital Gain

After noise reduction, the pixel data goes through black level subtraction and multiplication of all pixel values by a programmable digital gain. Independent color channel digital gain can be adjusted with registers. Black level subtract (to compensate for sensor data pedestal) is a single value applied to all color channels. If the black level subtraction produces a negative result for a particular pixel, the value of this pixel is set to 0.

Positional Gain Adjustments (PGA)

Lenses tend to produce images whose brightness is significantly attenuated near the edges. There are also other factors causing fixed pattern signal gradients in images captured by image sensors. The cumulative result of all these factors is known as image shading. The AP0101CS has an embedded shading correction module that can be programmed to counter the shading effects on each individual R, Gb, Gr, and B color signal.

The correction functions

The correction functions can then be applied to each pixel value to equalize the response across the image as follows:

$$P_{corrected}(row, col) = P_{sensor}(row, col) \times f(row, col) \quad \text{(eq. 1)}$$

where P are the pixel values and f is the color dependent correction functions for each color channel.

Adaptive Local Tone Mapping (ALTM)

Real world scenes often have very high dynamic range (HDR) that far exceeds the electrical dynamic range of the imager. Dynamic range is defined as the luminance ratio between the brightest and the darkest object in a scene. In recent years many technologies have been developed to capture the full dynamic range of real world scenes. For example, the multiple exposure method is a widely adopted method for capturing high dynamic range images, which combines a series of low dynamic range images of the same scene taken under different exposure times into a single HDR image.

Even though the new digital imaging technology enables the capture of the full dynamic range, low dynamic range display devices are the limiting factor. Today's typical LCD monitor has contrast ratio around 1,000:1; however, it is not atypical for an HDR image having contrast ratio around 250,000:1. Therefore, in order to reproduce HDR images on a low dynamic range display device, the captured high dynamic range must be compressed to the available range of the display device. This is commonly called tone mapping.

Tone mapping methods can be classified into global tone mapping and local tone mapping. Global tone mapping methods apply the same mapping function to all pixels. While global tone mapping methods provide computationally simple and easy to use solutions, they often cause loss of contrast and detail. A local tone mapping is thus necessary in addition to global tone mapping for the reproduction of visually more appealing images that also reveal scene details that are important for automotive safety and surveillance applications. Local tone mapping methods use a spatially varying mapping function determined by the neighborhood of a pixel, which allows it to increase the local contrast and the visibility of some details of the image. Local methods usually yield more pleasing results because they exploit the fact that human vision is more sensitive to local contrast.

onsemi's ALTM solution significantly improves the performance over global tone mapping. ALTM is directly applied to the Bayer domain to compress the dynamic range from 20−bit to 12−bit. This allows the regular color pipeline to be used for HDR image rendering.

Color Interpolation

In the raw data stream fed by the sensor core to the IFP, each pixel is represented by a 20− or 12−bit integer number, which can be considered proportional to the pixel's response to a one−color light stimulus, red, green, or blue, depending on the pixel's position under the color filter array. Initial data processing steps, up to and including ALTM, preserve the one−color−per−pixel nature of the data stream, but after ALTM it must be converted to a three−colors−per−pixel stream appropriate for standard color processing. The conversion is done by an edge−sensitive color interpolation module. The module pads the incomplete color information available for each pixel with information extracted from an appropriate set of neighboring pixels. The algorithm used to select this set and extract the information seeks the best compromise between preserving edges and filtering out high frequency noise in flat field areas. The edge threshold can be set through register settings.

Color correction and aperture correction

To achieve good color fidelity of the IFP output, interpolated RGB values of all pixels are subjected to color correction. The IFP multiplies each vector of three pixel colors by a 3 x 3 color correction matrix. The three components of the resulting color vector are all sums of three 10−bit numbers. The color correction matrix can be either programmed by the user or automatically selected by the auto white balance (AWB) algorithm implemented in the IFP. Color correction should ideally produce output colors that are corrected for the spectral sensitivity and color crosstalk characteristics of the image sensor. The optimal values of the color correction matrix elements depend on those sensor characteristics and on the spectrum of light incident on the sensor. The color correction variables can be adjusted through register settings.

To increase image sharpness, a programmable 2D aperture correction (sharpening filter) is applied to

color−corrected image data. The gain and threshold for 2D correction can be defined through register settings.

Gamma Correction

The gamma correction curve is implemented as a piecewise linear function with 33 knee points, taking 12−bit arguments and mapping them to 10−bit output. The abscissas of the knee points are fixed at 0, 8, 16, 24, 32, 40, 48, 56, 64, 80, 96, 112, 128, 160, 192, 224, 256, 320, 384, 448, 512, 640, 768, 896, 1024, 1280, 1536, 1792, 2048, 2560, 3072, 3584, and 4096. The 10−bit ordinates are programmable through variables.

The AP0101CS has the ability to calculate the 33−point knee points based on the tuning of cam_ll_gamma and cam_ll_contrast_gradient_bright. The other method is for the host to program the 33 knee point curve themselves.

Also included in this block is a Fade−to Black curve which sets all knee points to zero and causes the image to go black in extreme low light conditions.

Color Kill

To remove high−or low−light color artifacts, a color kill circuit is included. It affects only pixels whose luminance exceeds a certain preprogrammed threshold. The U and V values of those pixels are attenuated proportionally to the difference between their luminance and the threshold.

YUV Color Filter

As an optional processing step, noise suppression by one−dimensional low−pass filtering of Y and/or UV signals is possible. A 3− or 5−tap filter can be selected for each signal.

CAMERA CONTROL AND AUTO FUNCTIONS

Auto Exposure

The auto exposure algorithm optimizes scene exposure to minimize clipping and saturation in critical areas of the image. This is achieved by controlling exposure time and analog gains of the sensor core as well as digital gains applied to the image.

The auto exposure module analyzes image statistics collected by the exposure measurement engine, makes a decision, and programs the sensor and color pipeline to achieve the desired exposure. The measurement engine subdivides the image into 25 windows organized as a 5 x 5 grid.

W 0,0	W 0,1	W 0,2	W 0,3	W 0,4
W 1,0	W 1,1	W 1,2	W 1,3	W 1,4
W 2,0	W 2,1	W 2,2	W 2,3	W 2,4
W 3,0	W 3,1	W 3,2	W 3,3	W 3,4
W 4,0	W 4,1	W 4,2	W 4,3	W 4,4

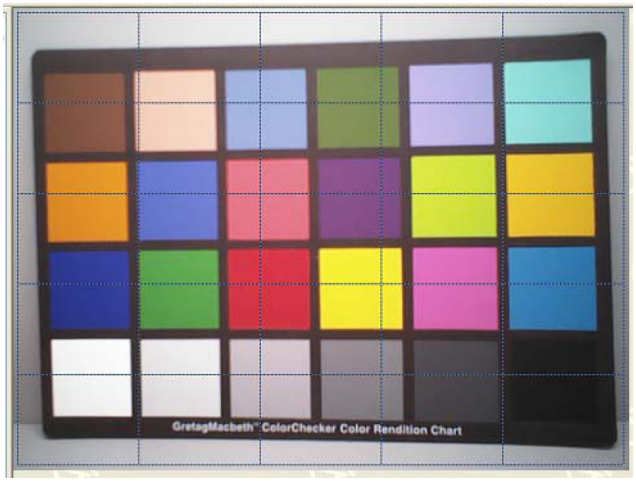


Figure 10. 5 x 5 Grid

AE TRACK DRIVER

Other algorithm features include the rejection of fast fluctuations in illumination (time averaging), control of speed of response, and control of the sensitivity to small changes. While the default settings are adequate in most situations, the user can program target brightness, measurement window, and other parameters described above.

The driver changes AE parameters (integration time, gains, and so on) to drive scene brightness to the programmable target.

To avoid unwanted reaction of AE on small fluctuations of scene brightness or momentary scene changes, the AE track driver uses a temporal filter for luma and a threshold around the AE luma target. The driver changes AE parameters only if the difference between the AE luma target and the filtered luma is larger than the AE target step and pushes the luma beyond the threshold.

AUTO WHITE BALANCE

The AP0101CS has a built−in AWB algorithm designed to compensate for the effects of changing spectra of the scene illumination on the quality of the color rendition. The algorithm consists of two major parts: a measurement engine performing statistical analysis of the image and a driver performing the selection of the optimal color correction matrix and IFP digital gain. While default settings of these algorithms are adequate in most situations,

the user can reprogram base color correction matrices, place limits on color channel gains, and control the speed of both matrix and gain adjustments. The AP0101CS AWB displays the current AWB position in color temperature, the range of which will be defined when programming the CCM matrixes.

The region of interest can be controlled through the combination of an inclusion window and an exclusion window.

DUAL BAND IRCF

For some applications a day/night filter would be switched in/out, this option is an additional cost to the camera system. The AP0101CS supports the use of dual band IRCF, which removes the need for the switching day/night filter. Tuning support is provided for this usage case. Refer to the AP0101CS developer guide for details.

EXPOSURE AND WHITE BALANCE MODES

AP0101CS supports auto and manual exposure and white balance modes. In addition, it will operate within synchronized multi−camera systems. In this use case, one camera within the system will be the 'master', and the others 'slaves'. The master is used to calculate the appropriate exposure and white balance. This is then applied to all slaves concurrently under host control.

Auto Mode

In Auto Exposure mode the AE algorithm is responsible for calculating the appropriate exposure to keep the desired scene brightness, and for applying the exposure to the underlying hardware. In Auto White Balance mode the AWB algorithm is responsible for calculating the color temperature of the scene and applying the appropriate red and blue gains.

Triggered Auto Mode

The Triggered Auto Exposure and Triggered Auto White Balance modes are intended for the multicamera use cases, where a host is controlling the exposure and white balance of a number of cameras. The idea is that one camera is in triggered−auto mode (the master), and the others in host−controlled mode (slaves). The master camera must calculate the exposure and gains, the host then copies this to the slaves, and all changes are then applied at the same time.

Manual Mode

Manual mode is intended to allow simple manual exposure and white balance control by the host. The host needs to set the CAM_AET_EXPOSURE_TIME_MS, CAM_AET_EXPOSURE_GAIN and CAM_AWB_COLOR_TEMPERATURE controls, the camera will calculate the appropriate integration times and gains.

Host Controlled

The Host Controlled mode is intended to give the host full control over exposure and gains.

FLICKER AVOIDANCE

Flicker occurs when the integration time is not an integer multiple of the period of the light intensity. The AP0101CS can be programmed to avoid flicker for 50 or 60 Hz. For integration times less than the light intensity period (10ms for 50 Hz environment), flicker cannot be avoided. The AP0101CS supports an indoor AE mode, that will ensure flicker−free operation.

OUTPUT FORMATTING

The AP0101CS can output pixel data as an 8 or 10 bit word, over one or two clocks per pixel. AP0101AT supports parallel output & SMPTE modes.

Uncompressed YCbCr Data Ordering

The AP0101CS supports swapping YCbCr mode, as illustrated in Table 12.

Table 12. YCbCr OUTPUT DATA ORDERING

Mode	Data Sequence			
Default (no swap)	Cbi	Yi	Cri	Yi+1
Swapped CrCb	Cri	Yi	Cbi	Yi+1
Swapped YC	Yi	Cbi	Yi+1	Cri
Swapped CrCb, YC	Yi	Cri	Yi+1	Cbi

The data ordering for the YCbCr output modes for AP0101CS are shown in Tables 13 and 14:

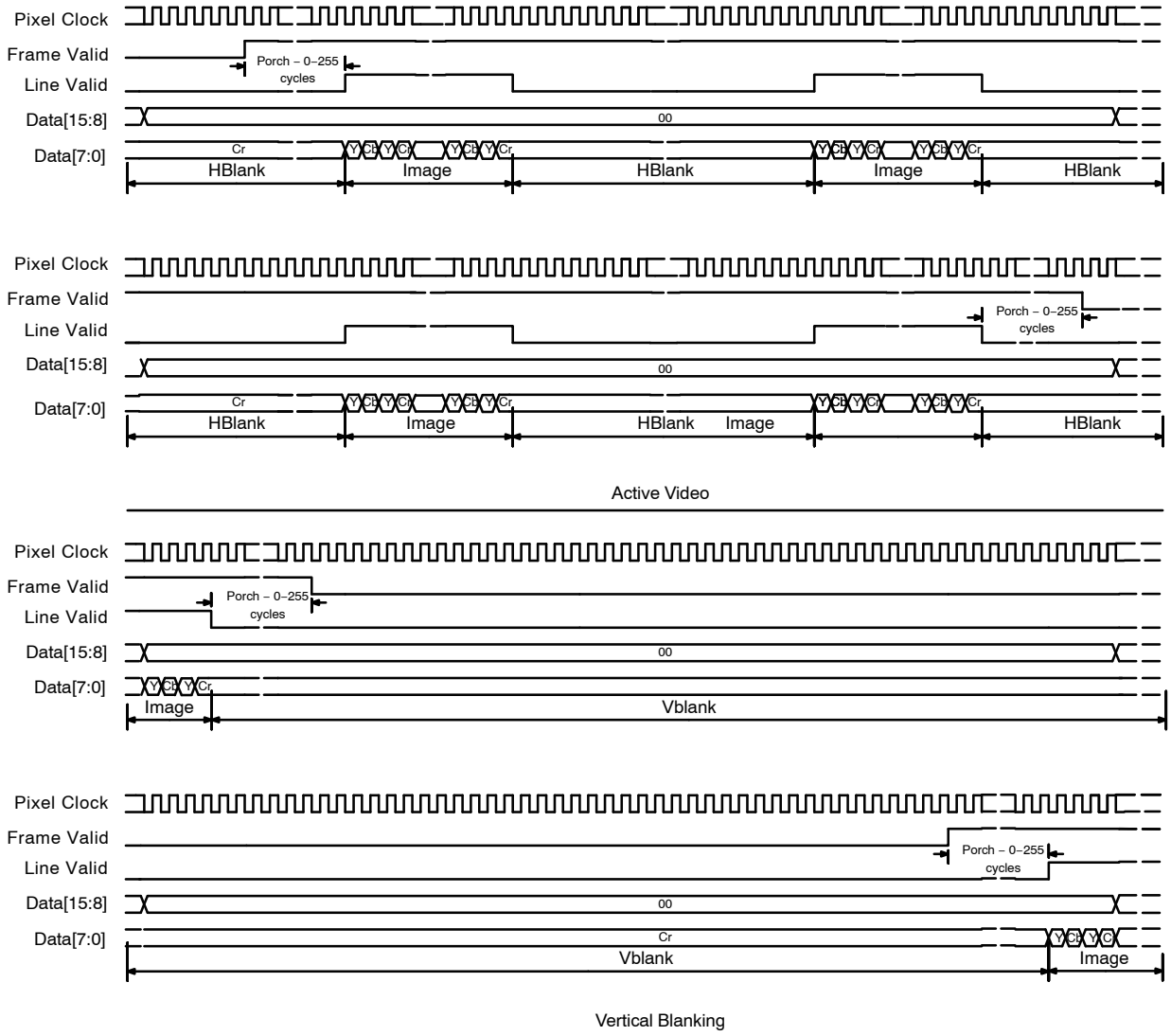
Table 13. YCbCr OUTPUT MODES (cam_port_parallel_msb_align=0x1, cam_port_parallel_swap_bytes = 0, cam_output_format_yuv_swap_red_blue = 0)

Mode	Byte	Pixel i	Pixel i+1	Notes
YCbCr_422_8_8	Odd (D_{OUT} [15:8])	Cbi	Cri	Data range of 0−255 (Y = 16−235 and C = 16−240)
	Even (D_{OUT} [15:8])	Yi	Yi+1	
YCbCr_422_10_10	Odd (D_{OUT} [15:6])	Cbi	Cri	Data range of 0−1023 (Y = 64−940 and C = 64−960)
	Even (D_{OUT} [15:6])	Yi	Yi+1	
YCbCr_422_16	Single (D_{OUT} [15:0])	Cbi_Yi	Cri_Yi+1	Data range of 0−255 (Y = 16−235 and C = 16−240)

7. Odd means first cycle; even means second cycle.

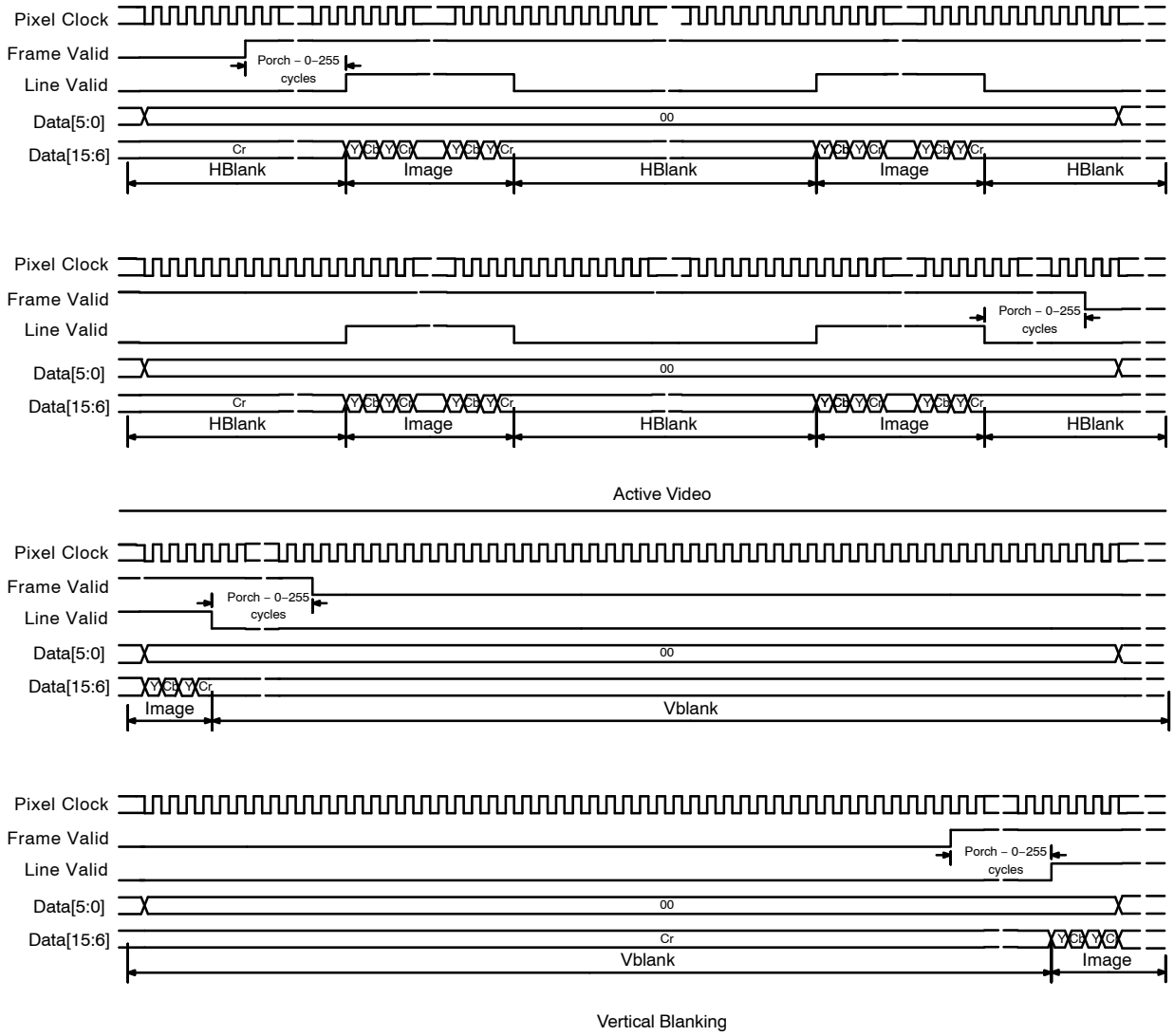
Table 14. YCbCr OUTPUT MODES (cam_port_parallel_msb_align=0x0, cam_port_parallel_swap_bytes = 0, cam_output_format_yuv_swap_red_blue = 0)

Mode	Byte	Pixel i	Pixel i+1	Notes
YCbCr_422_8_8	Odd (D_{OUT} [7:0])	Cbi	Cri	Data range of 0−255 (Y = 16−235 and C = 16−240)
	Even (D_{OUT} [7:0])	Yi	Yi+1	
YCbCr_422_10_10	Odd (D_{OUT} [9:0])	Cbi	Cri	Data range of 0−1023 (Y = 64−940 and C = 64−960)
	Even (D_{OUT} [9:0])	Yi	Yi+1	
YCbCr_422_16	Single (D_{OUT} [15:0])	Cbi_Yi	Cri_Yi+1	Data range of 0−255 (Y = 16−235 and C = 16−240)



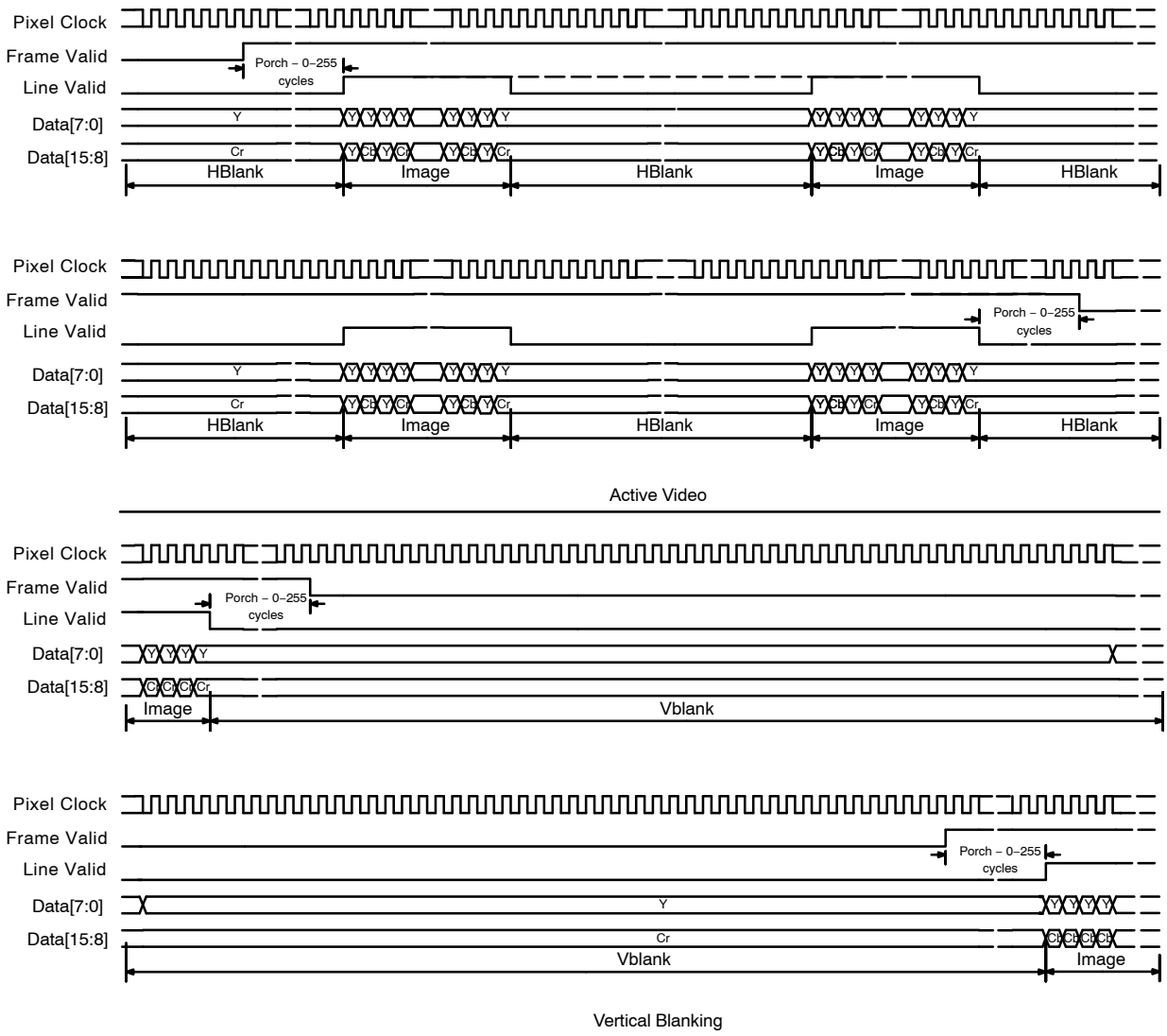
NOTES: cam_port_parallel_msb_align = 0
cam_port_parallel_swap_bytes = 1
cam_output_format_yuv_swap_red_blue = 0

Figure 11. 8−bit YCbCr Output (YCbCr_422_8_8)



NOTES: cam_port_parallel_msb_align = 1
cam_port_parallel_swap_bytes = 1
cam_output_format_yuv_swap_red_blue = 0

Figure 12. 10−bit YCbCr Output (YCbCr_422_10_10)



NOTES: cam_port_parallel_swap_bytes = 0
cam_output_format_yuv_swap_red_blue = 0

Figure 13. 16−bit YCbCr Output (YCbCr_422_16)

SMPTE Output

The data ordering for the SMPTE output mode for AP0101AT is shown in Table 15.

Table 15. SMPTE OUTPUT MODE

Mode	Byte	Pixel i	Pixel i+1	Notes
SMPTE	Single{Dout[15:8],GPIO[5:4]} → Cb/Cr {Dout[7:0],GPIO[3:2]} → Y	Cbi_Yi	Cri_Yi+1	Data range of 4−1019 (Y = 64−940 and C = 64−960)

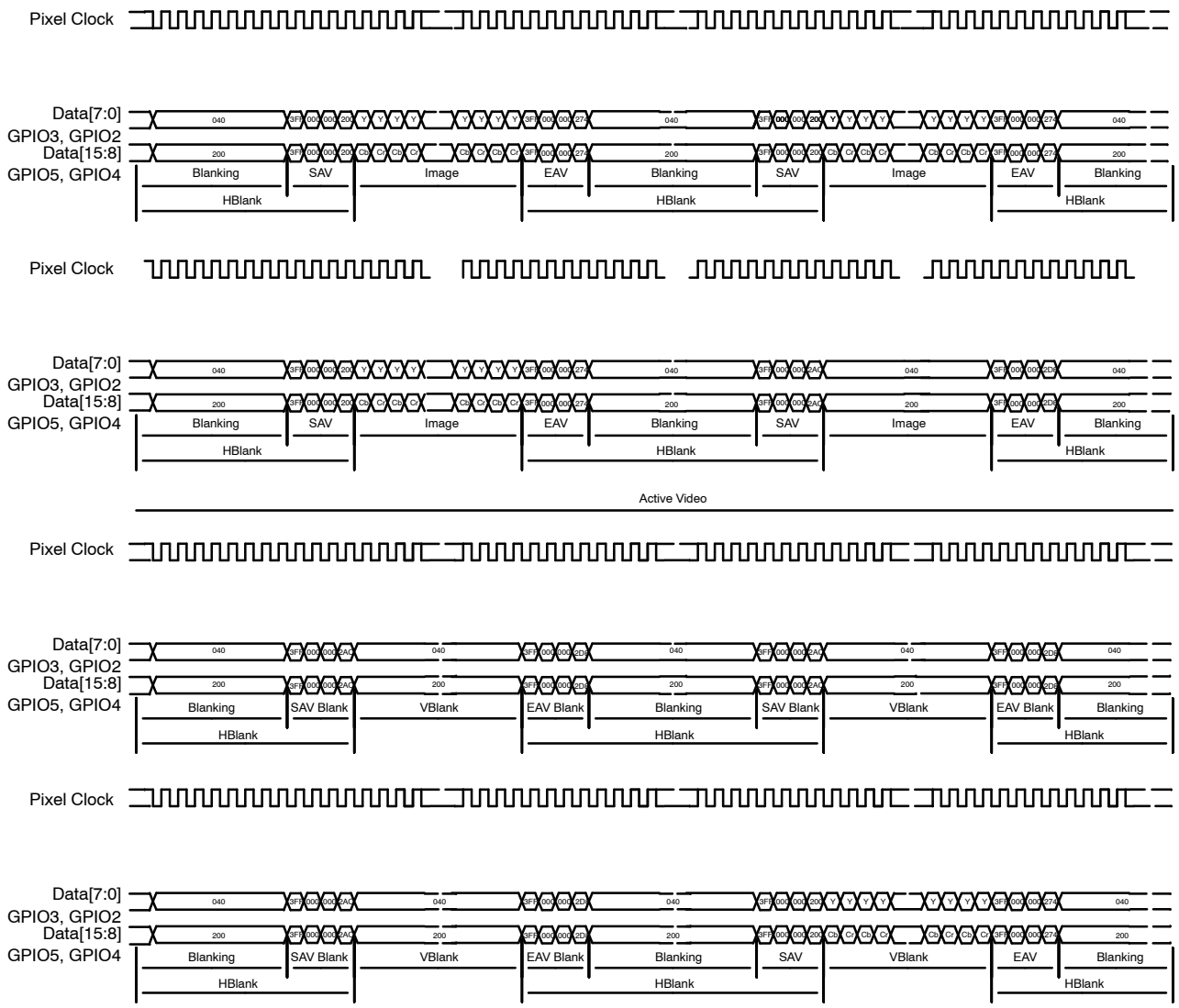


Figure 14. SMPTE296M Output

ALTM Bayer Output

The data ordering for the ALTM Bayer output modes for AP0101CS are shown in Table 16. ALTM Bayer modes are selected by setting cam_mode_select = 7 (ALTM Bayer 12) or 8 (ALTM Bayer 10).

Table 16. ALTM BAYER OUTPUT MODES

Mode	Byte	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALTM_Bayer_10	Single	0	0	0	0	0	0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ALTM_Bayer_12	Single	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Tables 16 and 17 show LSB aligned data; it is possible by using a register setting to obtain MSB aligned data.

The data ordering for the Bayer output modes for AP0101CS are shown in Table 17.

Table 17. BAYER OUTPUT MODES

Mode	Byte	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Raw_Bayer_12	Single	0	0	0	0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

SENSOR EMBEDDED DATA

The AP0101CS is capable of passing sensor embedded data in Bayer output mode only. The AP0101CS Statistics are available through the serial interface. Refer to the Developer Guide for details.

SLAVE TWO−WIRE SERIAL INTERFACE

The two−wire slave serial interface bus enables read/write access to control and status registers within the AP0101CS.

The interface protocol uses a master/slave model in which a master controls one or more slave devices.

PROTOCOL

Data transfers on the two−wire serial interface bus are performed by a sequence of low−level protocol elements, as follows:

- a start or restart condition
- a slave address/data direction byte
- a 16−bit register address
- an acknowledge or a no−acknowledge bit
- data bytes
- a stop condition

The bus is idle when both SCLK and SDATA are HIGH. Control of the bus is initiated with a start condition, and the bus is released with a stop condition. Only the master can generate the start and stop conditions.

The SADDR pin is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xBA. See Table 18 below. The user can change the slave address by changing a register value.

Table 18. TWO−WIRE INTERFACE ID ADDRESS SWITCHING

S_{ADDR}	Two−Wire Interface Address ID
0	0x90
1	0xBA

Start Condition

A start condition is defined as a HIGH−to−LOW transition on SDATA while SCLK is HIGH.

At the end of a transfer, the master can generate a start condition without previously generating a stop condition; this is known as a “repeated start” or “restart” condition.

Data Transfer

Data is transferred serially, 8 bits at a time, with the MSB transmitted first. Each byte of data is followed by an acknowledge bit or a no−acknowledge bit. This data transfer mechanism is used for the slave address/data direction byte and for message bytes. One data bit is transferred during each SCLK clock period. SDATA can change when SCLK is low and must be stable while SCLK is HIGH.

Slave Address/Data Direction Byte

Bits [7:1] of this byte represent the device slave address and bit [0] indicates the data transfer direction. A “0” in bit [0] indicates a write, and a “1” indicates a read. The default slave addresses used by the AP0101CS are 0x90 (write address) and 0x91 (read address). Alternate slave addresses of 0xBA (write address) and 0xBB (read address) can be selected by asserting the SADDR input signal.

Message Byte

Message bytes are used for sending register addresses and register write data to the slave device and for retrieving register read data. The protocol used is outside the scope of the two−wire serial interface specification.

Acknowledge Bit

Each 8−bit data transfer is followed by an acknowledge bit or a no−acknowledge bit in the SCLK clock period following the data transfer. The transmitter (which is the master when writing, or the slave when reading) releases SDATA. The receiver indicates an acknowledge bit by driving SDATA LOW. As for data transfers, SDATA can change when SCLK is LOW and must be stable while SCLK is HIGH.

No−Acknowledge Bit

The no−acknowledge bit is generated when the receiver does not drive SDATA low during the SCLK clock period following a data transfer. A no−acknowledge bit is used to terminate a read sequence.

Stop Condition

A stop condition is defined as a LOW−to−HIGH transition on SDATA while SCLK is HIGH.

Typical Operation

A typical READ or WRITE sequence begins by the master generating a start condition on the bus. After the start condition, the master sends the 8−bit slave address/data direction byte. The last bit indicates whether the request is for a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ. If the address matches the address of the slave device, the slave device acknowledges receipt of the address by generating an acknowledge bit on the bus.

If the request was a WRITE, the master then transfers the 16−bit register address to which a WRITE will take place. This transfer takes place as two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master will then transfer the 8−bit or 16−bit data, as one or two 8−bit sequences and the slave sends an acknowledge bit after each sequence to indicate that the byte has been received. The master stops writing by generating a (re)start or stop condition. If the request was a READ, the master sends the 8−bit write slave address/data direction byte and 16−bit register address, just as in the write request. The master then

generates a (re)start condition and the 8−bit read slave address/data direction byte, and clocks out the register data, 8 bits at a time. The master generates an acknowledge bit after each 8−bit transfer. The data transfer is stopped when the master sends a no−acknowledge bit.

Single READ from random location

Figure 15 shows the typical READ cycle of the host to the AP0101CS. The first two bytes sent by the host are an internal 16−bit register address. The following 2−byte READ cycle sends the contents of the registers to host.

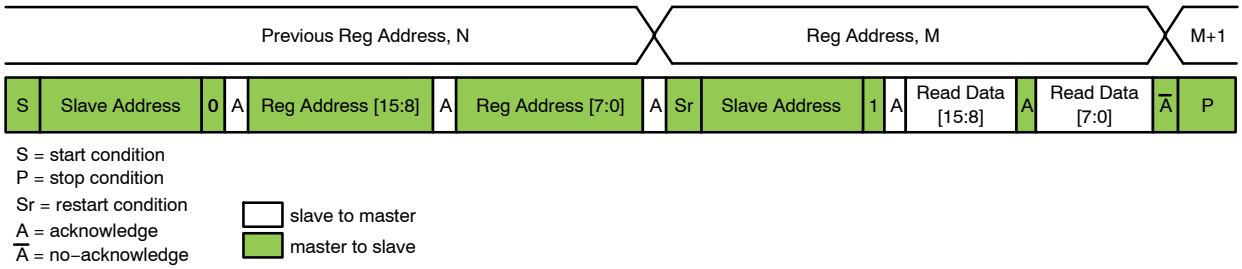


Figure 15. Single READ from Random Location

Single READ from current location

Figure 16 shows the single READ cycle without writing the address. The internal address will use the previous address value written to the register.

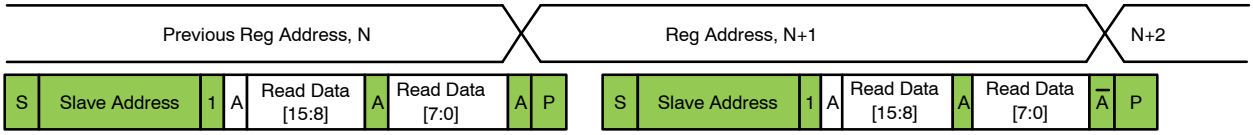


Figure 16. Single Read from Current Location

Sequential READ, start from random location

This sequence (Figure 17) starts in the same way as the single READ from random location (Figure 15). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte READs until “L” bytes have been read.

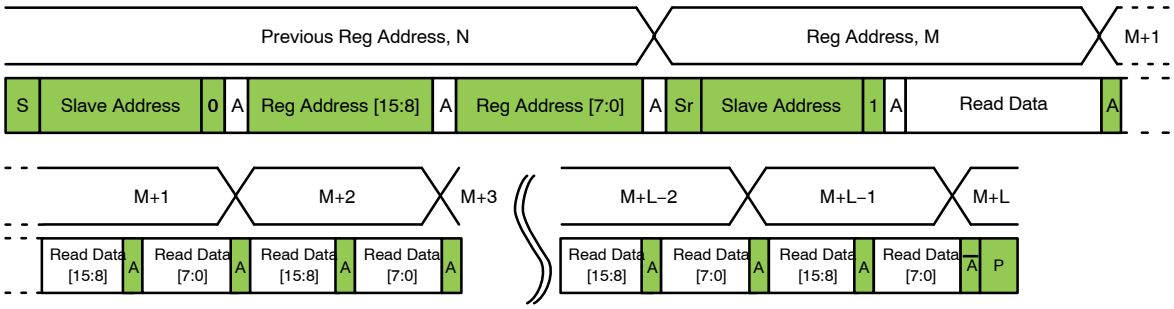


Figure 17. Sequential READ, Start from Random Location

Sequential READ, start from current location

This sequence (Figure 18) starts in the same way as the single READ from current location (Figure 16). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte reads until “L” bytes have been read.

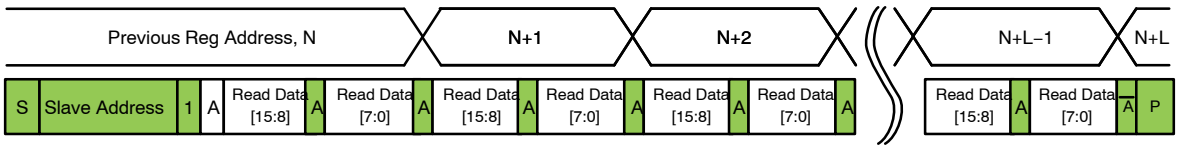


Figure 18. Sequential READ, Start from Current Location

Single write to random location

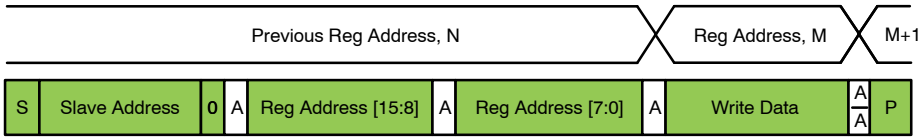


Figure 19. Single WRITE to Random Location

Sequential WRITE, start at random location

This sequence (Figure 20) starts in the same way as the single WRITE to random location (Figure 19). Instead of generating a no−acknowledge bit after the first byte of data has been transferred, the master generates an acknowledge bit and continues to perform byte writes until "L" bytes have been written. The WRITE is terminated by the master generating a stop condition.

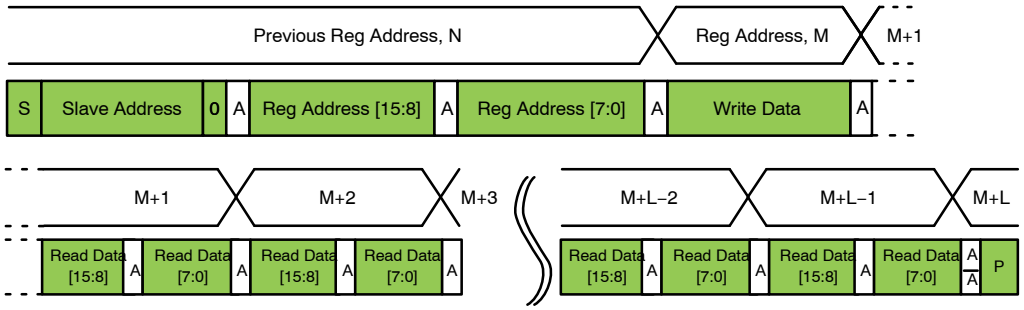


Figure 20. Sequential WRITE, Start from Current Location

Device Configuration and Usage Modes

After power is applied and the device is out of reset (either the power on reset, hard or soft reset), it will enter a boot sequence to configure its operating mode. There are essentially three configuration modes: Flash/EEPROM Config, Auto Config, and Host Config.

The AP0101CS firmware supports a System Configuration phase at start−up. This consists of four sub−phases of execution:

Flash detection, then one of:

a. Flash Config

b. Auto Config

c. Host Config

The System Configuration phase is entered immediately following power−up or reset. Then the firmware performs Flash Detection.

Flash Detection attempts to detect the presence of an SPI Flash or EEPROM device:

- If no device is detected, the firmware then samples the SPI_SDI pin state to determine the next mode:
  - ♦ If SPI_SDI is low, then it enters the Host−Config mode.
  - ♦ If SPI_SDI is high, then it enters the Auto−Config mode.
- If a device is detected, the firmware switches to the Flash−Config mode.

In the Flash−Config mode, the firmware interrogates the device to determine if it contains valid configuration records:

- If no records are detected, then the firmware enters the Auto−Config mode.
- If records are detected, the firmware processes them. By default, when all Flash records are processed the firmware switches to the Host−Config mode. However, the records encoded into the Flash can optionally be used to instruct the firmware to proceed to auto−config, or to start streaming (via a Change−Config).

In the Host−Config mode, the firmware performs no configuration, and remains idle waiting for configuration and commands from the host. The System Configuration phase is effectively complete and the AP0101CS will take no actions until the host issues commands.

In the Auto−Config mode, the part will start streaming with the default settings.

USAGE MODES

How a camera based on the AP0101CS will be configured depends on what features are used. In the simplest case, an AP0101AT operating in Auto−Config mode with no customized settings might be sufficient.

In the simplest case no EEPROM or Flash memory or μC is required, as shown in Figure 21.

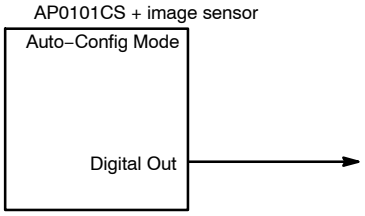


Figure 21. Auto−Config Mode

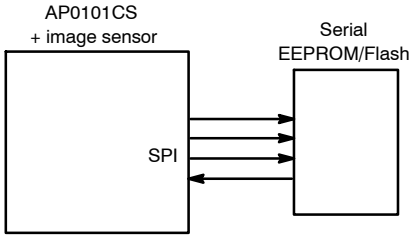
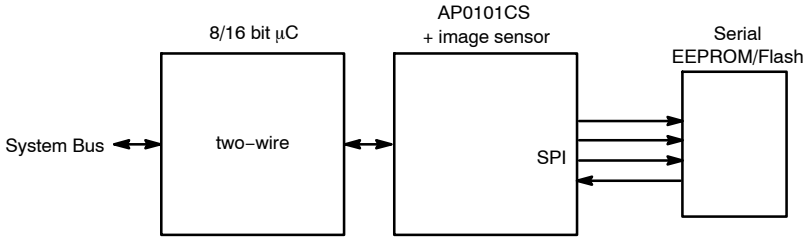


Figure 22. Flash Mode



NOTE: In this configuration all settings are communicated to the AP0101CS and sensor through the micro−controller.

Figure 23. Host Mode with Flash

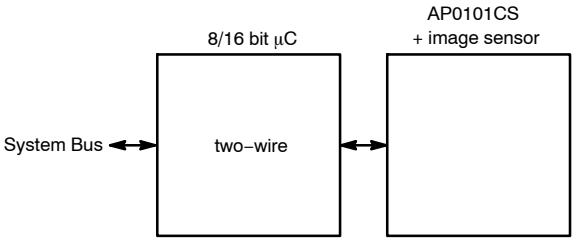


Figure 24. Host Mode

Supported NVM Devices

The AP0101AT supports a variety of SPI NVM devices. Refer to the Flash/EEPROM programming section of the Developer Guide for details.

HOST COMMAND INTERFACE

The AP0101CS has a mechanism to execute higher level commands, the Host Command Interface (HCI). Once a command has been written through the HCI, it will be executed by on−chip firmware and the results are reported back. EEPROM or Flash memory is also available to store commands for later execution. For details on the host command interface and host commands, refer to the Host Command Interface document.

ELECTRICAL SPECIFICATIONS

Caution: Stresses greater than those listed in Table 19 may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 19. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating		Unit
		Min	Max	
V_{DD}_REG	Digital power (1.8 V)	−0.3	4.95	V
V_{DD}IO_H	Host I/O power (2.5 V, 3.3 V)	2.25	5.4	V
V_{DD}IO_S	Sensor I/O power (1.8 V, 2.8 V)	1.7	5.4	V
V_{DD}	Digital core power	1.1	2.5	V
V_{DD}_PLL	PLL power	1.1	2.5	V
V_{DD}IO_OTPM	OTPM power	2.25	5.4	V
V_{IN}	DC Input Voltage	−0.3	V_{DD}IO_* + 0.3	V
V_{OUT}	DC Output Voltage	−0.3	V_{DD}IO_* + 0.3	V
T_{STG}	Storage Temperature	−50	150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Table 20. ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

Parameter	Min	Typ	Max	Unit
Supply input to on−chip regulator (V_{DD}_REG)	1.62	1.8	1.98	V
Host IO voltage (V_{DD}IO_H)	2.25	2.5/3.3	3.6	V
Sensor IO voltage (V_{DD}IO_S)	1.7	1.8/2.8	3.1	V
Core voltage (V_{DD})	1.08	1.2	1.32	V
PLL voltage (V_{DD}_PLL)	1.08	1.2	1.32	V
OTPM power supply (V_{DD}IO_OTPM)	2.25	2.5/3.3	3.6	V
Functional operating temperature (ambient − T_A)	−30		70	°C
Storage Temperature	−55		150	°C

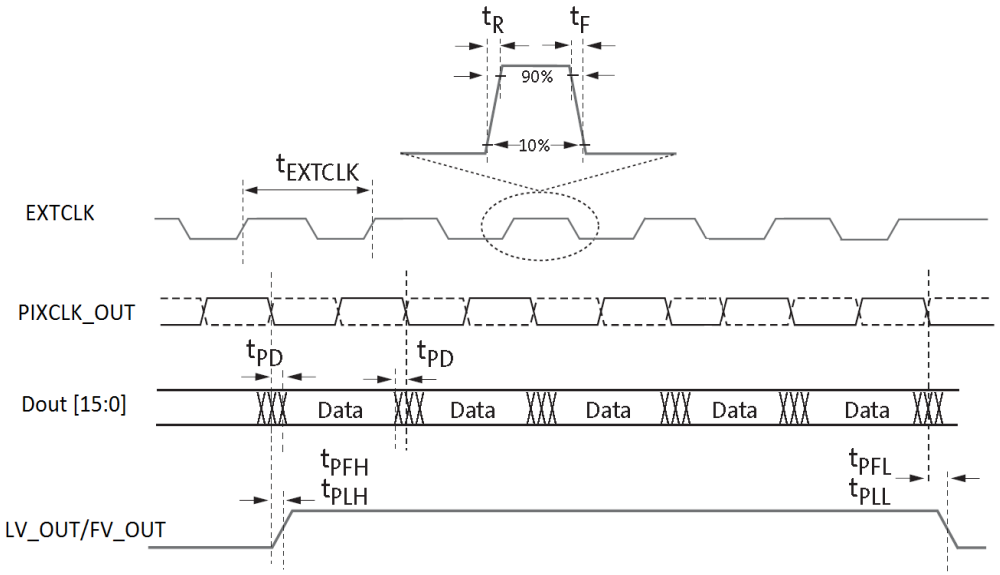


Figure 25. Parallel Digital Output I/O Timing

Table 21. AC ELECTRICAL CHARACTERISTICS (referring to Figure 25)
Default Setup Conditions: f_{EXTCLK}= 27 MHz, f_{PIXCLK} = 74.125 MHz or f_{PIXCLK} = 84 MHz, $V_{DD}IO\_H = V_{DD}\_OTPM$ = 2.8 V, $V_{DD}\_REG = V_{DD}IO\_S$ = 1.8 V, T_A = 25°C unless otherwise stated.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{EXTCLK}	External clock frequency (Note 8)		6		30	MHz
t_R	External input clock rise time (Note 9)	10%–90% $V_{DD}IO\_H$	–	2	5	ns
t_F	External input clock fall time (Note 9)	90%–10% $V_{DD}IO\_H$	–	2	5	ns
D_{EXTCLK}	External input clock duty cycle		40	50	60	%
t_{JITTER}	External input clock jitter		–	500	–	ps
f_{PIXCLK}	Pixel clock frequency (one−clock/pixel)		6	–	74.25	MHz
	Pixel clock frequency (two−clocks/pixel)		6	–	84	MHz
$t_{RPIXCLK}$	Pixel clock rise time (10−90%)	C_{LOAD} = 35 pF	–	3	5	ns
$t_{FPIXCLK}$	Pixel clock fall time (10−90%)	C_{LOAD} = 35 pF	–	3	5	ns
t_{PD}	PIXCLK to data valid		–	3	5	ns
t_{PFH}	PIXCLK to FV HIGH		–	3	5	ns
t_{PLH}	PIXCLK to LV HIGH		–	3	5	ns
t_{PFL}	PIXCLK to FV LOW		–	3	5	ns
t_{PLL}	PIXCLK to LV LOW		–	3	5	ns

8. V_{IH}/V_{IL} restrictions apply.
9. This is applicable only a when the PLL is bypassed. When the PLL is being used then the user should ensure that V_{IH}/V_{IL} is met.

Table 22. DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	Input HIGH voltage (Note 10)		$V_{DD}IO\_H$ or $V_{DD}IO\_S$*0.8		V
V_{IL}	Input LOW voltage (Note 10)			$V_{DD}IO\_H$ or $V_{DD}IO\_S$*0.2	V
I_{IN}	Input leakage current (Note 11)	V_{IN} = 0 V or V_{IN} = $V_{DD}IO\_H$ or $V_{DD}IO\_S$		10	μA
V_{OH}	Output HIGH voltage		$V_{DD}IO\_H$ or $V_{DD}IO\_S$*0.8		V
V_{OL}	Output LOW voltage			$V_{DD}IO\_H$ or $V_{DD}IO\_S$*0.2	V

10. V_{IL} and V_{IH} have min/max limitations specified by absolute ratings.
11. Excludes pins that have internal PU resistors.

Table 23. OPERATING CURRENT CONSUMPTION

Default Setup Conditions: f_{EXTCLK}= 27 MHz, f_{PIXCLK} = as below, V_{DD}_REG = 1.8 V; $V_{DDI}O\_H$ not included in measurement $V_{DDI}O\_S$ = 2.8 V, $V_{DDI}O\_OTPM$ = 3.3 V, T_A = 50°C unless otherwise stated

Symbol	Conditions	Min	Typ	Max	Unit
V_{DD}_REG		1.62	1.8	1.98	V
$V_{DD}IO\_H$	$V_{DD}IO\_H$ = 2.5 V	2.25	2.5	2.75	V
	$V_{DD}IO\_H$ = 3.3 V	3	3.3	3.6	V
$V_{DD}IO\_S$	$V_{DD}IO\_S$ = 1.8 V	1.7	1.8	1.9	V
	$V_{DD}IO\_S$ = 2.8 V	2.5	2.8	3.1	V
$V_{DD}IO\_OTPM$	$V_{DD}IO\_OTPM$ = 2.5 V	2.25	2.5	2.75	V
	$V_{DD}IO\_OTPM$ = 3.3 V	3	3.3	3.6	V
I_{DD}_REG	960p HDR 30 fps 37.125 MHz YCbCr_422_16		42		mA
	800p HDR 30 fps 84 MHz YCbCr_422_10_10 or YCbCr_422_8_8		36		mA
	720p HDR 60 fps 74.25 MHz YCbCr_422_16		64		mA
	720p HDR 30 fps 37.125 MHz YCbCr_422_16		33		mA
	720p HDR 30 fps 74.25 MHz YCbCr_422_10_10 or YCbCr_422_8_8		33		mA
$I_{DD}IO\_S$	960p HDR 30 fps 37.125 MHz YCbCr_422_16		4.4		mA
	800p HDR 30 fps 84 MHz YCbCr_422_10_10 or YCbCr_422_8_8		4.3		mA
	720p HDR 60 fps 74.25 MHz YCbCr_422_16		4.5		mA
	720p HDR 30 fps 37.125 MHz YCbCr_422_16		4.3		mA
	720p HDR 30 fps 74.25 MHz YCbCr_422_10_10 or YCbCr_422_8_8		4.3		mA
$I_{DD}IO\_OTPM$	960p HDR 30 fps 37.125 MHz YCbCr_422_16		0.25		mA
	800p HDR 30 fps 84 MHz YCbCr_422_10_10 or YCbCr_422_8_8		0.25		mA
	720p HDR 60 fps 74.25 MHz YCbCr_422_16		0.25		mA
	720p HDR 30 fps 37.125 MHz YCbCr_422_16		0.25		mA
	720p HDR 30 fps 74.25 MHz YCbCr_422_10_10 or YCbCr_422_8_8		0.25		mA
Total power consumption	960p HDR 30 fps 37.125 MHz YCbCr_422_16		89		mW
	800p HDR 30 fps 84 MHz YCbCr_422_10_10 or YCbCr_422_8_8		77		mW
	720p HDR 60 fps 74.25 MHz YCbCr_422_16		129		mW
	720p HDR 30 fps 37.125 MHz YCbCr_422_16		72		mW
	720p HDR 30 fps 74.25 MHz YCbCr_422_10_10 or YCbCr_422_8_8		71		mW

Table 24. STANDBY CURRENT CONSUMPTION

f_{EXTCLK}= 27 MHz, V_{DD}_REG = 1.8 V; V_{DDI}O_S = 1.8 V, V_{DDI}O_OTPM = V_{DDI}O_H = 3.3 V, T_A = 50°C, excludes V_{DDI}O_H current

Symbol	Parameter	Condition	Typ	Max	Unit
Hard standby	Total standby current when asserting the STANDBY signal		1.6		mA
Standby power			2.9		mW
Soft standby (clock on)	Total standby current	f_{EXTCLK} = 27 MHz	2.1		mA
Standby power			3.8		mW

Table 25. INRUSH CURRENT

Supply	Max. Current
V_{DD}_REG (1.8 V)	150 mA
V_{DD}IO_H (2.5/3.3 V)	80 mA
V_{DD}IO_S (2.8/1.8 V)	110 mA
V_{DD}IO_OTPM (2.5/3.3 V)	170 mA

TWO−WIRE SERIAL REGISTER INTERFACE

The electrical characteristics of the two−wire serial register interface (SCLK, SDATA) are shown in Figure 26 and Table 26.

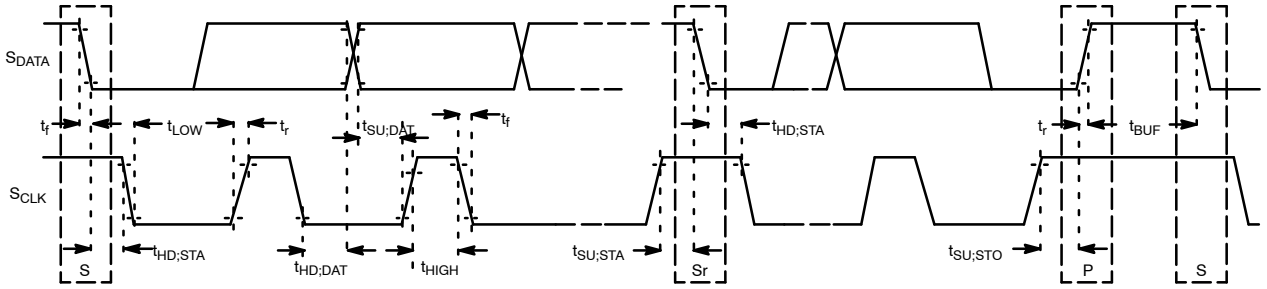


Figure 26. Slave Two Wire Serial Bus Timing Parameters (CCIS)

Table 26. SLAVE TWO−WIRE SERIAL BUS CHARACTERISTICS (CCIS)

(Default Setup Conditions: f_{EXTCLK} = 27 MHz, V_{DD}IO_H = V_{DD}_OTPM = 2.8 V, V_{DD}_REG = V_{DD}IO_S = 1.8 V, T_A = 25°C unless otherwise stated)

Parameter	Symbol	Standard−Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition						
After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0	–	0.6	–	μs
LOW period of the S_{CLK} clock	t_{LOW}	4.7	–	1.3	–	μs
HIGH period of the S_{CLK} clock	t_{HIGH}	4.0	–	0.6	–	μs
Set−up time for a repeated START condition	$t_{SU;STA}$	4.7	–	0.6	–	μs
Data hold time	$t_{HD;DAT}$	0 (Note 13)	3.45 (Note 14)	0	0.9 (Note 14)	μs
Data set−up time	$t_{SU;DAT}$	250	–	100	–	ns
Rise time of both S_{DATA} and S_{CLK} signals (10−90%)	t_r	–	1000	20+0.1Cb (Note15)	300	ns

Table 26. SLAVE TWO−WIRE SERIAL BUS CHARACTERISTICS (CCIS) (continued)
(Default Setup Conditions: f_{EXTCLK} = 27 MHz, $V_{DD}IO\_H = V_{DD}\_OTPM$ = 2.8 V, $V_{DD}\_REG = V_{DD}IO\_S$ = 1.8 V, T_A = 25°C unless otherwise stated)

Parameter	Symbol	Standard−Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
Fall time of both S_{DATA} and S_{CLK} signals (10−90%)	t_f	−	300	20+0.1Cb (Note15)	300	ns
Set−up time for STOP condition	$t_{SU;STO}$	4.0	−	0.6	−	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	−	1.3	−	μs
Capacitive load for each bus line	Cb	−	400	−	400	pF
Serial interface input pin capacitance	$C_{IN\ SI}$	−	3.3	−	3.3	pF
S_{DATA} max load capacitance	$C_{LOAD\ SD}$	−	30	−	30	pF
S_{DATA} pull−up resistor	R_{SD}	1.5	4.7	1.5	4.7	KΩ

12. All values referred to VIHmin = 0.9 V_{DD} and VILmax = 0.1 V_{DD} levels. EXCLK = 27 MHz.
13. A device must internally provide a hold time of at least 300 ns for the S_{DATA} signal to bridge the undefined region of the falling edge of S_{CLK}.
14. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the S_{CLK} signal.
15. Cb = total capacitance of one bus line in pF.

The electrical characteristics of the two−wire serial register interface (SCLK, SDATA) are shown in Figure 27 and Table 27.

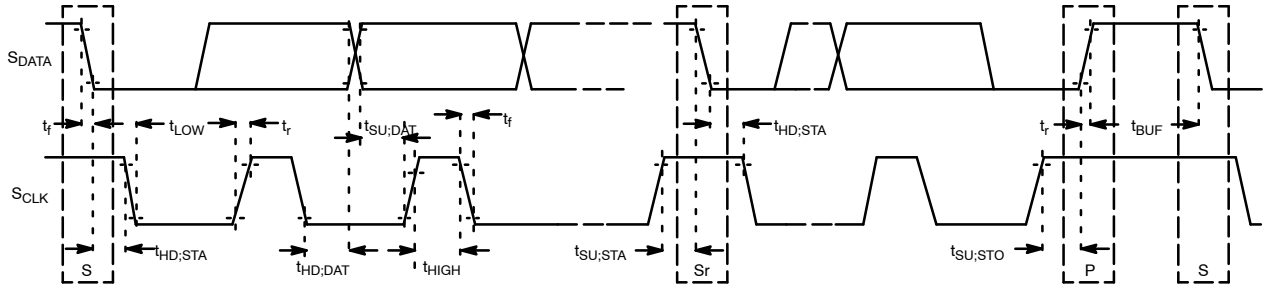


Figure 27. Master Two Wire Serial Bus Timing Parameters (CCIS)

Table 27. MASTER TWO−WIRE SERIAL BUS CHARACTERISTICS (CCIM)
(Default Setup Conditions: f_{EXTCLK} = 27 MHz, $V_{DD}IO\_H = V_{DD}\_OTPM$ = 2.8 V, $V_{DD}\_REG = V_{DD}IO\_S$ = 1.8 V, T_A = 25°C unless otherwise stated)

Parameter	Symbol	Standard−Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
M_S_{CLK} Clock Frequency	f_{SCL}	0	100	0	400	KHz
Hold time (repeated) START condition						
After this period, the first clock pulse is generated.	$t_{HD;STA}$	4.0	−	0.6	−	μs
LOW period of the M_S_{CLK} clock	t_{LOW}	4.7	−	1.2	−	μs
HIGH period of the M_S_{CLK} clock	t_{HIGH}	4.0	−	0.6	−	μs
Set−up time for a repeated START condition	$t_{SU;STA}$	4.7	−	0.6	−	μs
Data hold time	$t_{HD;DAT}$	0 (Note 17)	3.45 (Note 18)	0	0.9 (Note 18)	μs
Data set−up time	$t_{SU;DAT}$	250	−	100	−	ns
Rise time of both M_S_{DATA} and M_S_{CLK} signals (10−90%)	t_r	−	1000	20+0.1Cb (Note 19)	300	ns

Table 27. MASTER TWO−WIRE SERIAL BUS CHARACTERISTICS (CCIM) (continued)
(Default Setup Conditions: f_{EXTCLK} = 27 MHz, $V_{DD}IO\_H = V_{DD}\_OTPM$ = 2.8 V, $V_{DD}\_REG = V_{DD}IO\_S$ = 1.8 V, T_A = 25°C unless otherwise stated)

Parameter	Symbol	Standard−Mode		Fast−Mode		Unit
		Min	Max	Min	Max	
Fall time of both M_S_{DATA} and M_S_{CLK} signals (10−90%)	t_f	−	300	20+0.1Cb (Note 19)	300	ns
Set−up time for STOP condition	$t_{SU;STO}$	4.0	−	0.6	−	μs
Bus free time between a STOP and START condition	t_{BUF}	4.7	−	1.3	−	μs
Capacitive load for each bus line	Cb	−	400	−	400	pF
Serial interface input pin capacitance	$C_{IN\ SI}$	−	3.3	−	3.3	pF
M_S_{DATA} max load capacitance	$C_{LOAD\ SD}$	−	30	−	30	pF
M_S_{DATA} pull−up resistor	R_{SD}	1.5	4.7	1.5	4.7	kΩ

16. All values referred to VIHmin = 0.9 V_{DD} and VILmax = 0.1 V_{DD} levels. EXCLK = 27 MHz.
17. A device must internally provide a hold time of at least 300 ns for the M_S_{DATA} signal to bridge the undefined region of the falling edge of M_S_{CLK}.
18. The maximum $t_{HD;DAT}$ has only to be met if the device does not stretch the LOW period (t_{LOW}) of the M_S_{CLK} signal.
19. Cb = total capacitance of one bus line in pF.

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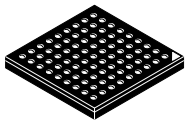

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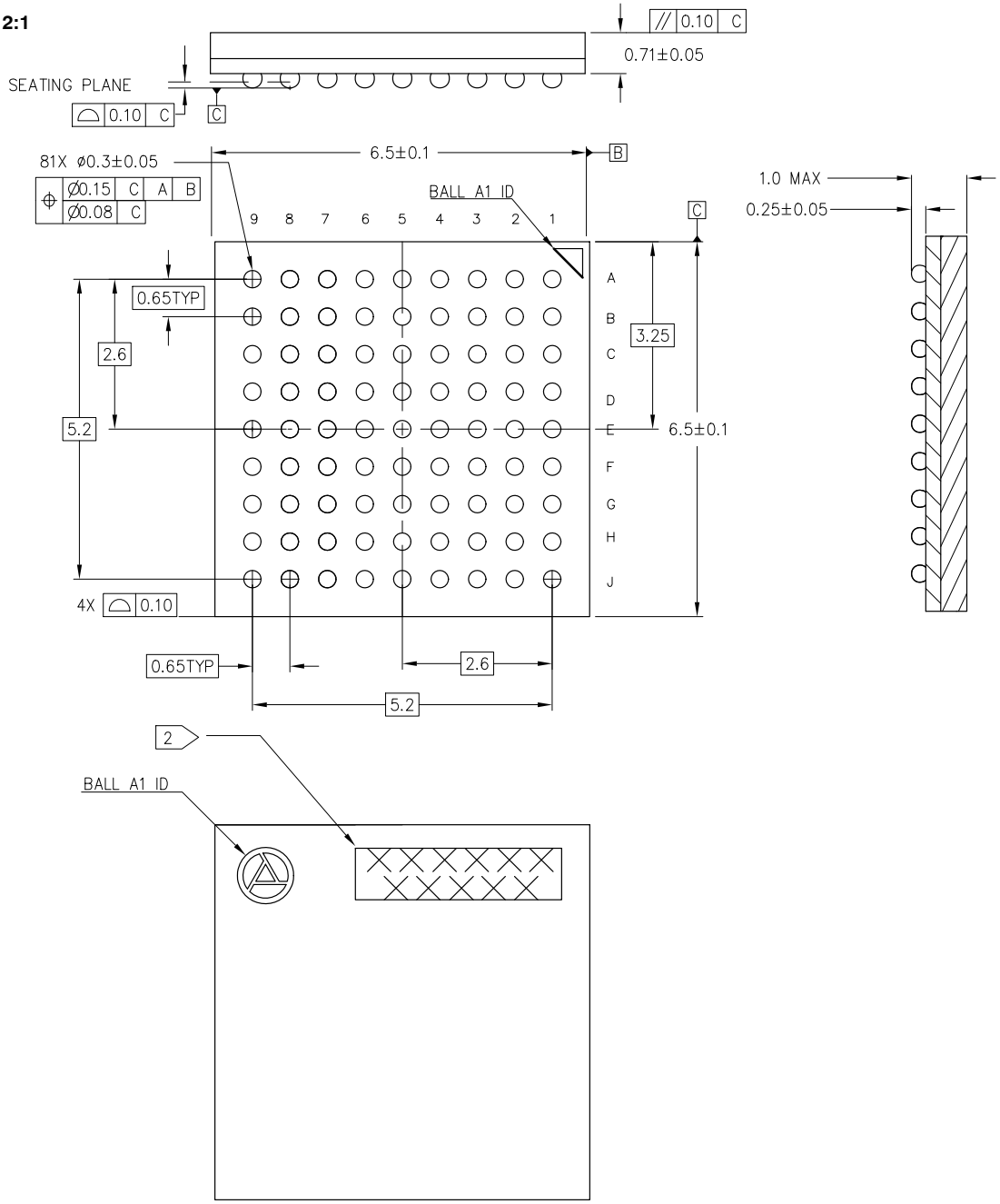

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