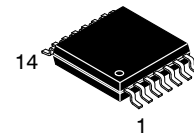


Quad 2-Input NAND Gate

74VHCT00A



TSSOP-14 WB
CASE 948G

General Description

The VHCT00A is an advanced high-speed CMOS 2-Input NAND Gate fabricated with silicon gate CMOS technology. It achieves the high-speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The internal circuit is composed of 3 stages, including buffer output, which provide high noise immunity and stable output.

The Protection circuits ensure that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage and to the output pins with $V_{CC} = 0$ V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3 V to 5 V systems and two supply systems such as battery backup.

Features

- High Speed: $t_{PD} = 5.0$ ns (Typ.) at $T_A = 25^\circ\text{C}$
- High Noise Immunity: $V_{IH} = 2.0$ V, $V_{IL} = 0.8$ V
- Power Down Protection is Provided on All Inputs and Outputs
- Low Noise: $V_{OLP} = 0.8$ V (Max.)
- Low Power Dissipation: $I_{CC} = 2$ A (Max.) at $T_A = 25^\circ\text{C}$
- Pin and Function Compatible with 74HCT00
- Pb-Free, Halogen Free/BFR Free and RoHS Compliant

Logic Symbol

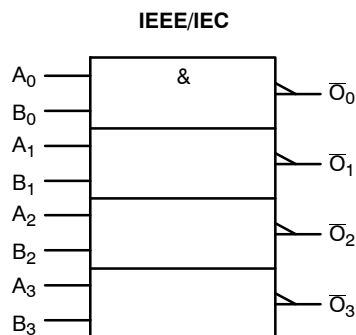
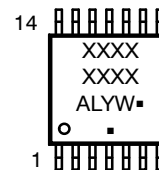


Figure 1. Logic Symbol

TRUTH TABLE

| A | B | \bar{O} |
|---|---|-----------|
| L | L | H |
| L | H | H |
| H | L | H |
| H | H | L |

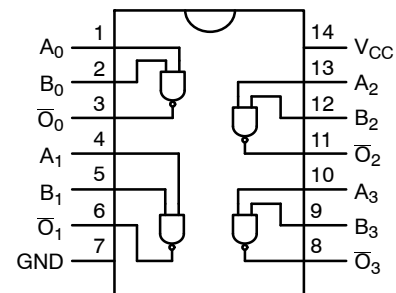
MARKING DIAGRAM



- XXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

| Pin Names | Description |
|-------------|-------------|
| A_n, B_n | Inputs |
| \bar{O}_n | Outputs |

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

74VHCT00A

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|---------------|--|--|----------------|
| V_{CC} | DC Supply Voltage | -0.5 to +6.5 | V |
| V_{IN} | DC Input Voltage | -0.5 to +6.5 | V |
| V_{OUT} | DC Output Voltage Active Mode (High or Low State) Tristate Mode (Note 1) Power=Off Mode ($V_{CC} = 0$ V) | -0.5 to $V_{CC} + 0.5$ -0.5 to +6.5 -0.5 to +6.5 | V |
| I_{IN} | DC Input Current, per Pin | ± 20 | mA |
| I_{OUT} | DC Output Current, per Pin | ± 25 | mA |
| I_{CC} | DC Supply Current, V_{CC} and GND Pins | ± 50 | mA |
| I_{IK} | Input Clamp Current | -20 | mA |
| I_{OK} | Output Clamp Current | -20 | mA |
| T_{STG} | Storage Temperature Range | -65 to +150 | $^{\circ}$ C |
| T_L | Lead Temperature, 1 mm from Case for 10 seconds | 260 | $^{\circ}$ C |
| T_J | Junction Temperature Under Bias | +150 | $^{\circ}$ C |
| θ_{JA} | Thermal Resistance (Note 2) | 150 | $^{\circ}$ C/W |
| P_D | Power Dissipation in Still Air at 25 $^{\circ}$ C | 833 | mW |
| V_{ESD} | ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model | 2000 N/A | V |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76mm-by-114mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|------------|---|-------------|------------------------|--------------|
| V_{CC} | DC Supply Voltage | 4.5 | 5.5 | V |
| V_{IN} | DC Input Voltage (Note 4) | 0 | 5.5 | V |
| V_{OUT} | DC Output Voltage (Note 4) Active Mode (High or Low State) Tristate Mode (Note 1) Power=Off Mode ($V_{CC} = 0$ V) | 0 0 0 | V_{CC} 5.5 5.5 | V |
| T_A | Operating Temperature | -40 | +85 | $^{\circ}$ C |
| t_r, t_f | Input Rise or Fall Rate $V_{CC} = 4.5$ V to 5.5 V | 0 | 20 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must be held HIGH or LOW. They may not float.

74VHCT00A

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Unit | |
|------------------|---|---------------------|--|--------------------------|------|------|---------------------------------|------|------|---|
| | | | | Min | Typ | Max | Min | Max | | |
| V _{IH} | HIGH Level Input Voltage | 4.5 | | 2.0 | - | - | 2.0 | - | V | |
| | | 5.5 | | 2.0 | - | - | 2.0 | - | | |
| V _{IL} | LOW Level Input Voltage | 4.5 | | - | - | 0.8 | - | 0.8 | V | |
| | | 5.5 | | - | - | 0.8 | - | 0.8 | | |
| V _{OH} | HIGH Level Output Voltage | 4.5 | V _{IN} = V _{IH} or V _{IL} | I _{OH} = -50 μA | 4.40 | 4.50 | - | 4.40 | - | V |
| | | | | I _{OH} = -8 mA | 3.94 | - | - | 3.80 | - | |
| V _{OL} | LOW Level Output Voltage | 4.5 | V _{IN} = V _{IH} or V _{IL} | I _{OL} = 50 μA | - | 0.0 | 0.1 | - | 0.1 | V |
| | | | | I _{OL} = 8 mA | - | - | 0.36 | - | 0.44 | |
| I _{IN} | Input Leakage Current | 0-5.5 | V _{IN} = 5.5 V or GND | - | - | ±0.1 | - | ±1.0 | μA | |
| I _{CC} | Quiescent Supply Current | 5.5 | V _{IN} = V _{CC} or GND | - | - | 2.0 | - | 20.0 | μA | |
| I _{CCT} | Maximum I _{CC} / Input | 5.5 | V _{IN} = 3.4 V, Other Inputs = V _{CC} or GND | - | - | 1.35 | - | 1.50 | mA | |
| I _{OFF} | Output Leakage Current (Power Down State) | 0.0 | V _{OUT} = 5.5 V | - | - | 0.5 | - | 5.0 | μA | |

NOISE CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | Unit |
|------------------|---|---------------------|------------------------|-----------------------|--------|------|
| | | | | Typ | Limits | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} (Note 5) | 5.0 | C _L = 50 pF | 0.4 | 0.8 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} (Note 5) | 5.0 | C _L = 50 pF | -0.4 | -0.8 | V |
| V _{IHD} | Minimum HIGH Level Dynamic Input Voltage (Note 5) | 5.0 | C _L = 50 pF | - | 2.0 | V |
| V _{ILD} | Maximum LOW Level Dynamic Input Voltage (Note 5) | 5.0 | C _L = 50 pF | - | 0.8 | V |

5. Parameter guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Unit |
|-------------------------------------|-------------------------------|---------------------|------------------------|-----------------------|-----|-----|---------------------------------|-----|------|
| | | | | Min | Typ | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay | 5.0 ±0.5 | C _L = 15 pF | - | 5.0 | 6.9 | 1.0 | 8.0 | ns |
| | | | C _L = 50 pF | - | 5.5 | 7.9 | 1.0 | 9.0 | |
| C _{IN} | Input Capacitance | | V _{CC} = Open | - | 4 | 10 | - | 10 | pF |
| C _{PD} | Power Dissipation Capacitance | | (Note 6) | - | 17 | - | - | - | pF |

6. CPD is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:
 $I_{CC} (opr.) = C_{PD} \times V_{CC} \times f_{IN} + I_{CC} / 4$ (per gate)

74VHCT00A

ORDERING INFORMATION

| Device Order Number | Top Marking | Package | Shipping [†] |
|---------------------|-------------|--------------------------|-----------------------|
| 74VHCT00AMTCX | VHCT 00A | TSSOP-14 WB (Pb-Free) | 2,500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

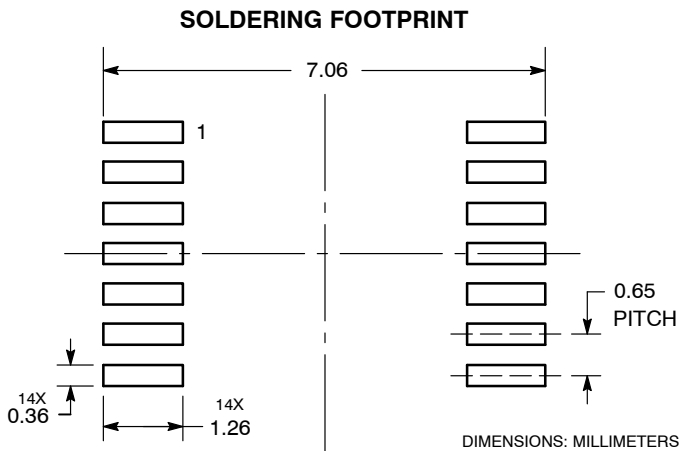
GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



| | | |
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