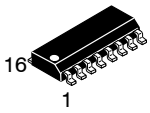
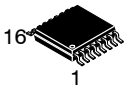
8-Bit Shift Register with Output Latches

74VHC595



SOIC−16
D SUFFIX
CASE 751BG



TSSOP−16
DT SUFFIX
CASE 948AH

General Description

The VHC595 is an advanced high−speed CMOS Shift Register fabricated with silicon gate CMOS technology. It achieves the high−speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

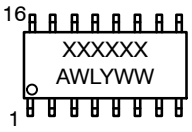
This device contains an 8−bit serial−in, parallel−out shift register that feeds an 8−bit D−type storage register. The storage register has eight 3−STATE outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct−overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive−edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

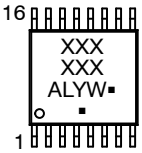
An input protection circuit insures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 5.4 ns (Typ.) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max.) at T_A = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min.)
- Power Down Protection is Provided on All Inputs
- Low Noise: V_{OLP} = 0.9 V (Typ.)
- Pin and function compatible with 74HC595
- This is a Pb−Free Device

MARKING DIAGRAMS





XXX	= Specific Device Code
A	= Assembly Location
WL, L	= Wafer Lot
Y	= Year
WW, W	= Work Week
G, ▪	= Pb−Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 9 of this data sheet.

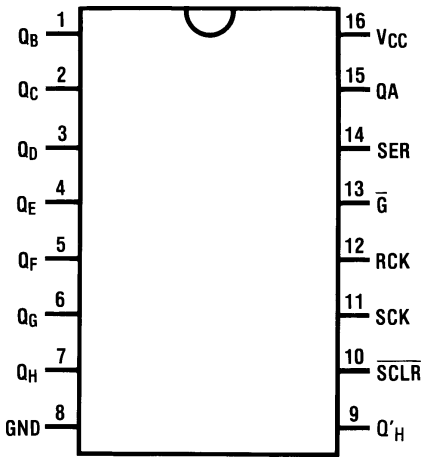


Figure 1. Connection Diagram

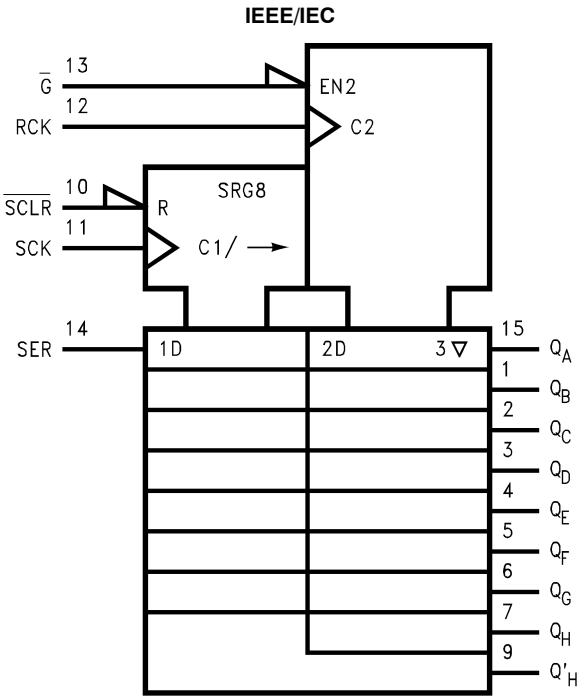


Figure 2. Logic Symbol

PIN DESCRIPTIONS

Pin Names	Description
SER	Serial Data Input
SCK	Shift Register Clock Input (Active rising edge)
RCK	Storage Register Clock Input (Active rising edge)
$\overline{SCLR}$	Reset Input
$\overline{G}$	3−STATE Output Enable Input (Active LOW)
Q_A − Q_H	Parallel Data Outputs
Q'_H	Serial Data Output

TRUTH TABLE

Inputs					Function
SER	RCK	SCK	$\overline{SCLR}$	$\overline{G}$	
X	X	X	X	H	Q_A thru Q_H 3−STATE
X	X	X	X	L	Q_A thru Q_H outputs enabled
X	X	X	L	L	Shift Register cleared: Q'_H = 0
L	X	↑	H	L	Shift Register clocked: $Q_N = Q_{n-1}$, Q_0 = SER = L
H	X	↑	H	L	Shift Register clocked: $Q_N = Q_{n-1}$, Q_0 = SER = H
X	↑	X	H	L	Contents of Shift Register transferred to output latches

Timing Diagram

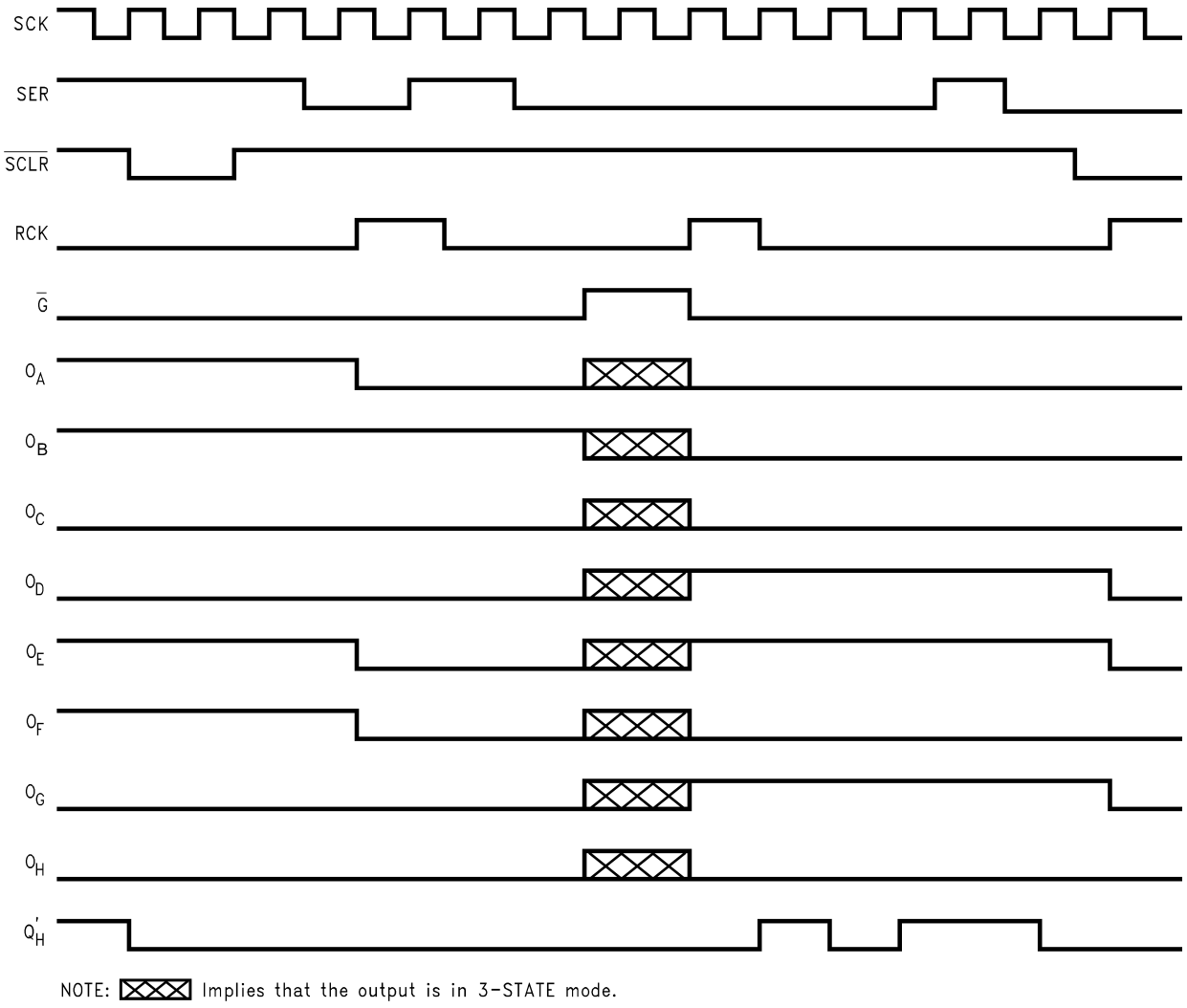


Figure 3. Timing Diagram

Logic Diagram (Positive Logic)

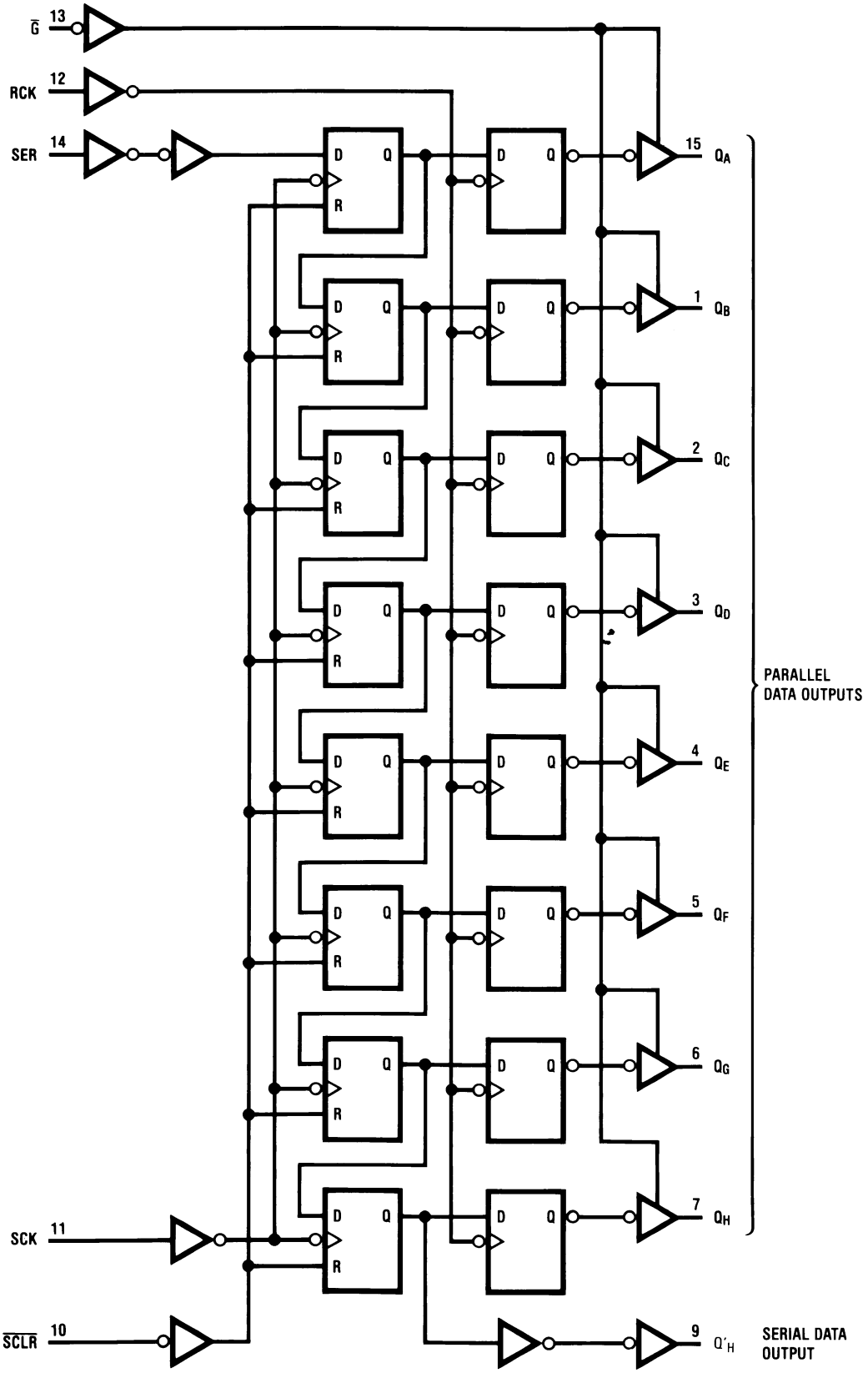


Figure 4. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC}+0.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, Per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 secs		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)	SOIC−16	126	°C/W
		TSSOP−16	159	
P_D	Power Dissipation in Still Air at 25°C	SOIC−16	995	mW
		TSSOP−16	787	
MSL	Moisture Sensitivity		Level 1	−
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.139 in	−
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 4)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V	0	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	0	20	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = 25°C			T_A = −40°C to +85°C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage	2.0			1.5			1.5		V
		3.0 – 5.5			0.7 × V_{CC}			0.7 × V_{CC}		
V_{IL}	LOW Level Input Voltage	2.0					0.50		0.50	V
		3.0 – 5.5					0.3 × V_{CC}		0.3 × V_{CC}	
V_{OH}	HIGH Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	1.9	2.0		1.9		V
		3.0			2.9	3.0		2.9		
		4.5			4.4	4.5		4.4		
		3.0		I_{OH} = −4 mA	2.58			2.48		
		4.5		I_{OH} = −8 mA	3.94			3.80		
V_{OL}	LOW Level Output Voltage	2.0	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA		0.0	0.1		0.1	V
		3.0				0.0	0.1		0.1	
		4.5				0.0	0.1		0.1	
		3.0		I_{OL} = 4 mA			0.36		0.44	
		4.5		I_{OL} = 8 mA			0.36		0.44	
I_{OZ}	3−STATE Output Off−State Current	5.5	V_{IN} = V_{CC} or GND, V_{OUT} = V_{CC} or GND, $V_{IN}\overline{G}$ = V_{IH} or V_{IL}				±0.25		±2.5	μA
I_{IN}	Input Leakage Current	0 – 5.5	V_{IN} = 5.5 V or GND				±0.1		±1.0	μA
I_{CC}	Quiescent Supply Current	5.5	V_{IN} = V_{CC} or GND				4.0		40.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOISE CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions	T_A = 25°C		Unit
				Typ	Limits	
V_{OLP} (Note 5)	Quiet Output Maximum Dynamic V_{OL}	5.0	C_L = 50 pF	0.9	1.2	V
V_{OLV} (Note 5)	Quiet Output Minimum Dynamic V_{OL}	5.0	C_L = 50 pF	−0.9	−1.2	V
V_{IHD} (Note 5)	Minimum HIGH Level Dynamic Input Voltage	5.0	C_L = 50 pF		3.5	V
V_{ILD} (Note 5)	Maximum LOW Level Dynamic Input Voltage	5.0	C_L = 50 pF		1.5	V

5. Parameter guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	V_{CC} (V)	Conditions		T_A = +25°C			T_A = −40°C to +85°C		Unit
					Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Time, RCK to Q_A–Q_H	3.3 ± 0.3		C_L = 15 pF		7.7	11.9	1.0	13.5	ns
				C_L = 50 pF		10.2	15.4	1.0	17.0	
		5.0 ± 0.5		C_L = 15 pF		5.4	7.4	1.0	8.5	ns
				C_L = 50 pF		6.9	9.4	1.0	10.5	
t_{PLH}, t_{PHL}	Propagation Delay Time, SCK–Q'H	3.3 ± 0.3		C_L = 15 pF		8.8	13.0	1.0	15.0	ns
				C_L = 50 pF		11.3	16.5	1.0	18.5	
		5.0 ± 0.5		C_L = 15 pF		6.2	8.2	1.0	9.4	ns
				C_L = 50 pF		7.7	10.2	1.0	11.4	
t_{PHL}	Propagation Delay Time, $\overline{SCLR}$–Q'H	3.3 ± 0.3		C_L = 15 pF		8.4	12.8	1.0	13.7	ns
				C_L = 50 pF		10.9	16.3	1.0	17.2	
		5.0 ± 0.5		C_L = 15 pF		5.9	8.0	1.0	9.1	ns
				C_L = 50 pF		7.4	10.0	1.0	11.1	
t_{PZL}, t_{PZH}	Output Enable Time, $\overline{G}$ to Q_A–Q_H	3.3 ± 0.3	R_L = 1 kΩ	C_L = 15 pF		7.5	11.5	1.0	13.5	ns
				C_L = 50 pF		9.0	15.0	1.0	17.0	
		5.0 ± 0.5		C_L = 15 pF		4.8	8.6	1.0	10.0	ns
				C_L = 50 pF		8.3	10.6	1.0	12.0	
t_{PLZ}, t_{PHZ}	Output Enable Time, $\overline{G}$ to Q_A–Q_H	3.3 ± 0.3	R_L = 1 kΩ	C_L = 50 pF		12.1	15.7	1.0	16.2	ns
		5.0 ± 0.5		C_L = 50 pF		7.6	10.3	1.0	11.0	
f_{MAX}	Maximum Clock Frequency	3.3 ± 0.3		C_L = 15 pF	80	150		70		MHz
				C_L = 50 pF	55	130		50		
		5.0 ± 0.5		C_L = 15 pF	135	185		115		MHz
				C_L = 50 pF	95	155		85		
t_{OSLH}, t_{OSHL}	Output to Output Skew	3.3 ± 0.3	(Note 6)	C_L = 50 pF			1.5		1.5	ns
		5.0 ± 0.5		C_L = 50 pF			1.0		1.0	
C_{IN}	Input Capacitance		V_{CC} = Open			5.0	10		10	pF
C_{OUT}	Output Capacitance		V_{CC} = 5.0 V			6.0				pF
C_{PD}	Power Dissipation Capacitance		(Note 7)			87				pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Parameter guaranteed by design. $t_{OSLH} = |t_{PLH}\ max - t_{PLH}\ min|$; $t_{OSHL} = |t_{PHL}\ max - t_{PHL}\ min|$.
7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:
   $I_{CC}\ (Opr.) = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}$

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC} (V)	T_A = 25°C		T_A = −40°C to +85°C	Unit
			Typ	Guaranteed Minimum		
t_S	Minimum Setup Time (SER–SCK)	3.3 ± 0.3		3.5	3.5	ns
		5.0 ± 0.5		3.0	3.0	
t_S	Minimum Setup Time (SCK–RCK)	3.3 ± 0.3		8.0	8.5	ns
		5.0 ± 0.5		5.0	5.0	
t_S	Minimum Setup Time ($\overline{SCLR}$–RCK)	3.3 ± 0.3		8.0	9.0	ns
		5.0 ± 0.5		5.0	5.0	
t_H	Minimum Hold Time (SER–SCK)	3.3 ± 0.3		1.5	1.5	ns
		5.0 ± 0.5		2.0	2.0	
t_H	Minimum Hold Time (SCK–RCK)	3.3 ± 0.3		0.0	0.0	ns
		5.0 ± 0.5		0.0	0.0	
t_H	Minimum Hold Time ($\overline{SCLR}$–RCK)	3.3 ± 0.3		0.0	0.0	ns
		5.0 ± 0.5		0.0	0.0	
$t_{W(L)}$	Minimum Pulse Width ($\overline{SCLR}$)	3.3 ± 0.3		5.0	5.0	ns
		5.0 ± 0.5		5.0	5.0	
$t_{W(L)}$, $t_{W(H)}$	Minimum Pulse Width (SCK)	3.3 ± 0.3		5.0	5.0	ns
		5.0 ± 0.5		5.0	5.0	
$t_{W(L)}$, $t_{W(H)}$	Minimum Pulse Width (RCK)	3.3 ± 0.3		5.0	5.0	ns
		5.0 ± 0.5		5.0	5.0	
t_{rem}	Minimum Removal Time ($\overline{SCLR}$–SCK)	3.3 ± 0.3		3.0	3.0	ns
		5.0 ± 0.5		2.5	2.5	

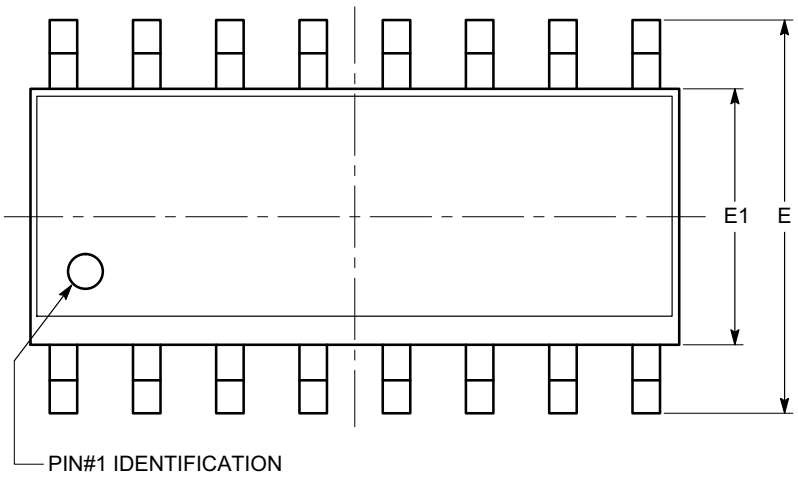
ORDERING INFORMATION

Device	Marking	Package	Shipping†
74VHC595MX	VHC595G	SOIC−16	2500 Units / Tape & Reel
74VHC595MTCX	VHC 595	TSSOP−16	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

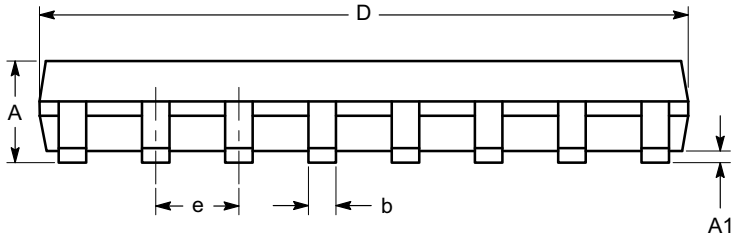
SOIC−16, 150 mils
CASE 751BG−01
ISSUE O

DATE 19 DEC 2008

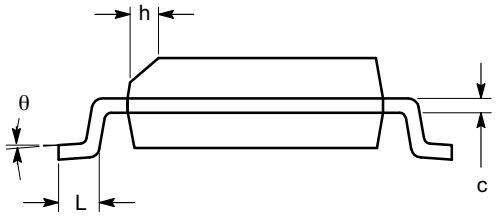


TOP VIEW

SYMBOL	MIN	NOM	MAX
A	1.35		1.75
A1	0.10		0.25
b	0.33		0.51
c	0.19		0.25
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27 BSC	
h	0.25		0.50
L	0.40		1.27
θ	0º		8º



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MS-012.

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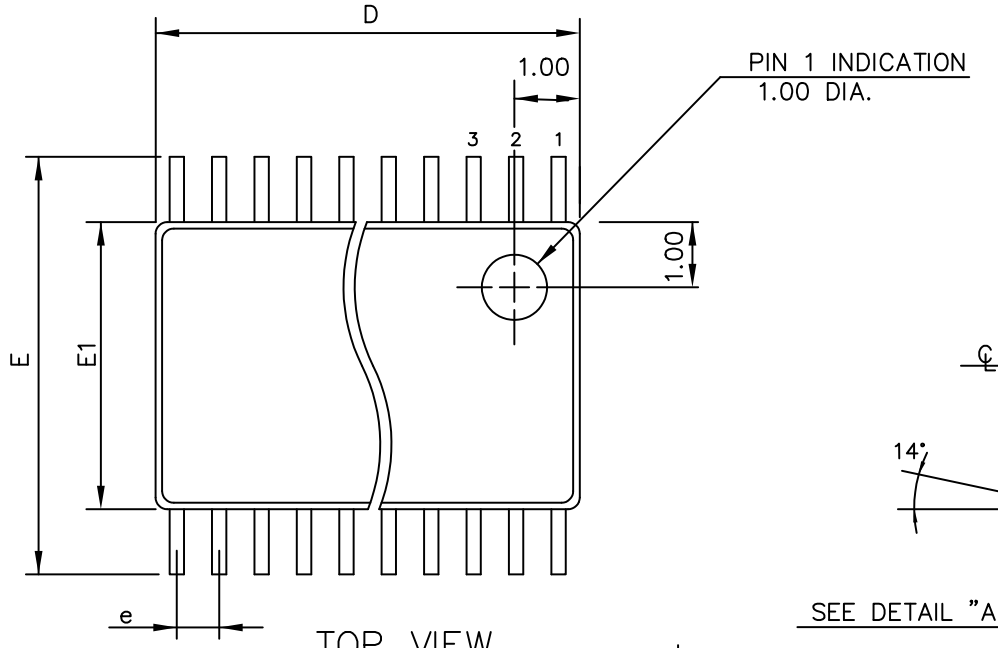
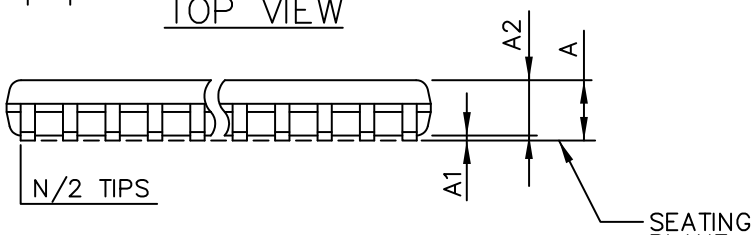
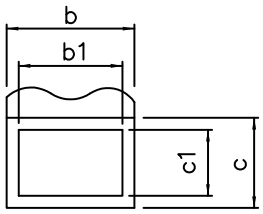


TOP VIEW

END VIEW



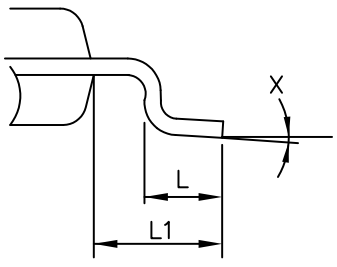
SIDE VIEW



SECTION "B–B"

THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS			NOTE VARIATIONS	D	N
	MIN.	NOM.	MAX.			
A	——	——	1.10	AA/AAT	3.00 BSC	8
A_1	0.05	——	0.15	AB–1/ABT	5.00 BSC	14
A_2	0.85	0.90	0.95	AB/ABT	5.00 BSC	16
b	0.19	–	0.30	AD/ADT	7.80 BSC	24
b1	0.19	0.22	0.25			
c	0.09	–	0.20			
c1	0.09	0.127	0.16			
D	SEE VARIATIONS					
E1	4.30	4.40	4.50			
e	0.65 BSC					
E	6.40 BSC					
L	0.50	0.60	0.70			
L1	1.00 REF					
N	SEE VARIATIONS					
X	0°	——	8°			



DETAIL 'A'

ALL DIMENSIONS IN MILLIMETERS

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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