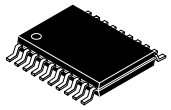
Octal D-Type Latch with 3-STATE Outputs

74VHC573



TSSOP20, 4.4x6.5
CASE 948AQ

General Description

The VHC573 is an advanced high speed CMOS octal latch with 3−STATE output fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. This 8−bit D−type latch is controlled by a latch enable input (LE) and an Output Enable input ($\overline{OE}$). When the $\overline{OE}$ input is HIGH, the eight outputs are in a high impedance state.

An input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

Features

- High Speed: t_{PD} = 5.0 ns (Typ) at V_{CC} = 5 V
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28% V_{CC} (Min)
- Power Down Protection is Provided on All Inputs
- Low Noise: V_{OLP} = 0.6 V (Typ)
- Low Power Dissipation: I_{CC} = 4 μA (Max) @ T_A = 25 °C
- Pin and Function Compatible with 74HC573
- This is a Pb−Free Device

Logic Symbol

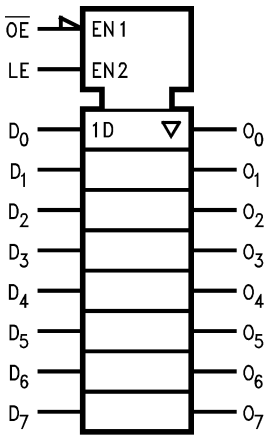
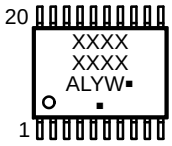


Figure 1. Logic Symbol

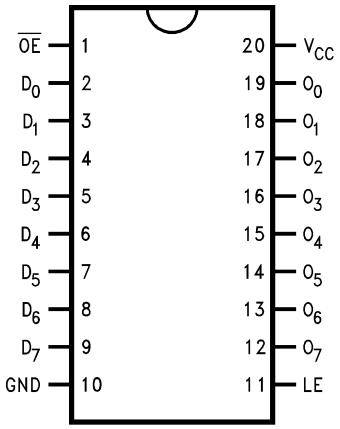
MARKING DIAGRAM



XXXXXX	= Specific Device Code
A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

Pin Names	Description
D_0–D_7	Data Inputs
LE	Latch Enable Input
$\overline{OE}$	3−STATE Output Enable Input
O_0–O_7	3−STATE Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

TRUTH TABLE

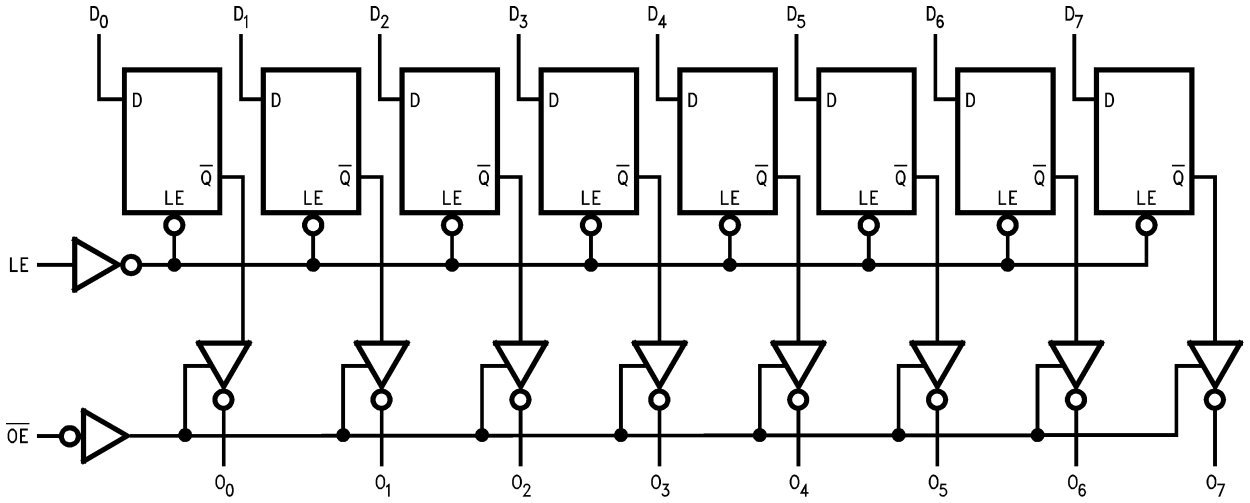
Inputs			Outputs
$\overline{OE}$	LE	D	O_n
L	H	H	H
L	H	L	L
L	L	X	O_0
H	X	X	Z

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

Functional Description

The VHC573 contains eight D−type latches with 3−STATE output buffers. When the Latch Enable (LE) input is HIGH, data on the Dn inputs enters the latches. In this condition the latches are transparent, i.e., a latch output will change state each time its D input changes. When LE is LOW the latches store the information that was present on the D inputs, a setup time preceding the HIGH−to−LOW transition of LE. The 3−STATE buffers are controlled by the Output Enable ($\overline{OE}$) input. When $\overline{OE}$ is LOW, the buffers are enabled. When $\overline{OE}$ is HIGH the buffers are in the high impedance mode, but, this does not interfere with entering new data into the latches.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage		−0.5 to V_{CC} + 0.5	V
I_{IN}	DC Input Current		±20	mA
I_{OUT}	DC Output Current		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		±20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		150	°C/W
P_D	Power Dissipation in Still Air at 25 °C		833	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.573 in	
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model	2000	V
		Charged Device Model	N/A	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri−stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm−by−114 mm, 2−ounce copper trace no air flow per JESD51−7.
3. HBM tested to EIA / JESD22−A114−A. CDM tested to JESD22−C101−A. JEDEC recommends that ESD qualification to EIA/JESD22−A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 4)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)		0	V_{CC}	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise or Fall Rate	V_{CC} = 3.0 V to 3.6 V	0	100	ns/V
		V_{CC} = 4.5 V to 5.5 V	0	20	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V_{CC} (V)	T_A = 25 °C			T_A = −40 °C to +85 °C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage			2.0	1.50	–	–	1.50	–	V
				3.0–5.5	0.7 x V_{CC}	–	–	0.7 x V_{CC}	–	
V_{IL}	LOW Level Input Voltage			2.0	–	–	0.50	–	0.50	V
				3.0–5.5	–	–	0.3 x V_{CC}	–	0.3 x V_{CC}	
V_{OH}	HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = –50 μA	2.0	1.9	2.0	–	1.9	–	V
				3.0	2.9	3.0	–	2.9	–	
				4.5	4.4	4.5	–	4.4	–	
			I_{OH} = –4 mA	3.0	2.58	–	–	2.48	–	
			I_{OH} = –8 mA	4.5	3.94	–	–	3.80	–	
V_{OL}	LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	2.0	–	0.0	0.1	–	0.1	V
				3.0	–	0.0	0.1	–	0.1	
				4.5	–	0.0	0.1	–	0.1	
			I_{OL} = 4 mA	3.0	–	–	0.36	–	0.44	
			I_{OL} = 8 mA	4.5	–	–	0.36	–	0.44	
I_{OZ}	3−STATE Output Off−State Current	V_{IN} = V_{IH} or V_{IL}, V_{OUT} = V_{CC} or GND		5.5	–	–	±0.25	–	±2.5	μA
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND		0–5.5	–	–	±0.1	–	±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND		5.5	–	–	4.0	–	40.0	μA

NOISE CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25 °C		Unit
				Typ	Limits	
V_{OLP} (Note 5)	Quiet Output Maximum Dynamic V_{OL}	C_L = 50 pF	5.0	0.9	1.2	V
V_{OLV} (Note 5)	Quiet Output Minimum Dynamic V_{OL}	C_L = 50 pF	5.0	–0.8	–1.0	V
V_{IHD} (Note 5)	Minimum HIGH Level Dynamic Input Voltage	C_L = 50 pF	5.0	–	3.5	V
V_{ILD} (Note 5)	Maximum LOW Level Dynamic Input Voltage	C_L = 50 pF	5.0	–	1.5	V

5. Parameter guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V_{CC} (V)	T_A = 25 °C			T_A = −40 °C to +85 °C		Unit
					Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay Time (LE to O_n)		C_L = 15 pF	3.3 ±0.3	−	7.6	11.9	1.0	14.0	ns
			C_L = 50 pF		−	10.1	15.4	1.0	17.5	
			C_L = 15 pF	5.0 ±0.5	−	5.0	7.7	1.0	9.0	ns
			C_L = 50 pF		−	6.5	9.7	1.0	11.0	
t_{PLH}, t_{PHL}	Propagation Delay Time (D−O_n)		C_L = 15 pF	3.3 ±0.3	−	7.0	11.0	1.0	13.0	ns
			C_L = 50 pF		−	9.5	14.5	1.0	16.5	
			C_L = 15 pF	5.0 ±0.5	−	4.5	6.8	1.0	8.0	
			C_L = 50 pF		−	6.0	8.8	1.0	10.0	
t_{PZL}, t_{PZH}	3−STATE Output Enable Time	R_L = 1 kΩ	C_L = 15 pF	3.3 ±0.3	−	7.3	11.5	1.0	13.5	ns
			C_L = 50 pF		−	9.8	15.0	1.0	17.0	
			C_L = 15 pF	5.0 ±0.5	−	5.2	7.7	1.0	9.0	ns
			C_L = 50 pF		−	6.7	9.7	1.0	11.0	
t_{PLZ}, t_{PHZ}	3−STATE Output Disable Time	R_L = 1 kΩ	C_L = 50 pF	3.3 ±0.3	−	10.7	14.5	1.0	16.5	ns
			C_L = 50 pF	5.0 ±0.5	−	6.7	9.7	1.0	11.0	
t_{OSLH}, t_{OSHL}	Output to Output Skew	(Note 6)	C_L = 50 pF	3.3 ±0.3	−	−	1.5	−	1.5	ns
			C_L = 50 pF	5.0 ±0.5	−	−	1.0	−	1.0	
C_{IN}	Input Capacitance	V_{CC} = Open			−	4	10	−	10	pF
C_{OUT}	Output Capacitance	V_{CC} = 5.0 V			−	6	−	−	−	pF
C_{PD}	Power Dissipation Capacitance	(Note 7)			−	29	−	−	−	pF

6. Parameter guaranteed by design. $t_{OSLH} = |t_{PLH\ max} - t_{PLH\ min}|$; $t_{OSHL} = |t_{PHL\ max} - t_{PHL\ min}|$
7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr.) = $C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 8$ (per Latch). The total C_{PD} when n pcs. of the Latch operates can be calculated by the equation: C_{PD} (total) = 21 + 8n.

AC OPERATING REQUIREMENTS

Symbol	Parameter	V_{CC} (V)	T_A = 25 °C			T_A = −40 °C to +85 °C		Unit
			Min	Typ	Max	Min	Max	
t_W(H), t_W(L)	Minimum Pulse Width (LE)	3.3 ±0.3	5.0	−	−	5.0	−	ns
		5.0 ±0.5	5.0	−	−	5.0	−	
t_S	Minimum Setup Time	3.3 ±0.3	3.5	−	−	3.5	−	ns
		5.0 ±0.5	3.5	−	−	3.5	−	
t_H	Minimum Hold Time	3.3 ±0.3	1.5	−	−	1.5	−	ns
		5.0 ±0.5	1.5	−	−	1.5	−	

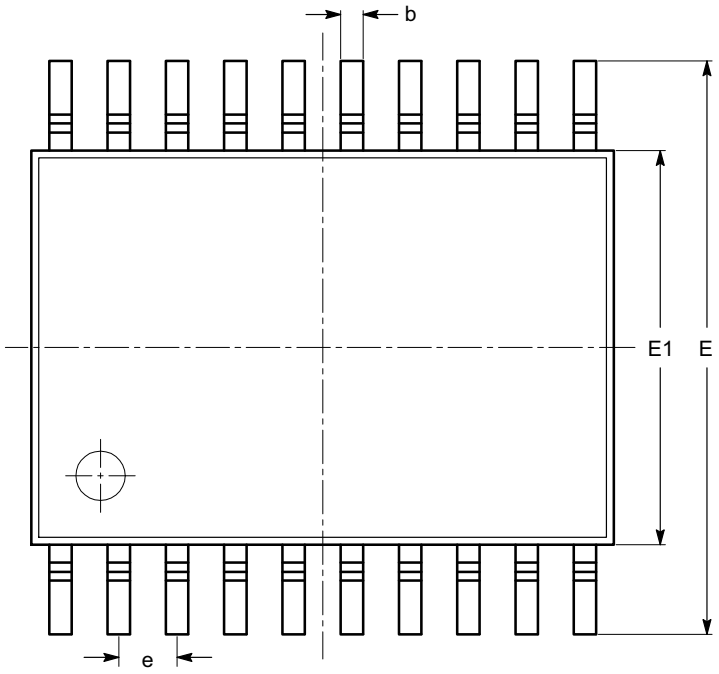
ORDERING INFORMATION

Device	Marking	Package	Shipping†
74VHC573MTC	VHC 573	TSSOP20 (Pb−Free)	75 Units / Tube
74VHC573MTCX	VHC 573	TSSOP20 (Pb−Free)	2500 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

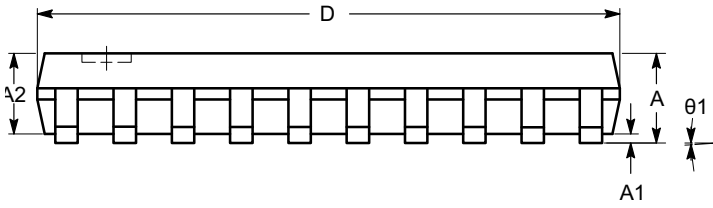
TSSOP20, 4.4x6.5
CASE 948AQ
ISSUE A

DATE 19 MAR 2009

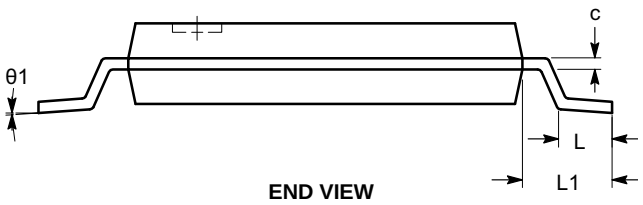


TOP VIEW

SYMBOL	MIN	NOM	MAX
A			1.20
A1	0.05		0.15
A2	0.80		1.05
b	0.19		0.30
c	0.09		0.20
D	6.40	6.50	6.60
E	6.30	6.40	6.50
E1	4.30	4.40	4.50
e		0.65 BSC	
L	0.45	0.60	0.75
L1		1.00 REF	
θ	0°		8°



SIDE VIEW



END VIEW

Notes:
(1) All dimensions are in millimeters. Angles in degrees.
(2) Complies with JEDEC MO-153.

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