

Low Voltage Quad 2-Input NAND Schmitt Trigger

74LVX132

General Description

The LVX132 contains four 2-input NAND Schmitt Trigger Gates. The pin configuration and function are the same as the LVX00 but the inputs have hysteresis between the positive-going and negative-going input thresholds, which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals, thus providing greater noise margins than conventional gates.

The inputs tolerate voltages up to 6.5 V allowing the interface of 5 V systems to 3 V systems.

Features

- Input Voltage Level Translation from 5 V to 3 V
- Ideal for Low Power/Low Noise 3.3 V Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Pb-Free, Halogen Free/BFR Free and RoHS Compliant

Logic Diagram

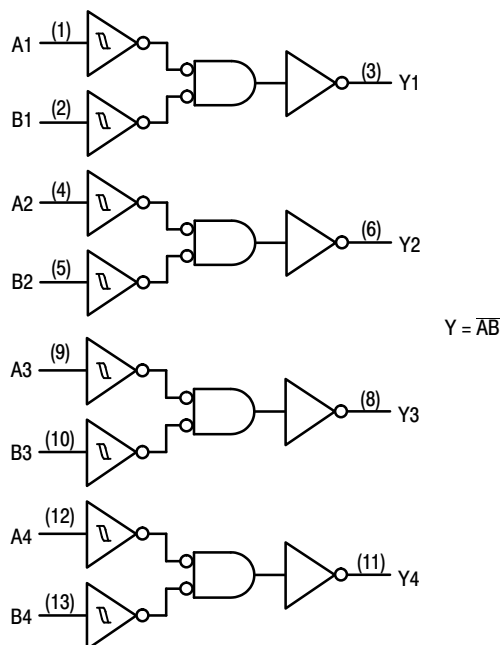
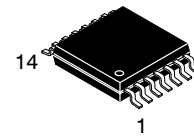
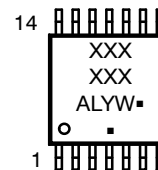


Figure 1. Logic Diagram



TSSOP-14 WB
CASE 948G

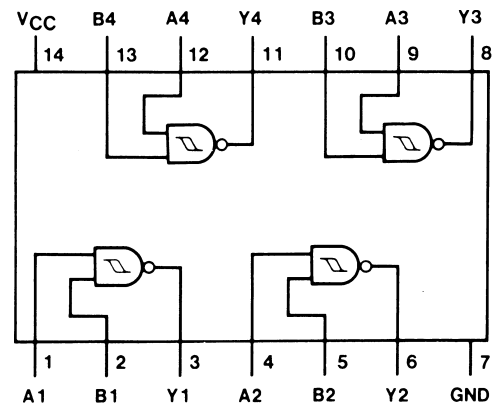
MARKING DIAGRAM



- XXXXX = Specific Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

| Pin Names | Description |
|------------|-------------|
| A_n, B_n | Inputs |
| Y_n | Outputs |

ORDERING INFORMATION

See detailed ordering and shipping information on page 4 of this data sheet.

74LVX132

MAXIMUM RATINGS

| Symbol | Parameter | Value | Unit |
|-----------------------|---|------------------------|--------------|
| V_{CC} | Supply Voltage | -0.5 to +6.5 | V |
| I_{IK} | DC Input Diode Current, $V_I = -0.5$ V | -20 | mA |
| V_I | DC Input Voltage | -0.5 to +6.5 | V |
| I_{OK} | DC Output Diode Current $V_O = -0.5$ V $V_O = V_{CC} + 0.5$ V | -20 +20 | mA |
| V_O | DC Output Voltage | -0.5 to $V_{CC} + 0.5$ | V |
| I_O | DC Output Source or Sink Current | ± 25 | mA |
| I_{CC} or I_{GND} | DC V_{CC} or Ground Current | ± 50 | mA |
| T_{STG} | Storage Temperature | -65 to +150 | $^{\circ}$ C |
| P_D | Power Dissipation | 833 | mW |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS (Note 1)

| Symbol | Parameter | Min | Max | Unit |
|-----------------------|--------------------------|-----|----------|--------------|
| V_{CC} | Supply Voltage | 2.0 | 3.6 | V |
| V_I | Input Voltage | 0 | 5.5 | V |
| V_O | Output Voltage | 0 | V_{CC} | V |
| T_A | Operating Temperature | -40 | +85 | $^{\circ}$ C |
| $\Delta t / \Delta V$ | Input Rise and Fall Time | 0 | 100 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

1. Unused inputs must be held HIGH or LOW. They may not float.

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DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Unit | |
|-----------------|---------------------------|---------------------|--|--------------------------|------|------|---------------------------------|------|------|---|
| | | | | Min | Typ | Max | Min | Max | | |
| V _{t+} | Positive Threshold | 3.0 | | - | - | 2.2 | - | 2.2 | V | |
| V _{t-} | Negative Threshold | 3.0 | | 0.9 | - | - | 0.9 | - | V | |
| V _H | Hysteresis | 3.0 | | 0.3 | - | 1.2 | 0.3 | 1.2 | V | |
| V _{OH} | HIGH Level Output Voltage | 2.0 | V _{IN} = V _{IL} or V _{IH} | I _{OH} = -50 μA | 1.9 | 2.0 | - | 1.9 | - | V |
| | | 3.0 | | I _{OH} = -50 μA | 2.9 | 3.0 | - | 2.9 | - | |
| | | 3.0 | | I _{OH} = -4 mA | 2.58 | - | - | 2.48 | - | |
| V _{OL} | LOW Level Output Voltage | 2.0 | V _{IN} = V _{IL} or V _{IH} | I _{OL} = 50 μA | - | 0.0 | 0.1 | - | 0.1 | V |
| | | 3.0 | | I _{OL} = 50 μA | - | 0.0 | 0.1 | - | 0.1 | |
| | | 3.0 | | I _{OL} = 4 mA | - | - | 0.36 | - | 0.44 | |
| I _{IN} | Input Leakage Current | 3.6 | V _{IN} = 5.5 V or GND | - | - | ±0.1 | - | ±1.0 | μA | |
| I _{CC} | Quiescent Supply Current | 3.6 | V _{IN} = V _{CC} or GND | - | - | 2.0 | - | 20.0 | μA | |

NOISE CHARACTERISTICS (Note 2)

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | Unit |
|------------------|--|---------------------|------------------------|-----------------------|-------|------|
| | | | | Typ | Limit | |
| V _{OLP} | Quiet Output Maximum Dynamic V _{OL} | 3.3 | C _L = 50 pF | 0.3 | 0.5 | V |
| V _{OLV} | Quiet Output Minimum Dynamic V _{OL} | 3.3 | C _L = 50 pF | -0.3 | -0.5 | V |
| V _{IHD} | Minimum HIGH Level Dynamic Input Voltage | 3.3 | C _L = 50 pF | - | 2.0 | V |
| V _{ILD} | Maximum LOW Level Dynamic Input Voltage | 3.3 | C _L = 50 pF | - | 0.8 | V |

2. Input $t_r = t_f = 3$ ns

AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Unit |
|---------------------------------------|--------------------------------|---------------------|------------------------|-----------------------|------|------|---------------------------------|------|------|
| | | | | Min | Typ | Max | Min | Max | |
| t _{PLH} , t _{PHL} | Propagation Delay Time | 2.7 | C _L = 15 pF | - | 7.0 | 11.5 | 1.0 | 13.0 | ns |
| | | | C _L = 50 pF | - | 10.5 | 16.0 | 1.0 | 18.7 | |
| | | 3.3 ± 0.3 | C _L = 15 pF | - | 6.1 | 10.6 | 1.0 | 12.5 | ns |
| | | | C _L = 50 pF | - | 9.0 | 15.4 | 1.0 | 17.5 | |
| t _{OSLH} , t _{OSSL} | Output to Output Skew (Note 3) | 2.7 | C _L = 50 pF | - | - | 1.5 | - | 1.5 | ns |
| | | 3.3 | | - | - | 1.5 | - | 1.5 | |

3. Parameter guaranteed by design $t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSSL} = |t_{PHLm} - t_{PHLn}|$

CAPACITANCE

| Symbol | Parameter | Conditions | T _A = 25°C | | | T _A = -40°C to +85°C | | Unit |
|-----------------|--|------------|-----------------------|-----|-----|---------------------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | |
| C _{IN} | Input Capacitance | | - | 4 | 10 | - | 10 | pF |
| C _{PD} | Power Dissipation Capacitance (Note 4) | | - | 18 | - | - | - | pF |

4. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC(opr.)} = (C_{PD} \times V_{CC} \times f_{IN} \times I_{CC}) / 6 \text{ (per Gate)}$$

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ORDERING INFORMATION

| Device Order Number | Top Marking | Package Type | Shipping [†] |
|---------------------|-------------|---------------------------------------|--------------------------|
| 74LVX132MTCX | LVX 132 | TSSOP-14 WB (Pb-Free, Halide Free) | 2500 units / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
- DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
- DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
- DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
- DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.



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|-------------------------|--------------------|--|
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| DESCRIPTION: | TSSOP-14 WB | PAGE 1 OF 1 |

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