

Low Voltage Quad 2-Input OR Gate with 5 V Tolerant Inputs

74LCX32

The LCX32 contains four 2-input OR gates. The inputs tolerate voltages up to 7 V allowing the interface of 5 V systems to 3 V systems.

The 74LCX32 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

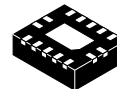
- 5 V Tolerant Inputs
- 2.3 V – 3.6 V V_{CC} Specifications Provided
- 5.5 ns t_{PD} Max. ($V_{CC} = 3.3$ V), 10 mA I_{CC} Max.
- Power Down High Impedance Inputs and Outputs
- ± 24 mA Output Drive ($V_{CC} = 3.0$ V)
- Implements Proprietary Noise/EMI Reduction Circuitry
- Latch-up Performance Exceeds JEDEC 78 Conditions
- ESD performance:
 - ◆ Human Body Model >2000 V
 - ◆ Machine model >150 V
- Available on SOIC, TSSOP WB and Leadless QFN Packages
- These are Pb-Free Devices



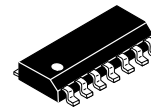
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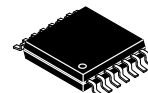
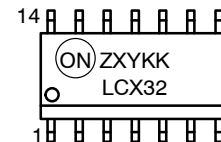
MARKING DIAGRAM



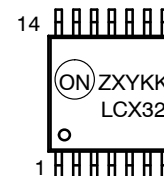
QFN14 3.0x2.5, 0.5P
CASE 510CB



SOIC14
CASE 751EF



TSSOP-14 WB
CASE 948G



LCX32 = Specific Device Code
 Z = Assembly Plant Code
 XY = Date Code
 KK = Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

74LCX32

CONNECTION DIAGRAMS

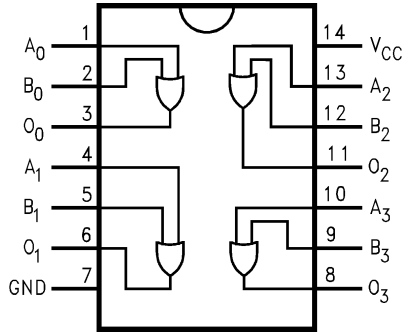


Figure 1. Pin Assignments for SOIC and TSSOP

LOGIC SYMBOL

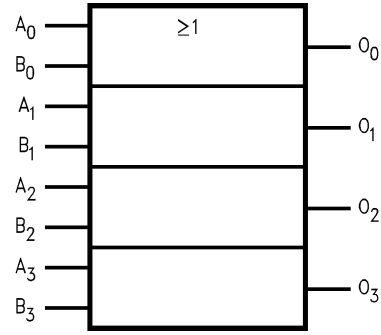


Figure 3. IEEE/IEC

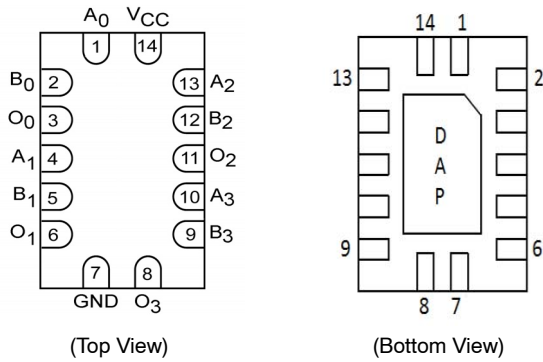


Figure 2. Pad Assignments for DQFN

PIN DESCRIPTION

| Pin Names | Description |
|------------|-------------|
| A_n, B_n | Inputs |
| O_n | Outputs |
| DAP | No Connect |

1. DAP (Die Attach Pad)

ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Rating |
|-----------|---|----------------------------|
| V_{CC} | Supply Voltage | -0.5 V to +7.0 V |
| V_I | DC Input Voltage | -0.5 V to +7.0 V |
| V_O | DC Output Voltage, Output in HIGH or LOW State (Note 2) | -0.5 V to $V_{CC} + 0.5$ V |
| I_{IK} | DC Input Diode Current, $V_I < GND$ | -50 mA |
| I_{OK} | DC Output Diode Current $V_O < GND$ | -50 mA |
| | $V_O > V_{CC}$ | +50 mA |
| I_O | DC Output Source/Sink Current | ±50 mA |
| I_{CC} | DC Supply Current per Supply Pin | ±100 mA |
| I_{GND} | DC Ground Current per Ground Pin | ±100 mA |
| T_{STG} | Storage Temperature | -65°C to +150°C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. I_O Absolute Maximum Rating must be observed.

74LCX32

RECOMMENDED OPERATING CONDITIONS (Note 3)

| Symbol | Parameter | Min | Max | Unit |
|-----------------------------------|---|-----|-----------------|------|
| V _{CC} | Supply Voltage Operating | 2.0 | 3.6 | V |
| | Data Retention | 1.5 | 3.6 | |
| V _I | Input Voltage | 0 | 5.5 | V |
| V _O | Output Voltage, HIGH or LOW State | 0 | V _{CC} | V |
| I _{OH} / I _{OL} | Output Current V _{CC} = 3.0 V – 3.6 V | – | ±24 | mA |
| | V _{CC} = 2.7 V – 3.0 V | – | ±12 | |
| | V _{CC} = 2.3 V – 2.7 V | – | ±8 | |
| T _A | Free-Air Operating Temperature | –40 | 85 | °C |
| Δt / ΔV | Input Edge Rate, V _{IN} = 0.8 V – 2.0 V, V _{CC} = 3.0 V | 0 | 10 | ns/V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. Unused inputs must be held HIGH or LOW. They may not float.

DC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | V _{CC} (V) | Conditions | –40°C to 85°C | | Unit |
|------------------|---------------------------------------|---------------------|---|-----------------------|------|------|
| | | | | Min | Max | |
| V _{IH} | HIGH Level Input Voltage | 2.3 – 2.7 | | 1.7 | – | V |
| | | 2.7 – 3.6 | | 2.0 | – | |
| V _{IL} | LOW Level Input Voltage | 2.3 – 2.7 | | – | 0.7 | V |
| | | 2.7 – 3.6 | | – | 0.8 | |
| V _{OH} | HIGH Level Output Voltage | 2.3 – 3.6 | I _{OH} = –100 μA | V _{CC} – 0.2 | – | V |
| | | 2.3 | I _{OH} = –8 mA | 1.8 | – | |
| | | 2.7 | I _{OH} = –12 mA | 2.2 | – | |
| | | 3.0 | I _{OH} = –18 mA | 2.4 | – | |
| | | | I _{OH} = –24 mA | 2.2 | – | |
| V _{OL} | LOW Level Output Voltage | 2.3 – 3.6 | I _{OL} = 100 μA | – | 0.2 | V |
| | | 2.3 | I _{OL} = 8 mA | – | 0.6 | |
| | | 2.7 | I _{OL} = 12 mA | – | 0.4 | |
| | | 3.0 | I _{OL} = 16 mA | – | 0.4 | |
| | | | I _{OL} = 24 mA | – | 0.55 | |
| I _I | Input Leakage Current | 2.3 – 3.6 | 0 ≤ V _I ≤ 5.5 V | – | ±5.0 | μA |
| I _{OFF} | Power-Off Leakage Current | 0 | V _I or V _O = 5.5 V | – | 10 | μA |
| I _{CC} | Quiescent Supply Current | 2.3 – 3.6 | V _I = V _{CC} or GND | – | 10 | μA |
| | | | 3.6 V ≤ V _I ≤ 5.5 V | – | ±10 | |
| ΔI _{CC} | Increase in I _{CC} per Input | 2.3 – 3.6 | V _{IH} = V _{CC} – 0.6 V | – | 500 | μA |

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AC ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | $T_A = -40^\circ\text{C to } +85^\circ\text{C, } R_L = 500 \Omega$ | | | | | | Unit |
|----------------------|--------------------------------|--|-----|--|-----|--|-----|------|
| | | $V_{CC} = 3.3 \text{ V} + 0.3 \text{ V, } C_L = 50 \text{ pF}$ | | $V_{CC} = 2.7 \text{ V, } C_L = 50 \text{ pF}$ | | $V_{CC} = 2.5 \text{ V} + 0.2 \text{ V, } C_L = 30 \text{ pF}$ | | |
| | | Min | Max | Min | Max | Min | Max | |
| t_{PHL}, t_{PLH} | Propagation Delay | 1.5 | 5.5 | 1.5 | 6.2 | 1.5 | 6.6 | ns |
| t_{OSHL}, t_{OSLH} | Output to Output Skew (Note 4) | - | 1.0 | - | - | - | - | ns |

4. Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

DYNAMIC SWITCHING CHARACTERISTICS

| Symbol | Parameter | V_{CC} (V) | Conditions | $T_A = 25^\circ\text{C}$ | Unit |
|-----------|--------------------------------------|--------------|---|--------------------------|------|
| | | | | Typical | |
| V_{OLP} | Quiet Output Dynamic Peak V_{OL} | 3.3 | $C_L = 50 \text{ pF, } V_{IH} = 3.3 \text{ V, } V_{IL} = 0 \text{ V}$ | 0.8 | V |
| | | 2.5 | $C_L = 30 \text{ pF, } V_{IH} = 2.5 \text{ V, } V_{IL} = 0 \text{ V}$ | 0.6 | |
| V_{OLV} | Quiet Output Dynamic Valley V_{OL} | 3.3 | $C_L = 50 \text{ pF, } V_{IH} = 3.3 \text{ V, } V_{IL} = 0 \text{ V}$ | -0.8 | V |
| | | 2.5 | $C_L = 30 \text{ pF, } V_{IH} = 2.5 \text{ V, } V_{IL} = 0 \text{ V}$ | -0.6 | |

CAPACITANCE

| Symbol | Parameter | Conditions | Typical | Unit |
|-----------|-------------------------------|--|---------|------|
| C_{IN} | Input Capacitance | $V_{CC} = \text{Open, } V_I = 0 \text{ V or } V_{CC}$ | 7 | pF |
| C_{OUT} | Output Capacitance | $V_{CC} = 3.3 \text{ V, } V_I = 0 \text{ V or } V_{CC}$ | 8 | pF |
| C_{PD} | Power Dissipation Capacitance | $V_{CC} = 3.3 \text{ V, } V_I = 0 \text{ V or } V_{CC, } f = 10 \text{ MHz}$ | 25 | pF |

AC LOADING AND WAVEFORMS (GENERIC FOR LCX FAMILY)

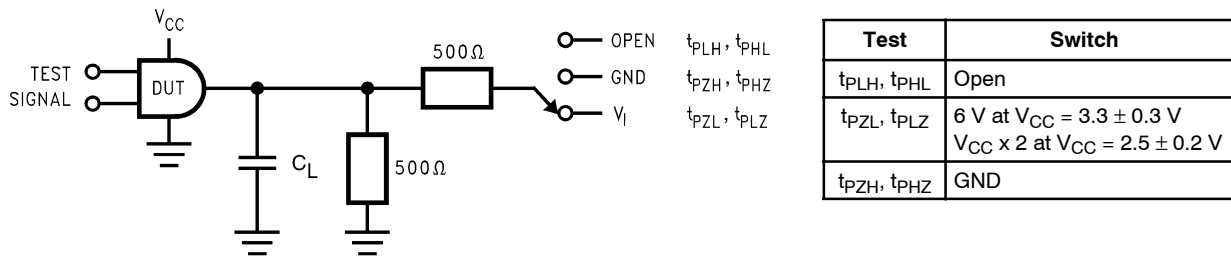
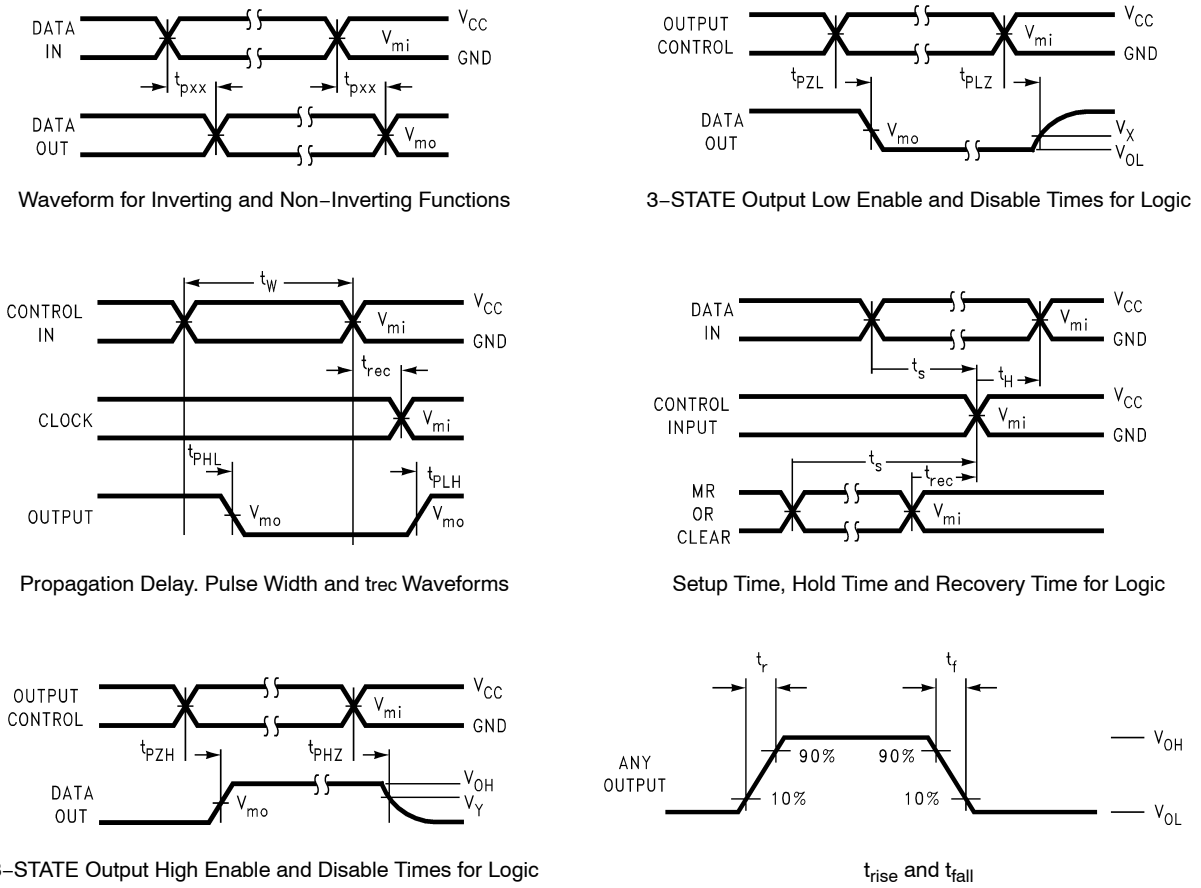


Figure 4. AC Test Circuit (CL Includes Probe and Jig Capacitance)



| Symbol | V_{CC} | | |
|----------|-------------------|------------------|-------------------|
| | 3.3 V \pm 0.3 V | 2.7 V | 2.5 V \pm 0.2 V |
| V_{mi} | 1.5 V | 1.5 V | $C_C/2$ |
| V_{mo} | 1.5 V | 1.5 V | $C_C/2$ |
| V_x | $V_{OL} + 0.3$ V | $V_{OL} + 0.3$ V | $V_{OL} + 0.15$ V |
| V_y | $V_{OH} - 0.3$ V | $V_{OH} - 0.3$ V | $V_{OH} - 0.15$ V |

Figure 5. Waveforms (Input Characteristics; $f = 1$ MHz, $t_r = t_f = 3$ ns)

74LCX32

SCHEMATIC DIAGRAM (GENERIC FOR LCX FAMILY)

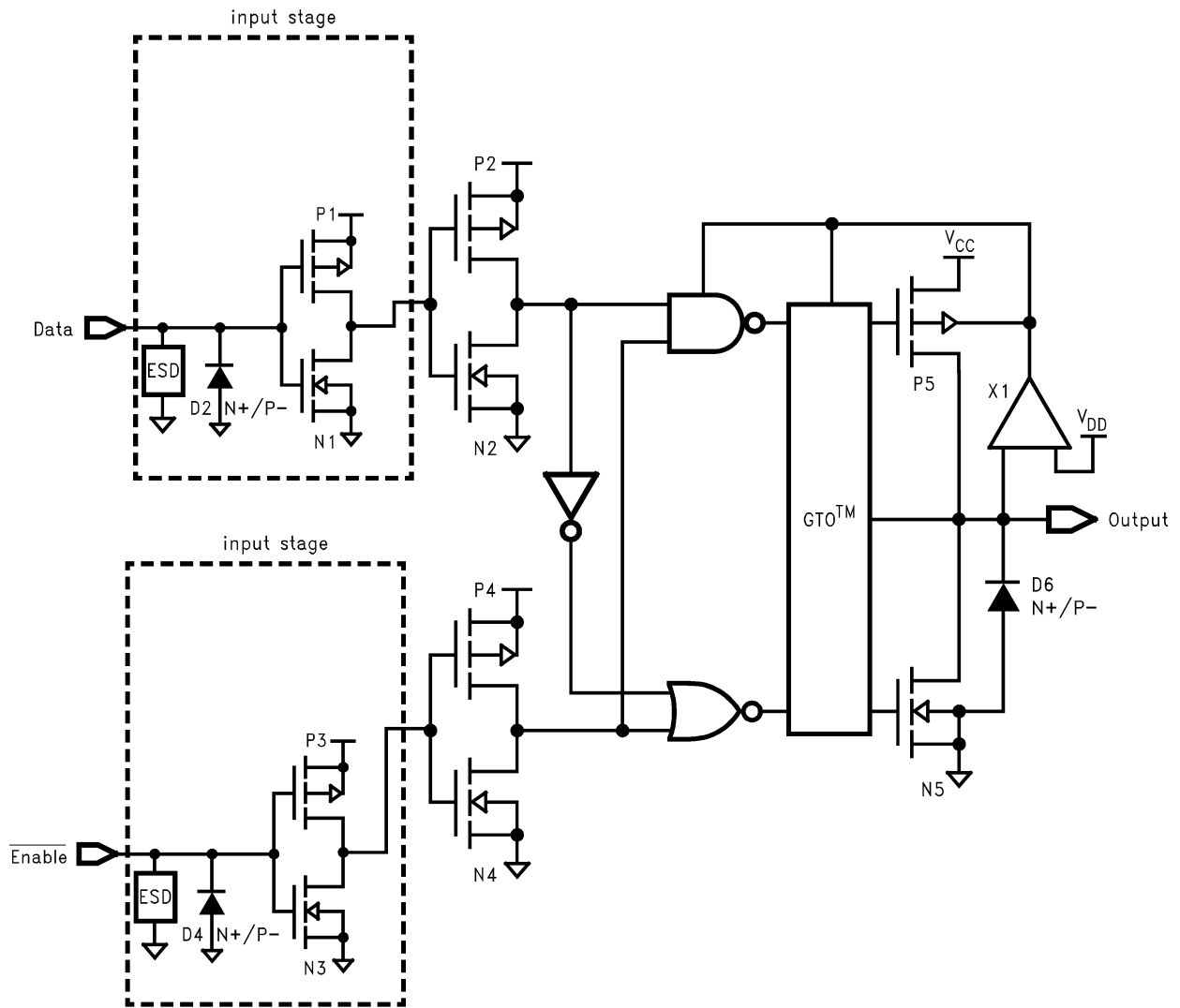


Figure 6. Schematic Diagram (Generic for LCX Family)

74LCX32

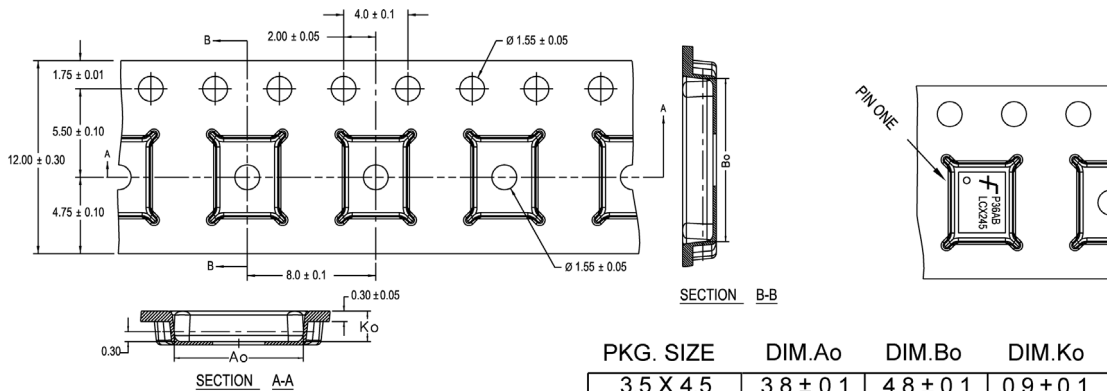
TAPE AND REEL SPECIFICATION

Tape Format for DQFN

TAPE FORMAT FOR DQFN

| Package Designator | Tape Section | Number of Cavities | Cavity Status | Cover Tape Status |
|--------------------|--------------------|--------------------|---------------|-------------------|
| BQX | Leader (Start End) | 125 (Typ.) | Empty | Sealed |
| | Carrier | 3000 | Filled | Sealed |
| | Trailer (Hub End) | 75 (Typ.) | Empty | Sealed |

Tape Dimensions (Inches (Millimeters))



| PKG. SIZE | DIM.Ao | DIM.Bo | DIM.Ko |
|-----------|-----------|-----------|-----------|
| 3.5 X 4.5 | 3.8 ± 0.1 | 4.8 ± 0.1 | 0.9 ± 0.1 |
| 3.0 X 3.0 | 3.3 ± 0.1 | 3.3 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 4.5 | 2.8 ± 0.1 | 4.8 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 3.5 | 2.8 ± 0.1 | 3.8 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 3.0 | 2.8 ± 0.1 | 3.3 ± 0.1 | 0.9 ± 0.1 |
| 2.5 X 2.5 | 2.8 ± 0.1 | 2.8 ± 0.1 | 0.9 ± 0.1 |

DIMENSIONS ARE IN MILLIMETERS

NOTES: unless otherwise specified

1. Cumulative pitch for feeding holes and cavities (chip pockets) not to exceed 0.008[0.20] over 10 pitch span.
2. Smallest allowable bending radius.
3. Thru hole inside cavity is centered within cavity.
4. Tolerance is ± 0.002 [0.05] for these dimensions on all 12mm tapes.
5. Ao and Bo measured on a plane 0.120[0.30] above the bottom of the pocket.
6. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
7. Pocket position relative to sprocket hole measured as true position of pocket. Not pocket hole.
8. Controlling dimension is millimeter. Dimension in inches rounded.

Figure 7. Tape Dimensions (Inches (Millimeters))

74LCX32

Reel Dimensions (Inches (Millimeters))

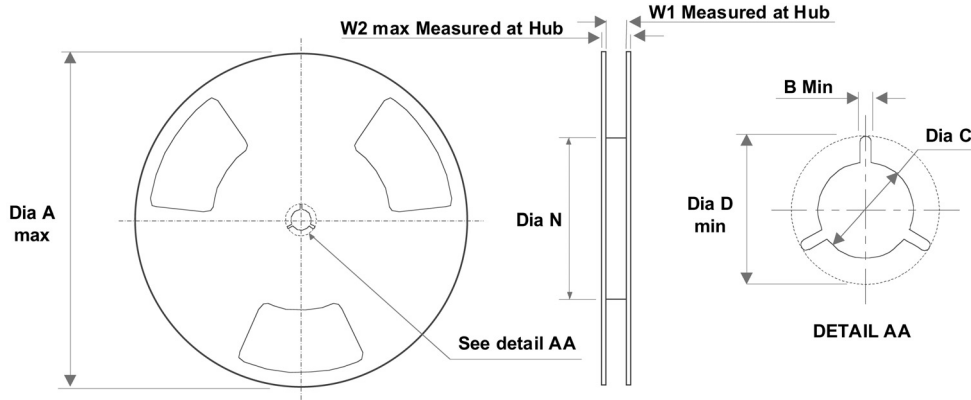


Figure 8.

| Tape Size | A | B | C | D | N | W1 | W2 |
|-----------|--------------|--------------|---------------|---------------|---------------|--------------|--------------|
| 12 mm | 13.0 (330.0) | 0.059 (1.50) | 0.512 (13.00) | 0.795 (20.20) | 2.165 (55.00) | 0.488 (12.4) | 0.724 (18.4) |

ORDERING INFORMATION

| Ordering Number | Package Number | Package Description | Shipping [†] |
|---------------------|----------------|--|--------------------------|
| 74LCX32M | SOIC14 | 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow | 1100 Units / Tube |
| 74LCX32BQX (Note 5) | QFN14 | 14-Terminal Depopulated Quad Very-Thin Flat Pack No Leads (DQFN), JEDEC MO-241, 2.5 x 3.0 mm | 3000 Units / Tape & Reel |
| 74LCX32MTC | TSSOP-14 WB | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide | 2350 Units / Tube |
| 74LCX32MTCX | TSSOP-14 WB | 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4 mm Wide | 2500 Units / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

5. DQFN package available in Tape and Reel only.

6. Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

7. All packages are lead free per JEDEC: J-STD-020B standard.

MECHANICAL CASE OUTLINE

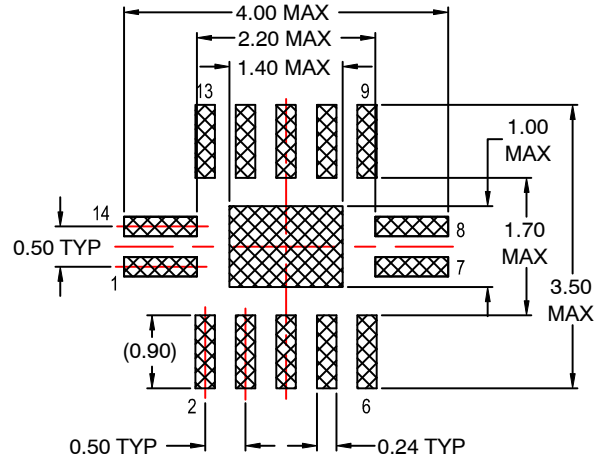
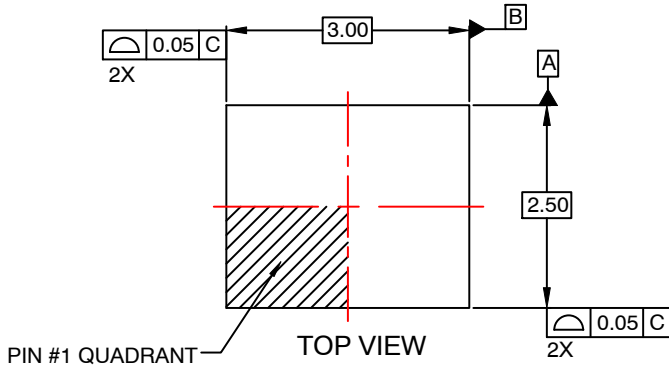
PACKAGE DIMENSIONS

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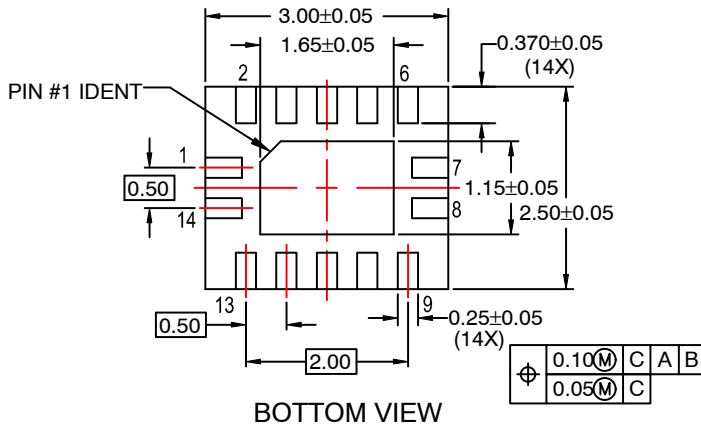
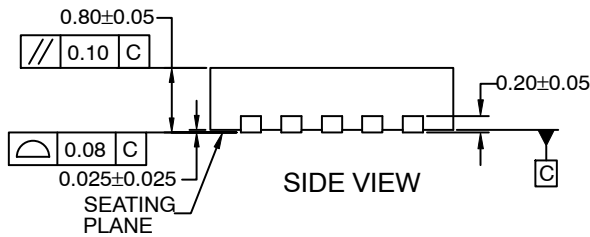


QFN14 3.0x2.5, 0.5P
CASE 510CB
ISSUE O

DATE 31 AUG 2016



RECOMMENDED LAND PATTERN



NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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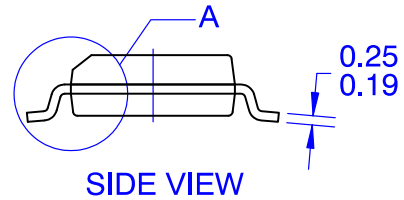
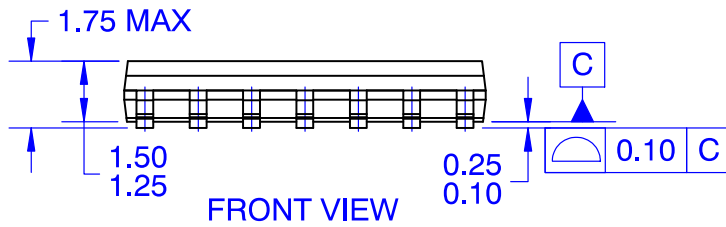
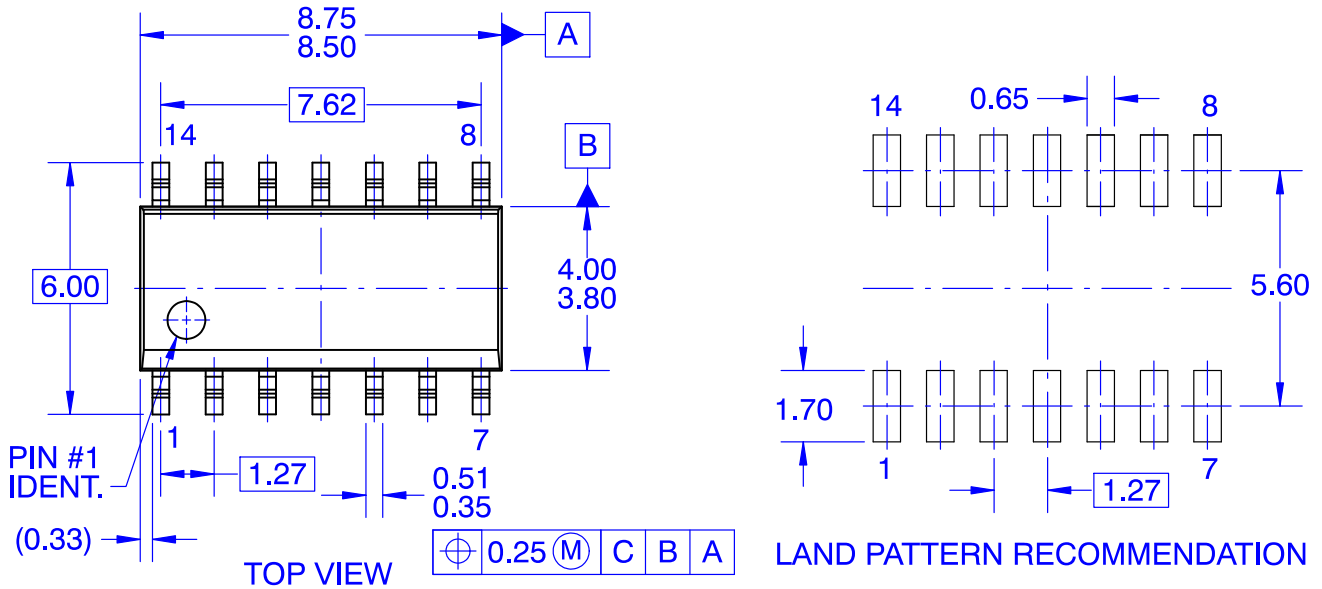
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

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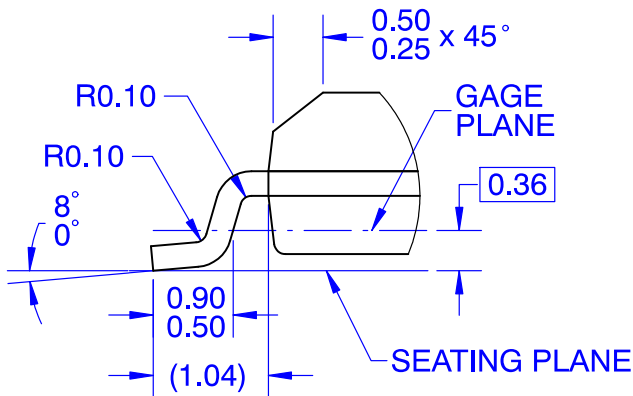
SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



NOTES:

- A. CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C
- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009



DETAIL A
SCALE 16 : 1

| | | |
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| DESCRIPTION: | SOIC14 | PAGE 1 OF 1 |

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MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



TSSOP-14 WB
CASE 948G
ISSUE C

DATE 17 FEB 2016

SCALE 2:1



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|------|-----------|-------|
| | MIN | MAX | MIN | MAX |
| A | 4.90 | 5.10 | 0.193 | 0.200 |
| B | 4.30 | 4.50 | 0.169 | 0.177 |
| C | --- | 1.20 | --- | 0.047 |
| D | 0.05 | 0.15 | 0.002 | 0.006 |
| F | 0.50 | 0.75 | 0.020 | 0.030 |
| G | 0.65 BSC | | 0.026 BSC | |
| H | 0.50 | 0.60 | 0.020 | 0.024 |
| J | 0.09 | 0.20 | 0.004 | 0.008 |
| J1 | 0.09 | 0.16 | 0.004 | 0.006 |
| K | 0.19 | 0.30 | 0.007 | 0.012 |
| K1 | 0.19 | 0.25 | 0.007 | 0.010 |
| L | 6.40 BSC | | 0.252 BSC | |
| M | 0° | 8° | 0° | 8° |

GENERIC MARKING DIAGRAM*

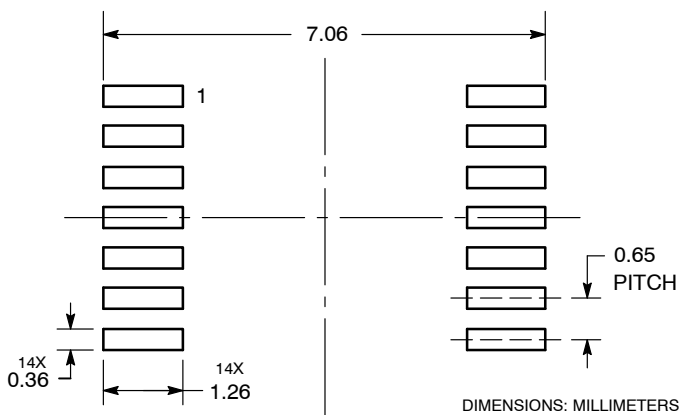


- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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