

Low-Voltage Quad 2-Input NAND Gate with 5 V Tolerant Inputs 74LCX00

General Description

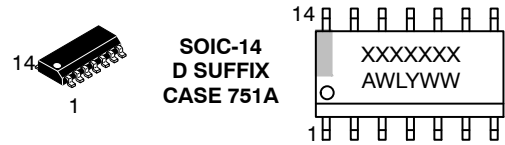
The LCX00 contains four 2-input NAND gates. The inputs tolerate voltages up to 5.5 V allowing the interface of 5 V systems to 3 V systems.

The 74LCX00 is fabricated with advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

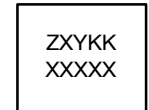
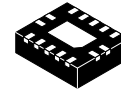
Features

- 5 V Tolerant Inputs
- 1.65 V – 5.5 V V_{CC} Specifications Provided
- 5.2 ns t_{PD} Max. ($V_{CC} = 3.3$ V), 10 μ A I_{CC} Max.
- Power Down High Impedance Inputs and Outputs
- ± 24 mA Output Drive ($V_{CC} = 3.0$ V)
- Implements Proprietary Noise/EMI Reduction Circuitry
- Latch-up Performance Exceeds JEDEC 78 Conditions
- ESD performance:
 - ◆ Human Body Model >2000 V
- Available on SOIC, TSSOP and Leadless QFN Packages
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

MARKING DIAGRAMS



XXXXXX = Specific Device Code
 A = Assembly Location
 L, WL = Wafer Lot
 Y, YY = Year
 W, WW = Work Week
 G or ■ = Pb-Free Package
 (Note: Microdot may be in either location)



QFN14 3.0x2.5, 0.5P
CASE 510CB

XXXXX = Specific Device Code
 Z = Assembly Plant Code
 XY = Date Code
 KK = Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

74LCX00

CONNECTION DIAGRAMS

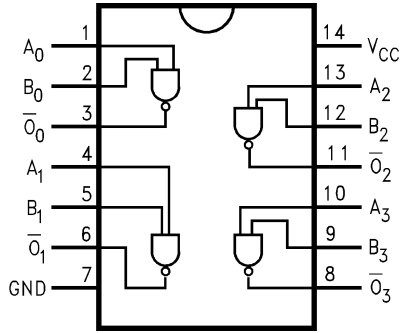


Figure 1. Pin Assignments for SOIC and TSSOP

LOGIC SYMBOL

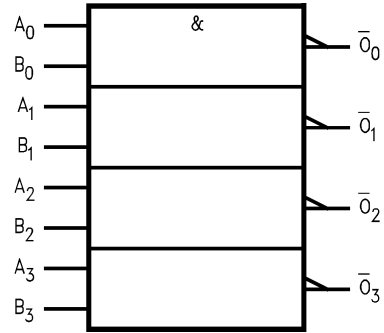
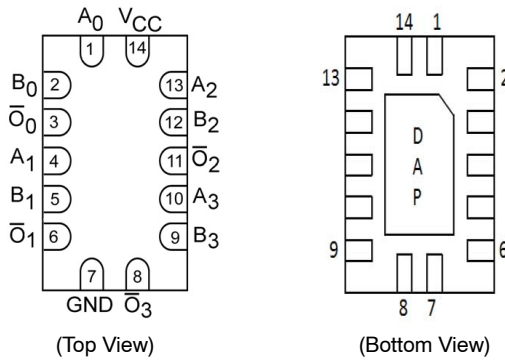


Figure 3. IEEE/IEC



(Top View)

(Bottom View)

Figure 2. Pad Assignments for DQFN

PIN DESCRIPTION

Pin Names	Description
A_n, B_n	Inputs
\bar{O}_n	Outputs
DAP	No Connect

NOTE: DAP (Die Attach Pad)

74LCX00

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +6.5	V
V _I	DC Input Voltage (Note 1)	-0.5 to +6.5	V
V _O	DC Output Voltage (Note 1)	Active-Mode (High or Low State) Tri-State Mode Power-Down Mode (V _{CC} = 0 V)	-0.5 to V _{CC} + 0.5 -0.5 to +6.5 -0.5 to +6.5
I _{IK}	DC Input Diode Current	V _I < GND	-50
I _{OK}	DC Output Diode Current	V _O < GND	-50
I _O	DC Output Source/Sink Current		±50
I _{CC} or I _{GND}	DC Supply Current per Supply Pin or Ground Pin		±100
T _{STG}	Storage Temperature Range		-65 to +150
T _L	Lead Temperature, 1 mm from Case for 10 secs		260
T _J	Junction Temperature Under Bias		+150
θ _{JA}	Thermal Resistance (Note 1)	SOIC-14 QFN14 TSSOP-14	116 130 150
P _D	Power Dissipation in Still Air at 125°C	SOIC-14 QFN14 TSSOP-14	1077 962 833
MSL	Moisture Sensitivity		Level 1
F _R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
V _{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- I_O absolute maximum rating must be observed.
- Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
- HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Typ	Max	Unit
V _{CC}	Supply Voltage				
	Operating	1.65	3.3	5.5	V
	Data Retention Only	1.5	3.3	5.5	V
V _I	Digital Input Voltage	0	-	5.5	V
V _O	Output Voltage				
	Active Mode (High or Low State)	0	-	V _{CC}	V
	Tri-State Mode	0	-	5.5	V
	Power Down Mode (V _{CC} = 0 V)	0	-	5.5	V
T _A	Operating Free-Air Temperature	-40	-	+125	°C
t _r , t _f	Input Rise or Fall Rate				
	V _{CC} = 1.65 V to 1.95 V	0	-	20	nS/V
	V _{CC} = 2.3 V to 2.7 V	0	-	20	nS/V
	V _{IN} from 0.8 V to 2.0 V, V _{CC} = 3.0 V	0	-	10	nS/V
	V _{CC} = 4.5 V to 5.5 V	0	-	5	nS/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

- Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40 °C to +85 °C		T _A = -40 °C to +125 °C		Unit
				Min	Max	Min	Max	
V _{IH}	HIGH Level Input Voltage		1.65 – 1.95	0.65 x V _{CC}	–	0.65 x V _{CC}	–	V
			2.3 – 2.7	1.7	–	1.7	–	
			3.0 – 3.6	2.0	–	2.0	–	
			4.5 – 5.5	0.70 x V _{CC}	–	0.70 x V _{CC}	–	
V _{IL}	LOW Level Input Voltage		1.65 – 1.95	–	0.35 x V _{CC}	–	0.35 x V _{CC}	V
			2.3 – 2.7	–	0.7	–	0.7	
			3.0 – 3.6	–	0.8	–	0.8	
			4.5 – 5.5	–	0.30 x V _{CC}	–	0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	V _I = V _{IH} or V _{IL} I _{OH} = -100 μA I _{OH} = -4 mA I _{OH} = -8 mA I _{OH} = -12 mA I _{OH} = -16 mA I _{OH} = -24 mA I _{OH} = -32 mA	1.65 – 5.5	V _{CC} – 0.1	–	V _{CC} – 0.1	–	V
			1.65	1.29	–	1.29	–	
			2.3	1.8	–	1.8	–	
			2.7	2.2	–	2.2	–	
			3.0	2.4	–	2.4	–	
			3.0	2.2	–	2.2	–	
			4.5	3.7	–	3.7	–	
V _{OL}	Low-Level Output Voltage	V _I = V _{IH} or V _{IL} I _{OL} = 100 μA I _{OL} = 4 mA I _{OL} = 8 mA I _{OL} = 12 mA I _{OL} = 16 mA I _{OL} = 24 mA I _{OL} = 32 mA	1.65 – 5.5	–	0.1	–	0.1	V
			1.65	–	0.24	–	0.24	
			2.3	–	0.3	–	0.3	
			2.7	–	0.4	–	0.4	
			3.0	–	0.4	–	0.4	
			3.0	–	0.55	–	0.55	
			4.5	–	0.6	–	0.6	
I _I	Input Leakage Current	V _I = 0 to 5.5 V	3.6	–	±5.0	–	±5.0	μA
I _{OFF}	Power Off Leakage Current	V _I = 5.5 V or V _O = 5.5 V	0	–	10	–	10	μA
I _{CC}	Quiescent Supply Current	V _I = 5.5 V or GND	3.6	–	10	–	10	μA
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} – 0.6 V	2.3 – 3.6	–	500	–	500	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition	V _{CC} (V)	T _A = -40 °C to +85 °C		T _A = -40 °C to +125 °C		Unit
				Min	Max	Min	Max	
t _{PLH} , t _{PHL}	Propagation Delay, Input to Output	See Figures 4 and 5	1.65 – 1.95	–	10	–	10	ns
			2.3 – 2.7	–	6.2	–	6.6	
			2.7	–	6.0	–	6.2	
			3.0 – 3.6	–	5.2	–	5.5	
			4.5 – 5.5	–	4.2	–	5.6	
t _{OSSL} , t _{OSLH}	Output to Output Skew		1.65 – 1.95	–	–	–	–	ns
			2.3 – 2.7	–	–	–	–	
			2.7	–	–	–	–	
			3.0 – 3.6	–	1.0	–	1.0	
			4.5 – 5.5	–	–	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

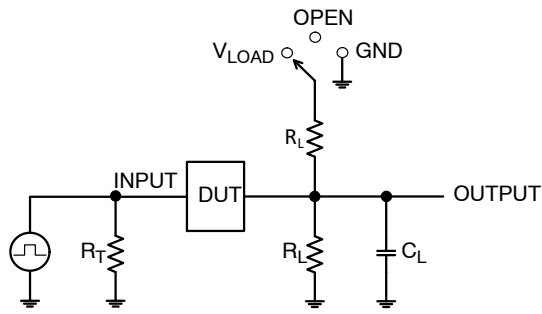
DYNAMIC SWITCHING CHARACTERISTICS

Symbol	Parameter	V _{CC} (V)	Conditions	T _A = 25 °C	Unit
				Typical	
V _{OLP}	Quiet Output Dynamic Peak V _{OL}	3.3	C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V	0.8	V
		2.5	C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V	0.6	
V _{OLV}	Quiet Output Dynamic Valley V _{OL}	3.3	C _L = 50 pF, V _{IH} = 3.3 V, V _{IL} = 0 V	-0.8	V
		2.5	C _L = 30 pF, V _{IH} = 2.5 V, V _{IL} = 0 V	-0.6	

CAPACITANCE

Symbol	Parameter	Conditions	Typical	Unit
C _{IN}	Input Capacitance	V _{CC} = Open, V _I = 0 V or V _{CC}	7	pF
C _{OUT}	Output Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC}	8	pF
C _{PD}	Power Dissipation Capacitance	V _{CC} = 3.3 V, V _I = 0 V or V _{CC} , f = 10 MHz	25	pF

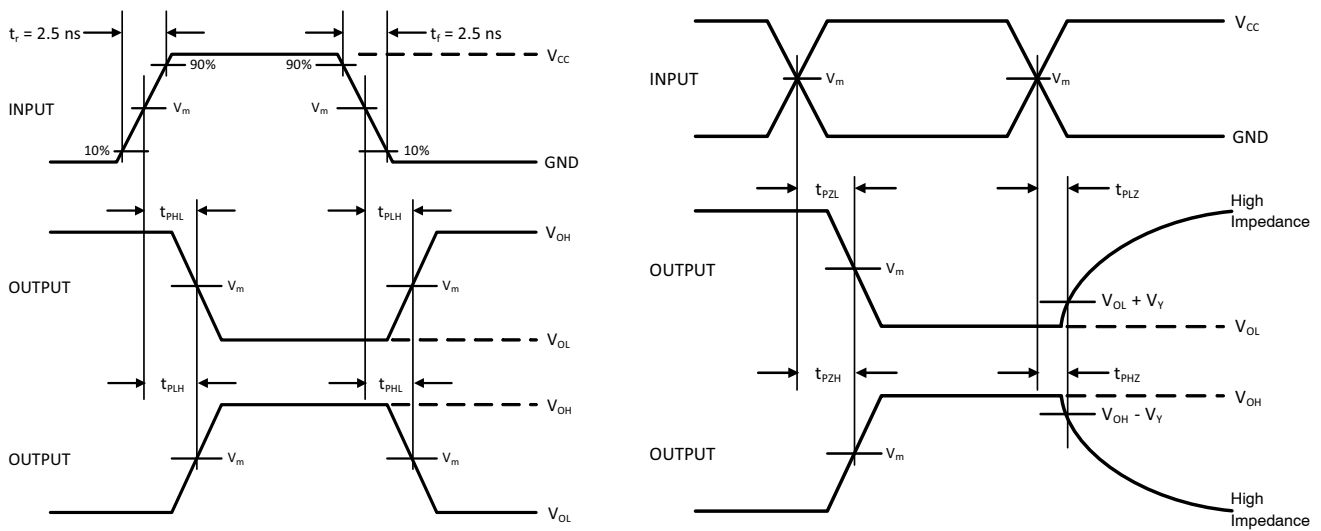
74LCX00



C_L includes probe and jig capacitance
 R_T is Z_{OUT} of pulse generator (typically 50 Ω)
 $f = 1$ Mhz, $t_W = 500$ ns

Test	Switch Position
t_{PLH} / t_{PHL}	Open
t_{PLZ} / t_{PZL}	V_{LOAD}
t_{PHZ} / t_{PZH}	GND

Figure 4. Test Circuit



V_{CC}, V	R_L, Ω	C_L, pF	V_{LOAD}	V_m, V	V_Y, V
1.65 to 1.95	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.3 to 2.7	500	30	$2 \times V_{CC}$	$V_{CC}/2$	0.15
2.7	500	50	6 V	1.5	0.3
3.0 to 3.6	500	50	6 V	1.5	0.3
4.5 to 5.5	500	50	$2 \times V_{CC}$	$V_{CC}/2$	0.3

Figure 5. Switching Waveforms

74LCX00

SCHEMATIC DIAGRAM (Generic for LCX Family)

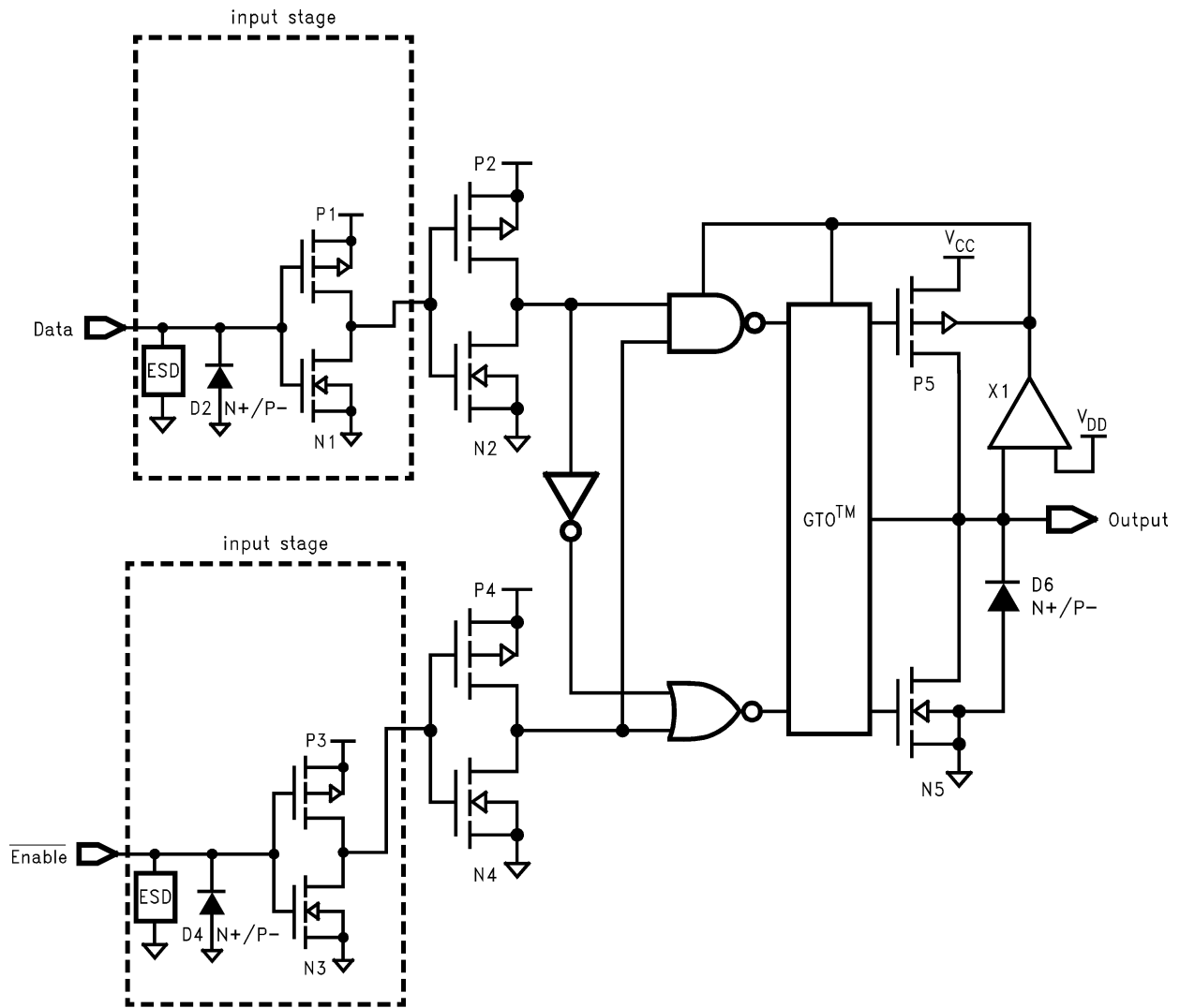


Figure 6. Schematic Diagram (Generic for LCX Family)

74LCX00

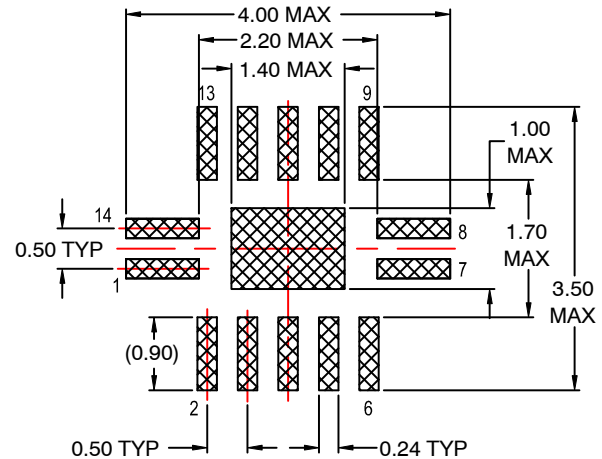
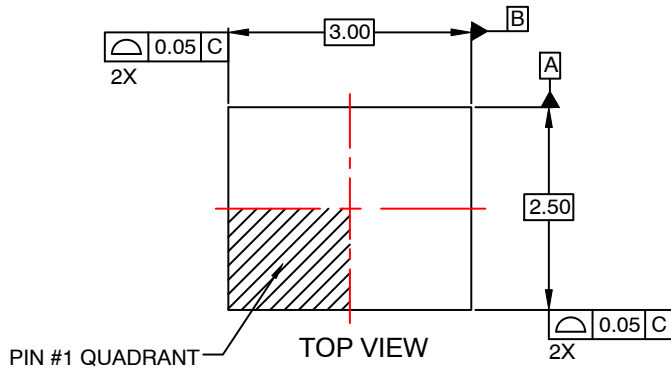
ORDERING INFORMATION

Device	Marking	Package	Shipping [†]
74LCX00MTCX	LCX 00	TSSOP-14	2500 / Tape & Reel
74LCX00BQX	LCX00	QFN-14	3000 / Tape & Reel

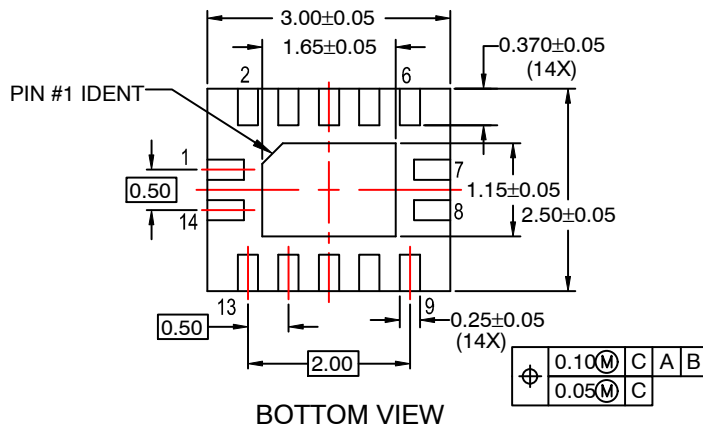
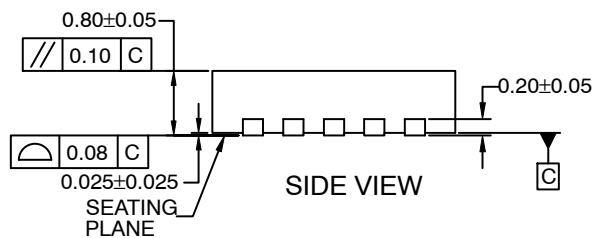
[†] For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

QFN14 3.0x2.5, 0.5P
CASE 510CB
ISSUE O

DATE 31 AUG 2016



RECOMMENDED LAND PATTERN



NOTES:

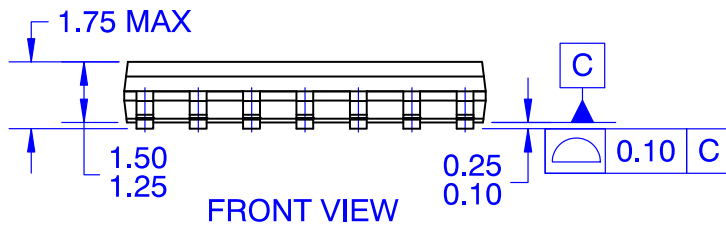
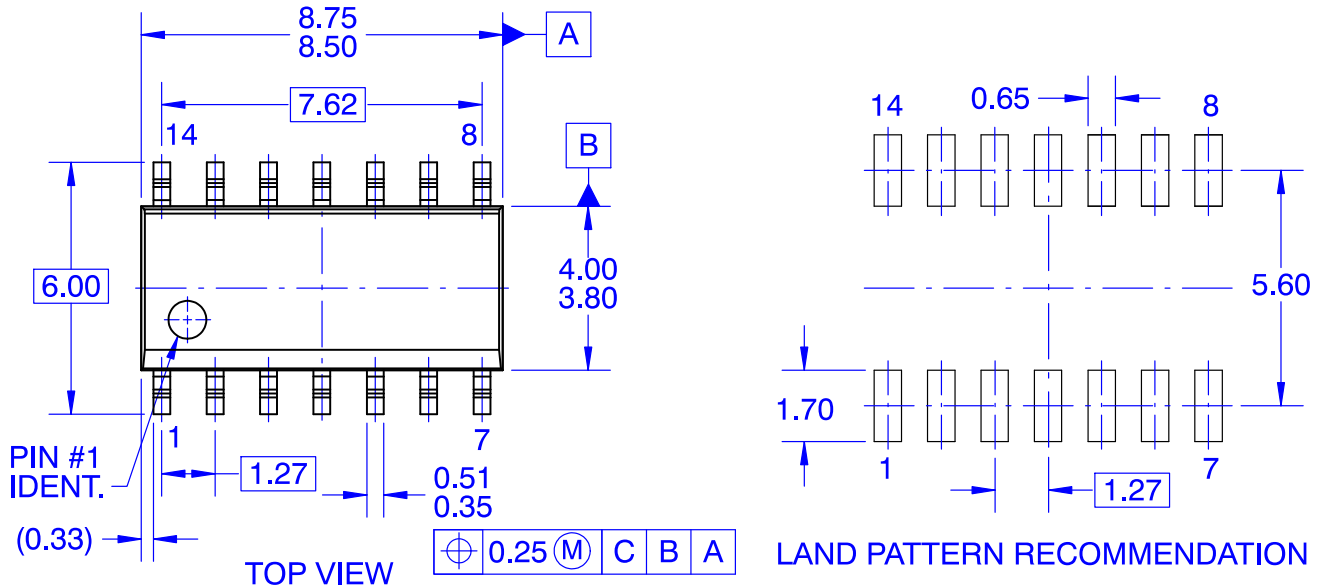
- A. CONFORMS TO JEDEC REGISTRATION MO-241, VARIATION AA
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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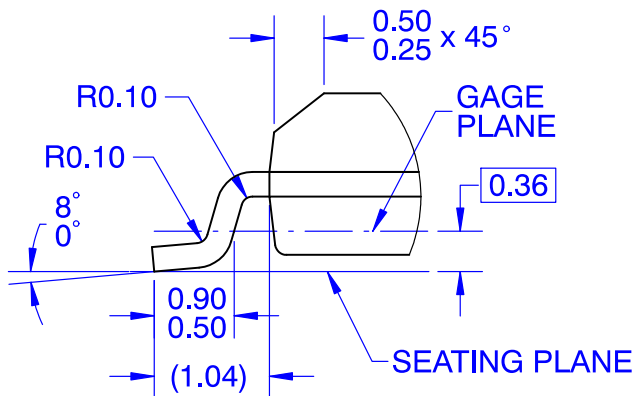
SOIC14
CASE 751EF
ISSUE O

DATE 30 SEP 2016



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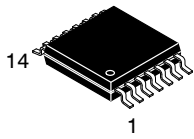
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- B. ALL DIMENSIONS ARE IN MILLIMETERS
- C. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS
- D. LAND PATTERN STANDARD: SOIC127P600X145-14M
- E. CONFORMS TO ASME Y14.5M, 2009



DETAIL A
SCALE 16 : 1

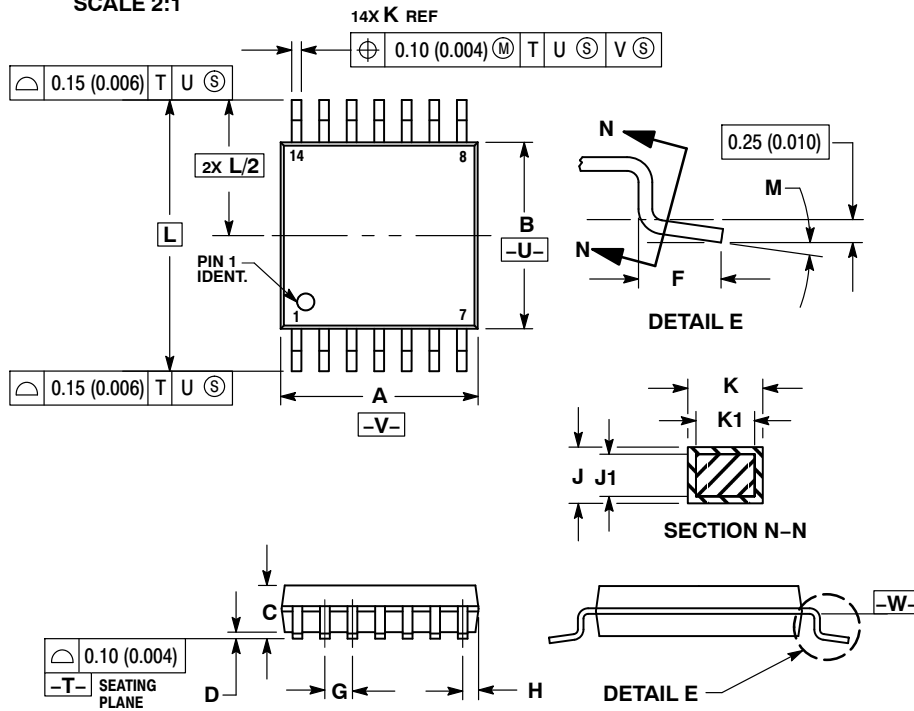
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TSSOP-14 WB
CASE 948G
ISSUE C

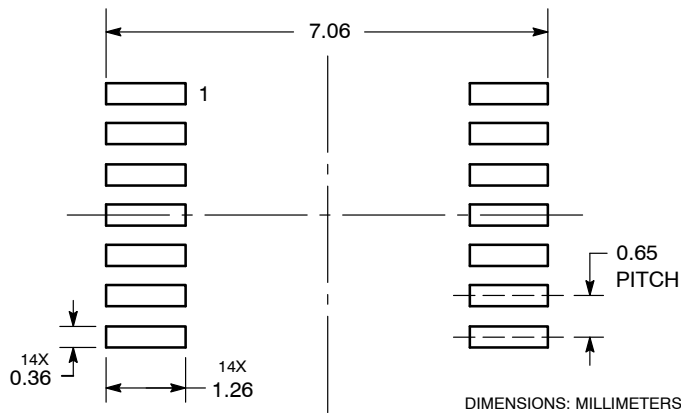
DATE 17 FEB 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
 5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
 6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

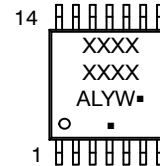
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED
SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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