

N-Channel JFET

15 V, 10 to 20 mA, 38 mS, CP

2SK2394



SC-59-3
318BJ

Features

- Large $|y_{fs}|$
- Small C_{iss}
- Small-Sized Package Permitting 2SK2394-Applied Sets to be Made Small Slim
- Ultralow Noise Figure
- This is a Pb-Free Device

Applications

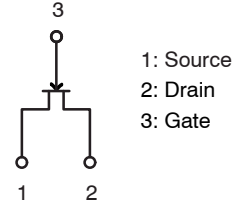
- AM Tuner RF Amplifier
- Low-Noise Amplifier

ABSOLUTE MAXIMUM RATINGS at $T_A = 25^\circ\text{C}$

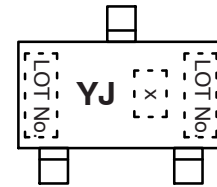
Symbol	Parameter	Value	Unit
V_{DSX}	Drain-to-Source Voltage	15	V
V_{GDS}	Gate-to-Drain Voltage	-15	V
I_G	Gate Current	10	mA
I_D	Drain Current	50	mA
P_D	Allowable Power Dissipation	200	mW
T_J	Junction Temperature	150	$^\circ\text{C}$
T_{stg}	Storage Temperature	-55 to +150	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

ELECTRICAL CONNECTION



MARKING DIAGRAM



YJx = Specific Device Code
x = 6

ORDERING INFORMATION

Device	Package	Shipping [†]
2SK2394-6-TB-E	SC-59-3 (Pb-Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

2SK2394

ELECTRICAL CHARACTERISTICS at $T_A = 25^\circ\text{C}$

Symbol	Parameter	Test Conditions	Ratings			Unit
			Min	Typ	Max	
$V_{(BR)GDS}$	Gate-to-Drain Breakdown Voltage	$I_G = -10 \mu\text{A}$, $V_{DS} = 0 \text{ V}$	-15	-	-	V
I_{GSS}	Gate Cutoff Current	$V_{GS} = -10 \text{ V}$, $V_{DS} = 0 \text{ V}$	-	-	-1.0	nA
$V_{GS(off)}$	Cutoff Voltage	$V_{DS} = 5 \text{ V}$, $I_D = 100 \mu\text{A}$	-0.3	-0.7	-1.0	V
I_{DSS}	Drain Current	$V_{DS} = 5 \text{ V}$, $V_{GS} = 0 \text{ V}$	10	-	20	mA
yfs	Forward Transfer Admittance	$V_{DS} = 5 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ kHz}$	20	38	-	mS
C_{iss}	Input Capacitance	$V_{DS} = 5 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	-	10.0	-	pF
C_{rss}	Reverse Transfer Capacitance		-	2.9	-	pF
NF	Noise Figure	$V_{DS} = 5 \text{ V}$, $R_g = 1 \text{ k}\Omega$, $I_D = 1 \text{ mA}$, $f = 1 \text{ kHz}$	-	1.0	-	dB

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TYPICAL CHARACTERISTICS

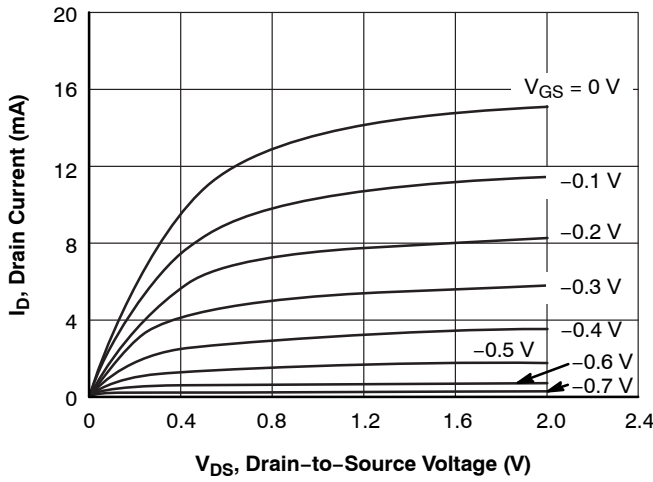


Figure 1. $I_D - V_{DS}$

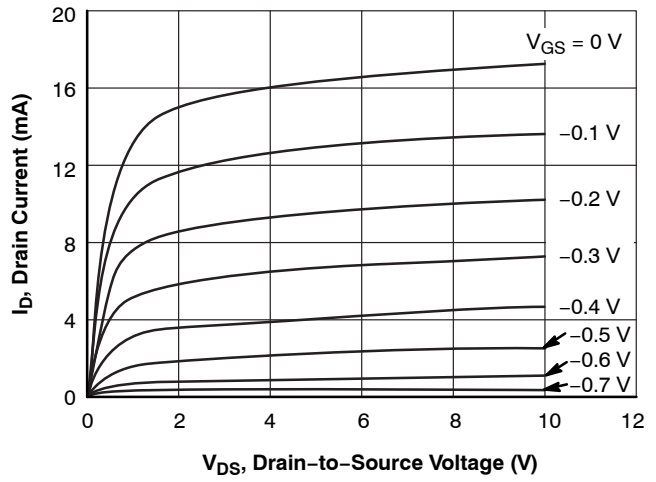


Figure 2. $I_D - V_{DS}$

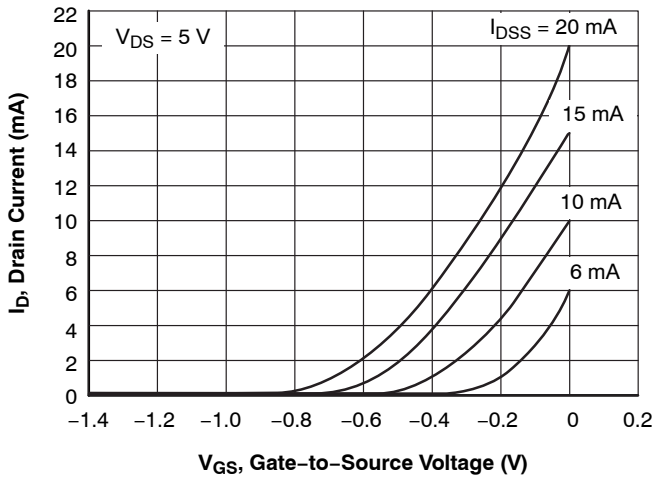


Figure 3. $I_D - V_{GS}$

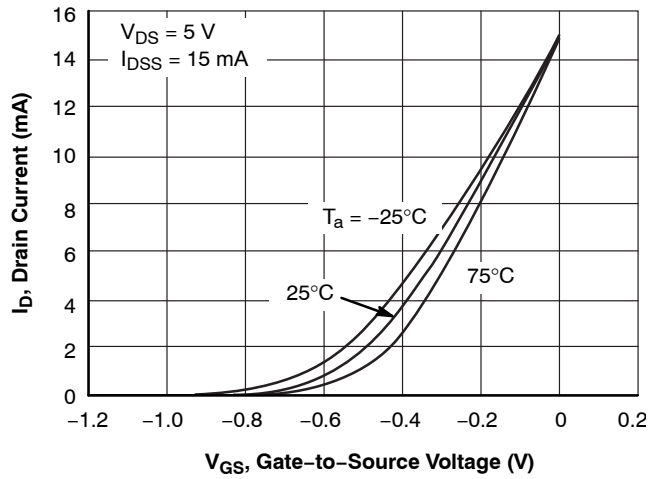


Figure 4. $I_D - V_{GS}$

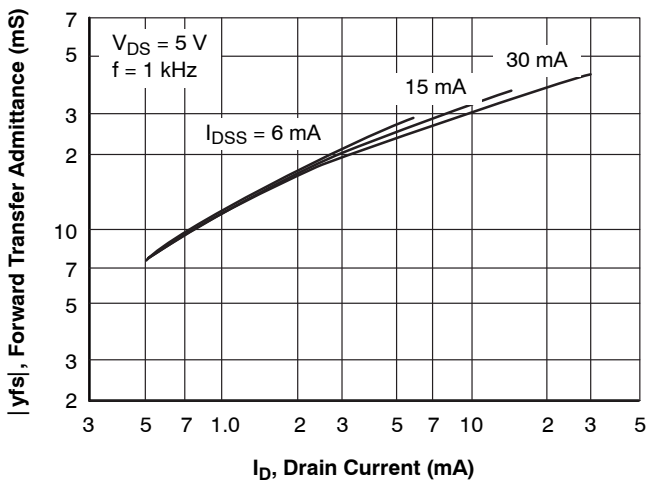


Figure 5. $|y_{fs}| - I_D$

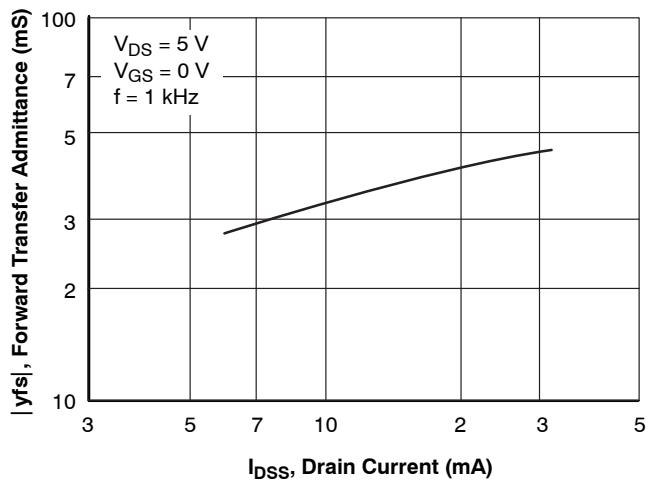


Figure 6. $|y_{fs}| - I_{DSS}$

TYPICAL CHARACTERISTICS (continued)

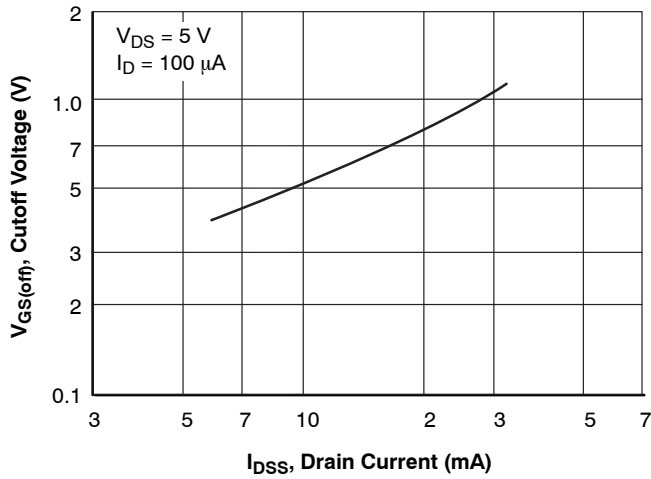


Figure 7. $V_{GS(off)} - I_{DSS}$

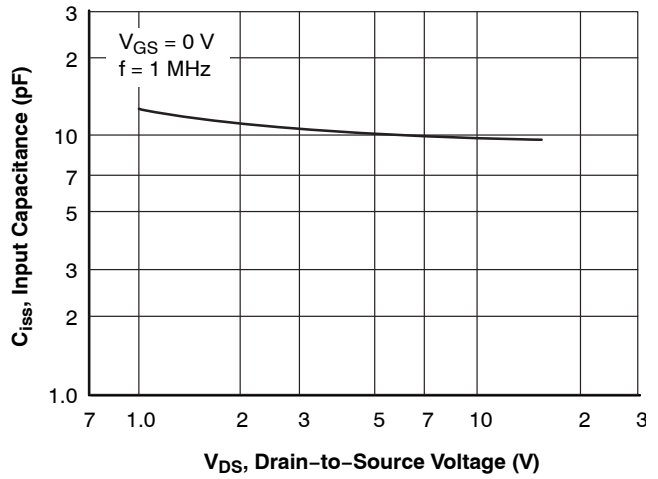


Figure 8. $C_{iss} - V_{DS}$

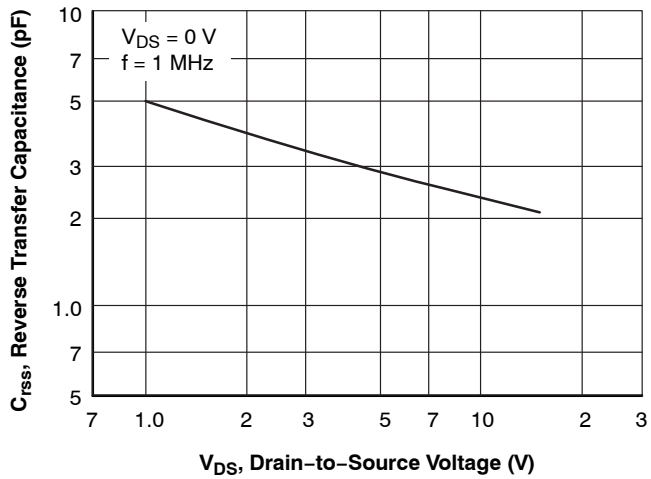


Figure 9. $C_{rss} - V_{DS}$

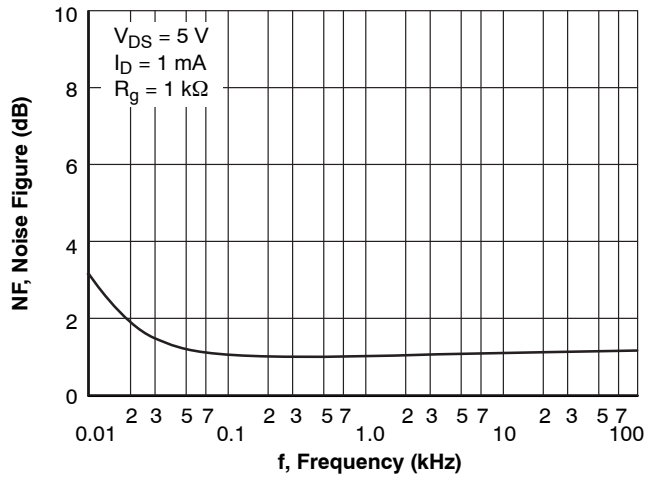


Figure 10. $NF - f$

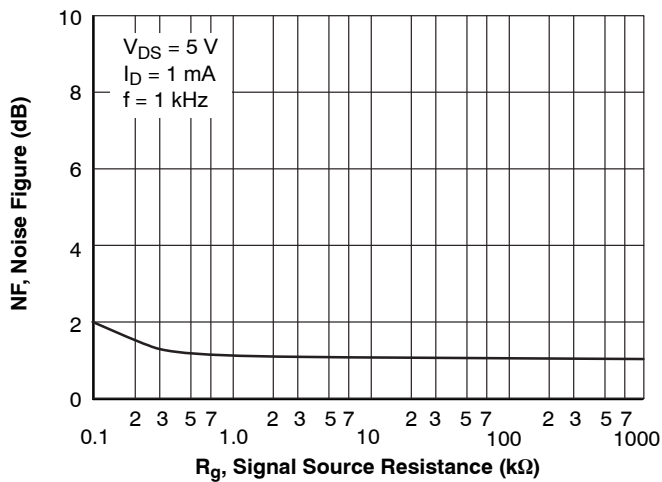


Figure 11. $NF - R_g$

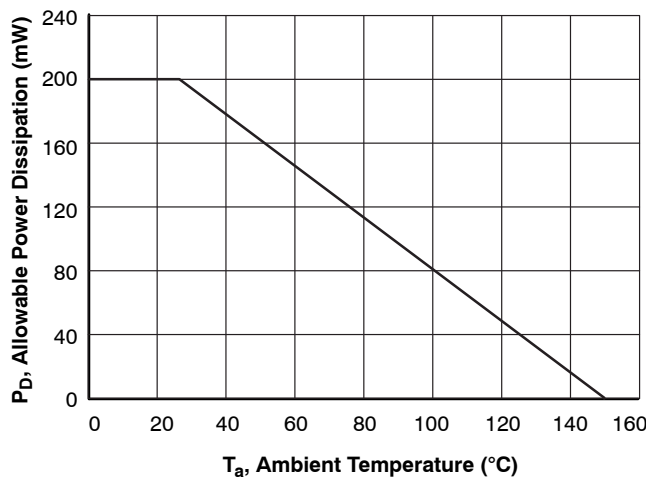


Figure 12. $P_D - T_a$

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

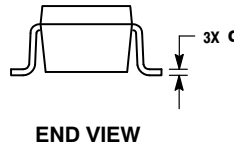
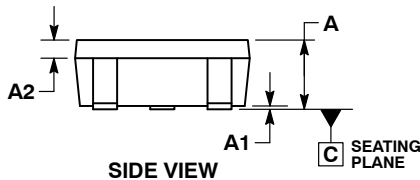
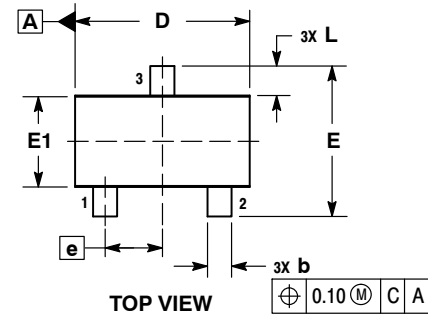
ON Semiconductor®



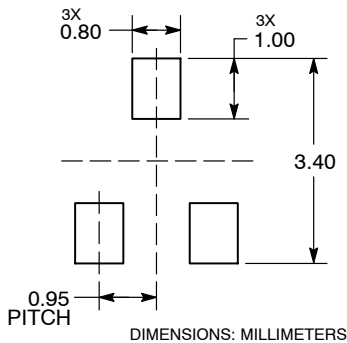
SCALE 2:1

SC-59 / CP3
CASE 318BJ
ISSUE O

DATE 09 JAN 2015



RECOMMENDED SOLDERING FOOTPRINT*

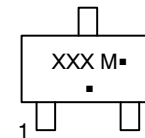


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.20 PER SIDE.
4. DIMENSIONS D AND E1 ARE MEASURED AT THE OUTERMOST EXTREME OF THE PLASTIC BODY.
5. DIMENSIONS b AND c APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 AND 0.20 FROM THE TIP.

MILLIMETERS		
DIM	MIN	MAX
A	0.95	1.35
A1	0.00	0.10
A2	0.20	0.40
b	0.35	0.50
c	0.10	0.20
D	2.75	3.05
E	2.30	2.70
E1	1.35	1.65
e	0.95 BSC	
L	0.35	0.75

GENERIC MARKING DIAGRAM



- XXX = Specific Device Code
- M = Date Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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