PCN# : P57LAA
Issue Date : Sep. 17, 2015

DESIGN/PROCESS CHANGE NOTIFICATION

This is to inform you that a change is being made to the products listed below.

Unless otherwise indicated in the details of this notification, the identified change will have no impact on product quality, reliability, electrical, visual or mechanical performance and affected products will remain fully compliant to all published specifications. Products incorporating this change may be shipped interchangeably with existing unchanged products.

This change is planned to take effect in 90 calendar days from the date of this notification. Please work with your local Fairchild Sales Representative to manage your inventory of unchanged product if your evaluation of this change will require more than 90 calendar days.

Please contact your local Customer Quality Engineer within 30 days of receipt of this notification if you require any additional data or samples.

Implementation of change:

Expected First Shipment Date for Changed Product : Dec. 16, 2015

Expected First Date Code of Changed Product :1551

Description of Change (From) :
Front-end Wafer Fabrication site Fairchild Salt Lake Utah, 6-inch wafers

Description of Change (To) :
Front-end Wafer Fabrication site Tower Jazz Israel Foundry, 8-inch wafers and Fairchild Mt. Top, PA 8-inch wafers

Reason for Change:
Improve supply flexibility.
Better quality and yields through equipment and facility upgrades.
- Increased automation in handling and inspection in assembly.
Fairchild partners with foundries and assembly subcontractors.
- Best manufacturing practices, access to many customers methods and practices.
- Advanced technology for fast ramp of future new products and technologies.

Affected Product(s): Please refer to the list of affected products in the addendum attached in the PCN email you received. This list is based on an analysis of your companys procurement history.

Qualification Plan	Device	Package	Process	No. of Lots
Q20150336	FDD6688	D-PAK	PT3 N	3

Test Description:	Condition:	Standard :	Duration:	Results:
Precon	MSL1, 260C	JESD22A-113	NA	Nov 20
Temperature Cycle With Precon	-65C, 150C	JESD22-A104	500 cyc	Dec 06
High Temperature Storage Life With Precon	175C	JESD22-A103	1000 hrs	Jan 10 2016
Power Cycle With Precon	Delta 100C, 2 Min On/Off	JESD22-A122	15000 cyc	Jan 10 2016
Highly Accelerated Stress Test With Precon	130C, 85%RH, 24V	JESD22-A110	96 hrs	Dec 01
High Temperature Gate Bias	175C, 20V	JESD22-A108	1000 hrs	Jan 15 2016
High Temperature Reverse Bias	175C, 24V	JESD22-A108	1000 hrs	Jan 15 2016
RSDH	270C	JESD22-B106	15 sec	Nov 20

Qualification Plan	Device	Package	Process	No. of Lots
Q20150336	FDD6635	D-PAK	PT3 N	3

Test Description:	Condition:	Standard :	Duration:	Results:
Precon	MSL1, 260C	JESD22A-113	NA	Nov 20
Temperature Cycle With Precon	-65C, 150C	JESD22-A104	500 cyc	Dec 06
High Temperature Storage Life With Precon	150C	JESD22-A103	1000 hrs	Jan 10 2016
Power Cycle With Precon	Delta 100C, 2 Min On/Off	JESD22-A122	15000 cyc	Jan 10 2016
Highly Accelerated Stress Test With Precon	130C, 85%RH, 28V	JESD22-A110	96 hrs	Dec 01
High Temperature Gate Bias	150C, 20V	JESD22-A108	1000 hrs	Jan 15 2016
High Temperature Reverse Bias	150C, 28V	JESD22-A108	1000 hrs	Jan 15 2016
RSDH	270C	JESD22-B106	15 sec	Nov 20

Qualification Plan	Device	Package	Process	No. of Lots
Q20140189	FDD4141_F085	TO252	RP3 P	3

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	260°C, 3 cycles	JESD22-A113	NA	Oct 15
Highly Accelerated Stress Test	130°C, 85%RH, Vr = -32V	JESD22-A110	96 hrs	Oct 29
High Temperature Gate Bias	175°C, Vgs = -20V	JESD22-A108	1000 hrs	Nov 23
High Temperature Reverse Bias	175°C, Vr = -40V	JESD22-A108	1000 hrs	Nov 23
High Temperature Storage Life	175°C	JESD22-A103	1000 hrs	Dec 7
Power Cycle	Delta 100CC, 2 Min cycle	JESD22-A105	15000 cyc	Dec10
Temperature Cycle	-55°C, 150°C	JESD22-A104	1000 cyc	Oct 26
Unbiased Highly Accelerated Stress Test	130°C, 85%RH	JESD22-A118	96 hrs	Oct 22
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	Oct 5

Qualification Plan	Device	Package	Process	No. of Lots
Q20150099	FDFM2P110	MLP	PT2 P, Schottky	3

Test Description:	Condition:	Standard:	Duration:	Results:
Preconditioning, MSL 1	Peak Temp(260°C), 3 Cycles	JESD22-A113	NA	Nov 20
Highly Accelerated Stress Test	85%RH, 130C, -16V	JESD22-A110	96 hrs	Dec 01
High Temperature Reverse Bias	150C, -16V	JESD22-A108	1000 hrs	Jan 15 2016
High Temperature Reverse Bias	125C, -16V	JESD22-A108	1000 hrs	Jan 15 2016
High Temperature Gate Bias	150C, -12V	JESD22-A108	1000 hrs	Jan 15 2016
Temperature Cycle	-65C, 150C	JESD22-A104	500 cyc	Dec 06
High Temperature Storage Life	150C	JESD22- A103	1000 hrs	Jan 10 2016
Power Cycle	Delta125CC,2 Mincycle	MILSTD-750-1036	7500 cyc	Jan 10 2016
Destructive Physical Analysis	NA	AEC-Q101-004 Section 4	NA	Jan 15 2016

Qualification Plan	Device	Package	Process	No. of Lots
Q20140219	FDS4675	SOIC 8L	PT2 P	1

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	260C, 3 cycles	JESD22-A113	NA	0/308
MSL1	260C, 3 cycles	J-STD_020	NA	0/22
Highly Accelerated Stress Test	130C, 85%RH, -32V	JESD22-A110	96 hrs	0/77
High Temperature Storage Life Test	150C	JESD22-A103	500 hrs	0/77
UnBiased Highly Accelerated Stress Test	130C, 85%RH	JESD22-A118	96 hrs	0/77
Temperature Cycle	-65C, 150C	JESD22-A104	1000 cyc	0/77
High Temperature Gate Bias	150C, -20V	JESD22-A108	1000 hrs	0/77
High Temperature Reverse Bias	150C, -40V	JESD22-A108	1000 hrs	0/77
Power Cycle	Delta 100CC, 2 Min cycle	MIL-STD-750-1036	15000 cyc	0/77
Lead Fatigue	15Degree, 3X	JESD22-B105		0/30
Resistance to Solder Heat	Solder Dip = 260C	JESD22-B106	10 sec	0/10
Solderability	Condition C steam aging (8hrs), Condition A solder Dip (245 for 5 sec)	JESD22-B102	NA	0/10

Qualification Plan	Device	Package	Process	No. of Lots
Q20140219	SI4467DY	SOIC 8L	PT2 P	2

Test Description:	Condition:	Standard:	Duration:	Results:
MSL3 Precondition	260C, 3 cycles	JESD22-A113	NA	0/616
MSL3	260C, 3 cycles	J-STD_020	NA	0/44
Highly Accelerated Stress Test	130C, 85%RH, -16V	JESD22-A110	96 hrs	0/154
High Temperature Storage Life Test	150C	JESD22-A103	500 hrs	0/154
UnBiased Highly Accelerated Stress Test	130C, 85%RH	JESD22-A118	96 hrs	0/154
Temperature Cycle	-65C, 150C	JESD22-A104	1000 cyc	0/154
High Temperature Gate Bias	150C, -8V	JESD22-A108	1000 hrs	0/154
High Temperature Reverse Bias	150C, -20V	JESD22-A108	1000 hrs	0/154
Power Cycle	Delta 100CC, 2 Min cycle	MIL-STD-750-1036	15000 cyc	0/154
Lead Fatigue	15Degree, 3X	JESD22-B105		0/60
Resistance to Solder Heat	Solder Dip = 260C	JESD22-B106	10 sec	0/20
Solderability	Condition C steam aging (8hrs), Condition A solder Dip (245 for 5 sec)	JESD22-B102	NA	0/20

Qualification Plan	Device	Package	Process	No. of Lots
Q20140001	FDMC6676BZ	MLDEUC08	ST3 PZ	3

Test Description:	Condition	Standard	Duration	Results:
High Temperature Gate Bias	150C, Vgs=20V	JESD22-A108	1000 hrs	0/237
High Temperature Reverse Bias	150C, Vr=80V	JESD22-A108	1000 hrs	0/237
High Temperature Storage Life	175C	JESD22-A103	500 hrs	0/237
Highly Accelerated Stress Test	130C, 85%RH, Vr=42V	JESD22-A110	96 hrs	0/237
MSLNL1A	PeakTemp(260°C), Cycles 3X	J-STD_020		0/66
Power Cycle	Delta 100C, 2 Min cycle	MIL-STD-750-1036	10000 cyc	0/237
Temperature Cycle	-65C,150C	JESD22-A104	500 cyc	0/237

Qualification Plan	Device	Package	Process	No. of Lots
Q20140208A	FDMC6683	MLDEUC08	ST3 P	1

Test Description:	Condition:	Standard :	Duration:	Results:
Auto Clave	100%RH, 121C	JESD22-A102	96 hrs	0/77
Highly Accelerated Stress Test	85%RH, 130C, -16V	JESD22-A110	96 hrs	0/77
High Temperature Gate Bias	150C, -8V	JESD22-A108	1000 hrs	0/77
High Temperature Reverse Bias	150C, -16V	JESD22-A108	1000 hrs	0/77
High Temperature Storage Life	150C	JESD22-A103	1000 hrs	0/77
Power Cycle	Delta 100C, 2 Min cycle	MIL-STD-750-1036	10000 cyc	0/77
Temperature Cycle	-65C, 150C	JESD22-A104	500 cyc	0/77
Resistance to Solder Heat	260°C	JESD22-B106	3X @ 10s	0/10
Solderability, Condition A	215°C, 5 sec	JESD22-B102	8 hrs	0/11
Solderability, Condition B	245°C, 5 sec	JESD22-B102	8 hrs	0/11
MSLNL1A	PeakTemp(260°C), Cycles 3X	J-STD_020		0/22

Qualification Plan	Device	Package	Process	No. of Lots
Q20140105A	NDB6030PL	TO263	5.0 M Cells Pch	2

Test Description:	Condition:	Standard:	Duration:	Results:
MSL1 Precondition	245°C, 3 cycles	JESD22-A113	NA	0/154
Highly Accelerated Stress Test	130°C, 85%RH, Vr = -24V	JESD22-A110	96 hrs	0/154
High Temperature Gate Bias	175°C, Vgs = -16V	JESD22-A108	1000 hrs	0/154
High Temperature Reverse Bias	175°C, Vr = -24V	JESD22-A108	1000 hrs	0/154
High Temperature Storage Life	175°C	JESD22-A103	1000 hrs	0/154
Power Cycle	Delta 100CC, 3.5 Min cycle	JESD22-A105	8572 cyc	0/154
Temperature Cycle	-65°C, 150°C	JESD22-A104	500 cyc	0/154
Resistance to Solder Heat	260°C	JESD22-B106	10 sec	0/60

Qualification Plan	Device	Package	Process	No. of Lots
Q20140105A	NDP7060	TO220	3.8M Cells Nch	3

Test Description:	Condition:	Standard :	Duration:	Results:
Temperature Cycle	-65C, 150C	JESD22-A104	500 cyc	0/231
High Temperature Storage Life	175C	JESD22-A103	1000 hrs	0/231
Power Cycle	Delta 100C, 3.5 Min On/Off	JESD22-A122	8572 cyc	0/231
Highly Accelerated Stress Test	130C, 85%RH, 42V	JESD22-A110	96 hrs	0/231
High Temperature Gate Bias	175C, 20V	JESD22-A108	1000 hrs	0/231
High Temperature Reverse Bias	175C, 48V	JESD22-A108	1000 hrs	0/231
Resistance to Solder Heat	270C	JESD22-B106	15 sec	0/90

Qualification Plan	Device	Package	Process	No. of Lots
Q20140414	FDD8453LZ_F085	D-PAK	PT4 NZ	3

Test Description:	Condition:	Standard :	Duration:	Results:
Precon	MSL1, 260C	JESD22A-113	NA	0/1155
Temperature Cycle With Precon	-55C, 150C	JESD22-A104	1000 cyc	0/231
High Temperature Storage Life With Precon	175C	JESD22-A103	1000 hrs	0/231
Power Cycle With Precon	Delta 100C, 2 Min On/Off	JESD22-A122	15000 cyc	0/231
Highly Accelerated Stress Test With Precon	130C, 85%RH, 32V	JESD22-A110	96 hrs	0/231
Un-bias HAST With Precon	130C, 85%RH,	JESD22-A118	96 hrs	0/231
High Temperature Gate Bias	175C, 20V	JESD22-A108	1000 hrs	0/231
High Temperature Reverse Bias	175C, 40V	JESD22-A108	1000 hrs	0/231
RSDH With Precon	270C	JESD22-B106	15 sec	0/90