ON Semiconductor®

Product Bulletin

Document #:PB23323X
Issue Date:07 May 2020

Title of Change:	AR0238 Register Reference Update
Effective date:	07 May 2020
Contact information:	Contact your local ON Semiconductor Sales Office or Sonya.Yip@onsemi.com
Type of notification:	This Product Bulletin is for notification purposes only. ON Semiconductor will proceed with implementation of this change upon publication of this Product Bulletin.
Change Category:	Documentation Change
Change Sub-Category(s):	Datasheet/Product Doc change

Sites Affected:

ON Semiconductor Sites	**External Foundry/Subcon Sites**
None	None

Description and Purpose:

The AR0238CS Register Reference has been updated with new information. These changes do not affect form, fit, or function of the product.

AR0238CS Register Reference Changes

1. Updated Introduction section with information about register attributes

Old Introduction Section:

Bad Frames

A bad frame is a frame where all rows do not have the same integration time or where offsets to the pixel values have changed during the frame. Many changes to the sensor register settings can cause a bad frame. For example, when line_length_pck (R0x0342–3) is changed, the new register value does not affect sensor behavior until the next frame start. However, the frame that would be read out at that frame start will have been integrated using the old row width, so reading it out using the new row width would result in a frame with an incorrect integration time.

Register Map

The tables in this section show which locations are used within the 16–bit address space. Locations that are not shown in the table are reserved for future use; to maintain compatibility with future designs they should not be read from or written to. Locations that are shown as "Reserved" should not be accessed. The default read values of registers are subject to change.

By default, bad frames are not masked. In the register tables, the "Bad Frame" column shows where changing a register or register field will cause a bad frame. This notation is used:

- *N*—No. Changing the register value will not produce a bad frame.
- *Y*—Yes. Changing the register value might produce a bad frame.
- *YM*—Yes; but the bad frame will be masked out when mask_corrupted_frames (R0x0105) is set to "1."

CAUTION: The effect of writing to reserved registers is undefined and may include the possibility of causing permanent electrical damage to the sensor.

Table 1 below lists registers and their default values. Register addresses are shown as 16– bit values in both decimal and hexadecimal. Table 2 lists registers and their descriptions.

New Introduction Section:

Buffering

In register tables, buffering shows the timing with which a newly–written register value takes effect. The notation used is:

Embedded

In register tables, the embedded column notes whether or not the register is present in the per_frame embedded data.

The notation used is:

Blank – By default, a register is not present in the embedded data

E – The register is present in the embedded data.

Locked

In register tables, locked notes whether writes to the register are protected by R0x3010. The notation used is

Blank – By default, writes to a register are not protected by R0x3010

L – Writes to the register are protected by R0x3010

2. Replaced Frame Syn'd and Bad Frame columns with new attribute columns for all registers in the Register Reference

Old Register Description Column Example:

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12288 R0x3000	15:0	0x0356	CHIP_VERSION_REG (R/W)	N	N
	Model ID. Read-only. Can be made read/write by clearing R0x301A–B[3].				
R12290 R0x3002	15:0	0x0004	Y_ADDR_START (R/W)	Y	YM
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.				

New Register Description Column Example:

Register Hex	Bits	Default	Name	Attributes			
R0x3000	15:0	0x0256	CHIP_VERSION_REG (R/W)				
	Model ID. Read–only. Can be made read/write by clearing R0x301A–B[3].						
R0x3002	15:0	0x0000	Y_ADDR_START (R/W)	S	YM		
	The first row of visible pixels to be read out (not counting any dark rows that may be read). To move the image window, set this register to the starting Y value.						

3. Updated R0x3060 Register Description

Old Register Description:

R12384 R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	Y	N
	15	X	Reserved		
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	Y	N
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	Y	N
	7	X	Reserved		
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	Y	N
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	Y	N
	Defines analog gains for both contexts $analog\_gain = 2^{coarse\_gain} \cdot \left(\frac{32}{32 - fine\_gain}\right)$				

New Register Description:

Register Hex	Bits	Default	Name	Attributes			
R0x3060	15:0	0x0000	ANALOG_GAIN (R/W)	S			
	15	X	Reserved				
	14:12	0x0000	COARSE_GAIN_CB Coarse Analog gain in context B. Gain is 2 power of the register value.	S			
	11:8	0x0000	FINE_GAIN_CB Fine analog gain in context B	S			
	7	X	Reserved				
	6:4	0x0000	COARSE_GAIN Coarse Analog gain in context A. Gain is 2 power of the register value.	S			
	3:0	0x0000	FINE_GAIN Fine analog gain in context A.	S			
	Defines analog gains for both contexts						

4. Added register R0x30FE

New Register Description:

R0x30FE	15:0	0x0080	NOISE_PEDESTAL (R/W)				
	Pedestal added prior to memory operations. Noise pedestal and AdaCD pedestals should be set to the same value.						

5. Updated R0x31E0 Register Description

Old Register Description:

Register Dec(Hex)	Bits	Default	Name	Frame Sync'd	Bad Frame
R12768 R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)	N	N
	15	0x0000	Reserved		
	14	0x0000	Reserved		
	13	X	Reserved		
	12	0x0000	Reserved		
	11	0x0000	Reserved		
	10	0x0000	Reserved		
	9	0x0000	Reserved		
	8	0x0000	Reserved		
	7:2	X	Reserved		
	1	0x0000	Reserved		
	0	0x0000	ENABLE Enable pixel defect correction.	N	N

New Register Description:

Register Hex	Bits	Default	Name	Attributes			
R0x31E0	15:0	0x0000	PIX_DEF_ID (R/W)				
	15	0x0000	Reserved				
	14	0x0000	Reserved				
	13	X	Reserved				
	12	0x0000	Reserved				
	11	0x0000	Reserved				
	10	0x0000	Reserved				
	9	0x0000	Reserved				
	8	0x0000	Reserved				
	7:2	X	Reserved				
	1	0x0000	CORRECTION_MODE Mode of pixel defect correction. 0: Tags bad pixels with the reserved value 0. 1: Corrects bad pixels using the traditional 1D correction scheme.		Y		
	0	0x0000	ENABLE Enable pixel defect correction.		Y		

List of Affected Standard Parts:

***Note**: Only the standard (off the shelf) part numbers are listed in the parts list. Any custom parts affected by this PCN are shown in the customer specific PCN addendum in the PCN email notification, or on the **PCN Customized Portal**.*

AR0238CSSC12SHRA0-DR1	AR0238CSSC12SHRA0-DP1	AR0238CSSC12SHRA0-DR
AR0238CSSC12SPRA0-DR	AR0238CSSC12SPRA0-DR1	AR0238CSSC12SHRA0-DP
AR0238CSSC12SUD20	AR0238IRSH12SUD20	