FUSB15101 Single Port USB Type-C/PD Controller One-Time Programming Guide

UM70086/D

Introduction

The FUSB15101 Evaluation Board (EVB) together with the firmware binary provided in the release package permits a customer to program the one−time programmable (OTP) non−volatile memory (NVM) of the FUSB15101.

Required Hardware and Setup Instructions

A. FUSB15101 Evaluation Board (EVB)
B. 32 kB OTP Chip labeled FUSB15101 MIN
C. SEGGER J−Link Pro JTAG/SWD programming and debug probe
D. 9−Pin Cortex−M Adapter to connect (A) the EVB to (C) J−Link Pro
E. External Power Supply

- Use (D) the 9−Pin Adapter to connect (C) the J−Link Pro to the SWD connector (J2) on the socket EVB
- Place the OTP chip in socket
- Connect (E) the Power Supply GND to the SGND pin of (A) the EVB
- Setup (E) the Power Supply to 8.4 V (~200 mA) and connect to VIN pin (Con1) of (A) the EVB

Required Software

A. SEGGER J−Link Tools
Please download and install the SEGGER J−Link utility
Note: We recommend using version 7.92d. Please make sure SEGGER J−Flash is installed.

B. Serial Wire Debug (SWD) Converter Tool
Please download and install the FUSB15101 SWD Converter tool
Note: Search for keyword FUSB15101 SWD Converter Tool.
If a new J−Link version is installed, please be aware that the windows environment path needs to point to the new installation folder for SWD to function properly.

C. FUSB15101 OTP Loader
Please download the FUSB15101 OTP Loader used by J−Link to flash the EVB.
Search for file FUSB15101_OTP_LOADER.ELF
Further instructions on where to place this file will be indicated in the subsequent paragraph.

D. FUSB15101 Device List AddOn
Please download the FUSB15101 Device AddOn to add the FUSB15101 to the device list xml.
Search for file FUSB15101_XML_ADDON.TXT

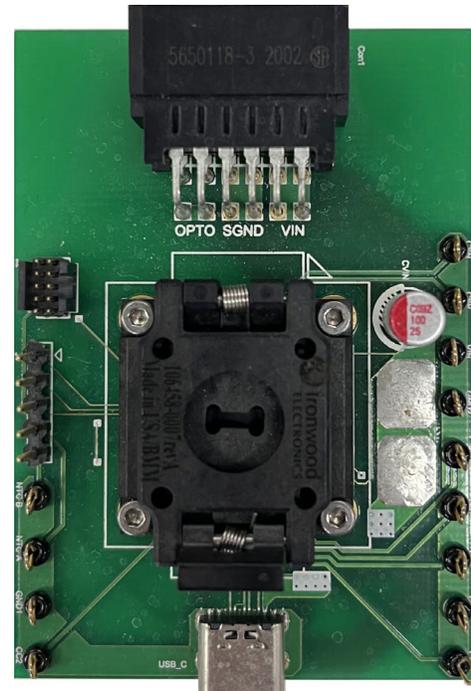**Figure 1. FUSB15101 Socket**

Adding FUSB15101 Support to J−Link

There is a need to add the FUSB15101 to the list of J−Link supported devices.

J−Link requires a device to be added in xml format as follow:

- Create a directory named onsemi\FUSB15101 as follow:
  C:\Users\<USER_NAME>\AppData\Roaming\SEGGER\JLinkDevices\onsemi\FUSB15101\

- Rename the file (E) FUSB15101_XML_ADDON.TXT to Devices.xml and place it in the following directory:
  C:\Users\<USER_NAME>\AppData\Roaming\SEGGER\JLinkDevices\onsemi\FUSB15101\

- Copy the file (C) from section "Required Software" into
  C:\Users\<USER_NAME>\AppData\Roaming\SEGGER\JLinkDevices\onsemi\FUSB15101\

Programming the OTP

Complete the following 4 steps:
- a. Connect J−Link to the EVB
- b. Validate OTP chip is blank
- c. Convert the FW Image with the SWD Converter tool
- d. Validate OTP Content

a) Connect J−Link to the EVB

- Open the SEGGER J−Flash and select "Create new project" then "Start J−Flash"
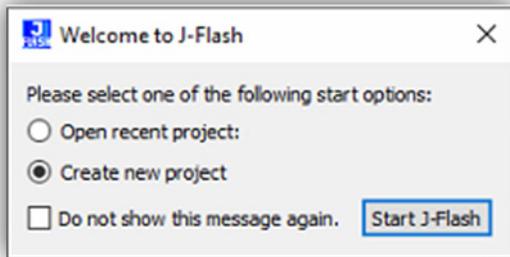
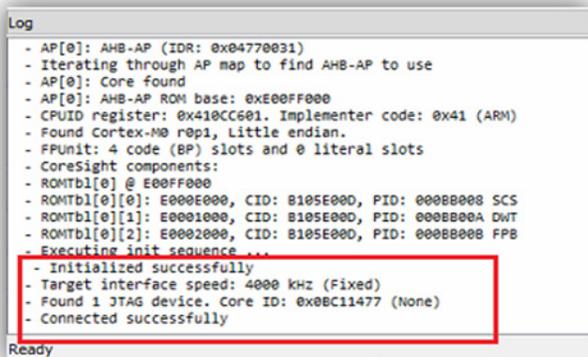- Click on the selection box
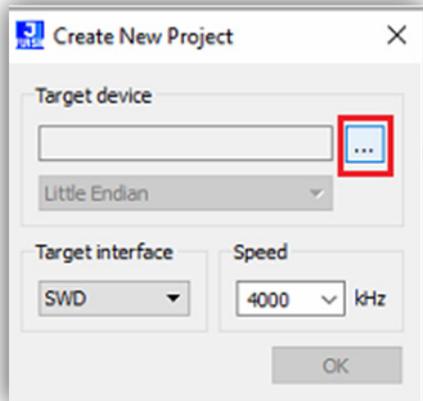
- Select FUSB15101
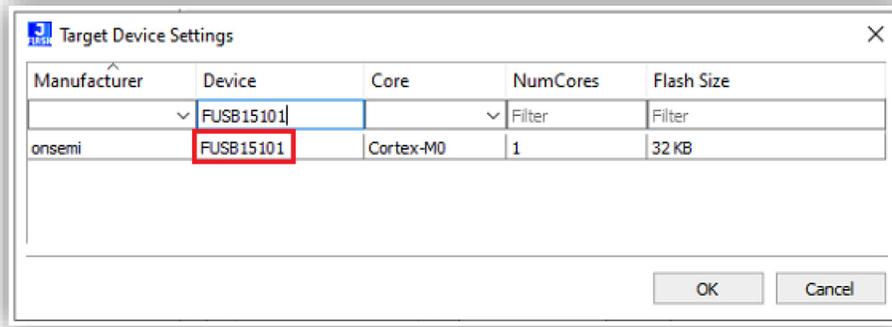
- Select Target interface: SWD
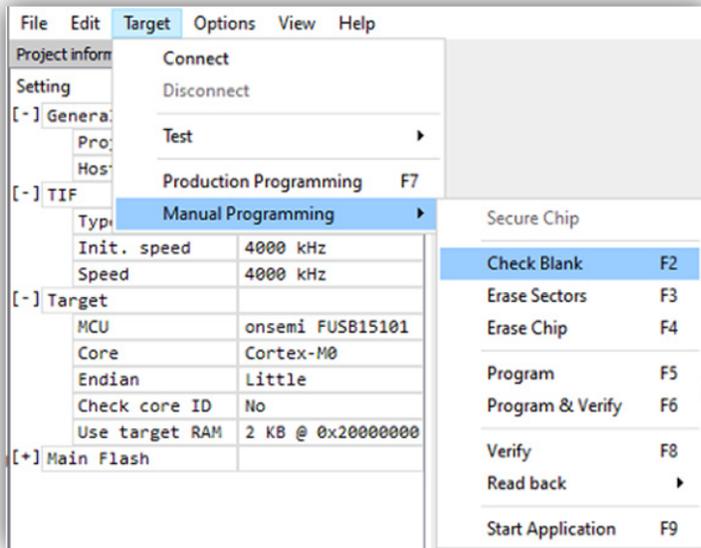- Select Speed: 4000 kHz
- Click OK for the new project to be created
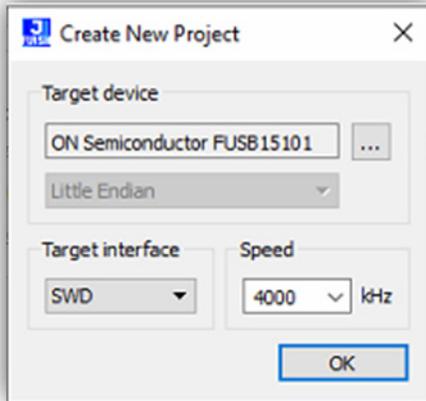
- From the menu go to Target
- Then go to Connect

  If the connection is established, you should see a message on the Log indicating a successful connection.

b) Validate OTP Chip is Blank

- Go to Target
- Go to Manual Programming
- Select Check Blank

J−Flash shall confirm the device is blank.

c) Program the FW Image with the SWD Converter Tool

- Open the SWD Converter Tool
- Select FUSB15101 from the Device list
- Select the FW Binary to use in the Select Binary field
- Click on Program OTP

Messages on the Log section shall confirm that the script processing is ongoing. When completed a message shall confirm that the OTP has been programmed successfully.
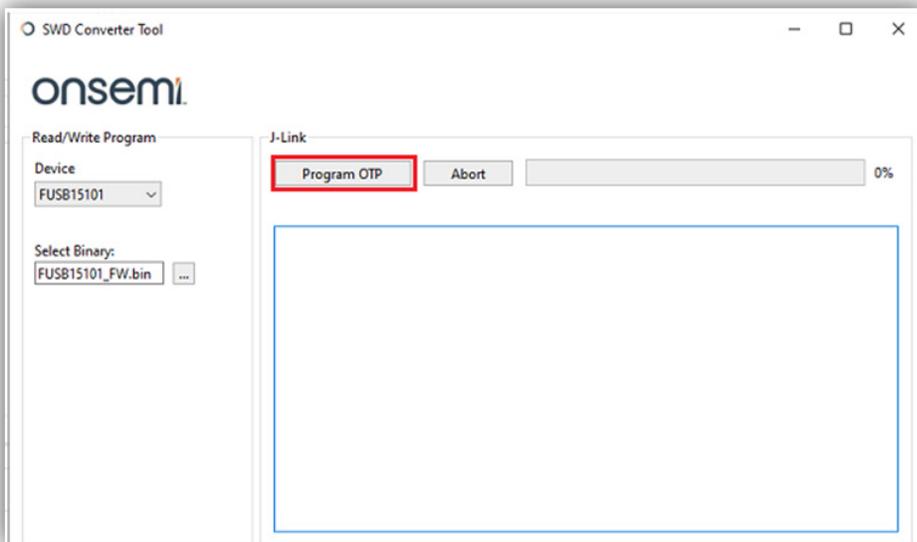
d) Validate the OTP Content

At the end of the process, users shall take the extra step to validate that programming the OTP went as expected.

- Drag the .bin file to verify into the J−Flash Window. J−Flash will ask for a start address. Enter 0 and click OK

- Go to Target

- Go to Manual Programming

- Select Verify

A message in the Log section shall state Target verified successfully.

The FW can start either by power cycling the EVB or by selecting Start Application (F9) shown also in the below screenshot.
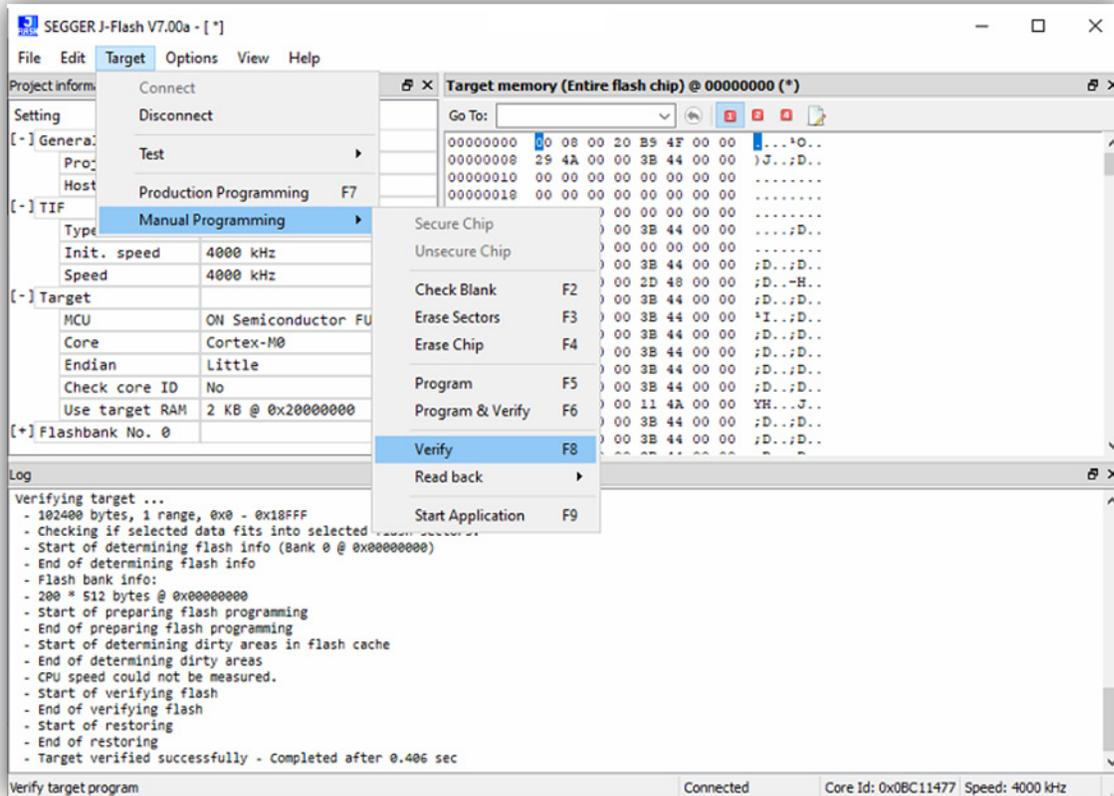
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