onsemi

FUSB15101 Single Port USB Type-C/PD Controller One-Time Programming Guide

UM70086/D

Introduction

The FUSB15101 Evaluation Board (EVB) together with the firmware binary provided in the release package permits a customer to program the one-time programmable (OTP) non-volatile memory (NVM) of the FUSB15101.

Required Hardware and Setup Instructions

A. FUSB15101 Evaluation Board (EVB)

- B. 32 kB OTP Chip labeled FUSB15101 MIN
- C. <u>SEGGER J-Link Pro</u> JTAG/SWD programming and debug probe
- D. 9-Pin Cortex-M Adapter to connect (A) the EVB to (C) J-Link Pro
- E. External Power Supply
- Use (D) the 9-Pin Adapter to connect (C) the J-Link Pro to the SWD connector (J2) on the socket EVB
- Place the OTP chip in socket
- Connect (E) the Power Supply GND to the SGND pin of (A) the EVB
- Setup (E) the Power Supply to 8.4 V (~200 mA) and connect to VIN pin (Con1) of (A) the EVB

Required Software

A. SEGGER J–Link Tools Please download and install the <u>SEGGER J–Link utility</u> *Note:* We recommend using version 7.92d. Please make sure SEGGER J–Flash is installed.

B. Serial Wire Debug (SWD) Converter Tool

Please download and install the FUSB15101 SWD Converter tool

Note: Search for keyword FUSB15101 SWD Converter Tool.

If a new J-Link version is installed, please be aware that the windows environment path needs to point to the new installation folder for SWD to function properly.

C. FUSB15101 OTP Loader

Please download the <u>FUSB15101 OTP Loader</u> used by J–Link to flash the EVB. Search for file FUSB15101_OTP_LOADER.ELF Further instructions on where to place this file will be indicated in the subsequent paragraph.

D. FUSB15101 Device List AddOn

Please download the <u>FUSB15101 Device AddOn</u> to add the FUSB15101 to the device list xml. Search for file FUSB15101_XML_ADDON.TXT



Figure 1. FUSB15101 Socket

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Adding FUSB15101 Support to J-Link

There is a need to add the FUSB15101 to the list of J-Link supported devices.

J-Link requires a device to be added in xml format as follow:
Create a directory named onsemi\FUSB15101 as follow:

C:\Users\<USER NAME>\AppData\Roaming\SEGGER\JLinkDevices\onsemi\FUSB15101\

- Rename the file (E) FUSB15101_XML_ADDON.TXT to Devices.xml and place it in the following directory: C:\Users\<USER_NAME>\AppData\Roaming\SEGGER\JLinkDevices\onsemi\FUSB15101\
- Copy the file (C) from section "Required Software" into C:\Users\<USER NAME>\AppData\Roaming\SEGGER\JLinkDevices\onsemi\FUSB15101\

Programming the OTP

- Complete the following 4 steps:
 - a. Connect J-Link to the EVB
 - b. Validate OTP chip is blank
 - c. Convert the FW Image with the SWD Converter tool
 - d. Validate OTP Content

a) Connect J-Link to the EVB

• Open the SEGGER J-Flash and select "Create new project" then "Start J-Flash"



• Click on the selection box

🔝 Create New Proje	ect X
Target device	
Little Endian	
Target interface	Speed
SWD 🔻	4000 ~ kHz
	OK

• Select FUSB15101

Settings				>
Device	Core	NumCores	Flash Size	
FUSB15101		✓ Filter	Filter	
FUSB15101	Cortex-M0	1	32 KB	
FUSB15101	Cortex-M0	1	32 KB	
			OK	Cancel
	Device V FUSB15101 FUSB15101	Settings Device Core V FUSB15101 FUSB15101 Cortex-M0	Device Core NumCores V FUSB15101 V Filter FUSB15101 Cortex-M0 1	Device Core NumCores Flash Size V FUSB15101 V Filter Filter FUSB15101 Cortex-M0 1 32 KB

- Select Target interface: SWD
- Select Speed: 4000 kHz
- Click OK for the new project to be created

Target deulse	
ON Semiconductor	FUSB15101
Little Endian	w.
Target interface	Speed
SWD 🔻	4000 V kHz
	OK

- From the menu go to Target
- Then go to Connect

If the connection is established, you should see a message on the Log indicating a successful connection.

.og	
	AP[0]: AHB-AP (IDR: 0x04770031)
-	Iterating through AP map to find AHB-AP to use
-	AP[0]: Core found
-	AP[0]: AHB-AP ROM base: 0xE00FF000
-	CPUID register: 0x410CC601. Implementer code: 0x41 (ARM)
-	Found Cortex-M0 r0p1, Little endian.
-	FPUnit: 4 code (BP) slots and 0 literal slots
-	CoreSight components:
-	ROMTD1[0] @ E00FF000
-	ROMTbl[0][0]: E000E000, CID: B105E00D, PID: 000BB008 SCS
-	ROMTbl[0][1]: E0001000, CID: B105E00D, PID: 000BB00A DWT
-	ROMTD1[0][2]: E0002000, CID: B105E00D, PID: 000BB00B FPB
	Executing init sequence
•	Initialized successfully
- I	Target interface speed: 4000 kHz (Fixed)
	Found 1 JTAG device, Core ID: 0x0BC11477 (None)
	Connected successfully
Ľ	
Rea	dy

b) Validate OTP Chip is Blank

- Go to Target
- Go to Manual Programming
- Select Check Blank
 - J-Flash shall confirm the device is blank.

File	Edit 1	Target (Options	View	Help			
Projec	t inform	Con	nect					
Settin	g	Disc	onnect					
[-] G	enera:							
	Pro:	Test		•				
	Host	Dred	luction	Dragram	mina E	,		
[-]т	IF	Prod	uction	Program	ming r			
	Тур	Man	ual Pro	grammir	ig	•	Secure Chip	
	Init.	speed	4	000 kH;	z	Charle Director D		
	Speed		4	4000 kHz			Check Blank	F2
[-] Target MCU							Erase Sectors	F3
		c	onsemi FUSB15101 Cortex-M0 Little No			Erase Chip	F4 F5 F6	
Core						0		
Endian		L				Program		
Check core ID						ID N		Program & Verify
	Use t	arget R	RAM 2	KB @ (3x2000000	3		
[+] Main Flash						Verify	F8	
							Read back	•
							Start Application	F9

c) Program the FW Image with the SWD Converter Tool

- Open the SWD Converter Tool
- Select FUSB15101 from the Device list
- Select the FW Binary to use in the Select Binary field
- Click on Program OTP

Messages on the Log section shall confirm that the script processing is ongoing. When completed a message shall confirm that the OTP has been programmed successfully.

O SWD Converter Tool			×
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Read/Write Program	J-Link		
Device FUSB15101 ~	Program OTP Abort		0%
Select Binary:			
rospision_rw.bin			

d) Validate the OTP Content

At the end of the process, users shall take the extra step to validate that programming the OTP went as expected.

- Drag the .bin file to verify into the J-Flash Window. J-Flash will ask for a start address. Enter 0 and click OK
- Go to Target
- Go to Manual Programming
- Select Verify

A message in the Log section shall state Target verified successfully.

The FW can start either by power cycling the EVB or by selecting Start Application (F9) shown also in the below screenshot.

Eile S	EGGER J-Flash V	77.00a - [*] Options View Help						.−. □	×
Project	tinform Co	onnect	5 ×	Target memory (Ent	ire flash chir) @ 0000	0000 (*)		đ×
Setting Disconnect			Go To:	~					
[-]G	eneral Pro: Te	Test Production Programming F7 Manual Programming		00000000 00 08 0 00000008 29 4A 0	0 20 B9 4	F 00 00 4 00 00	*0.)J;D.	• •	^
Host [-] TIF	Host Pr IF M			00000010 00 00 00 00000018 00 00 0	0 00 00 0	00 00 00 00 00 00 00 00 00 00 00 00			
	Typ∉ Init. spee Speed	d 4000 kHz 4000 kHz	Un	secure Chip) 00 3B 4) 00 00 0) 00 3B 4) 00 2D 4	4 00 00 0 00 00 4 00 00 8 00 00	;D.;D. ;D.,D.		
[-] Target MCU Core		ON Semiconducto Cortex-M0	n FU Era Era	еск вiank F2 se Sectors F3 se Chip F4) 00 3B 4) 00 3B 4) 00 3B 4	4 00 00 4 00 00 4 00 00	;D;D. *I;D. ;D;D.		
	Endian Check core Use target	Little ID No RAM 2 KB @ 0x200000	Pro 00 Pro	ogram F5 ogram & Verify F6) 00 3B 4) 00 3B 4) 00 3B 4) 00 11 4	3B 44 00 00 3B 44 00 00 3B 44 00 00 11 4A 00 00	;D;D. ;D;D. ;HJ.		
[+] F	lashbank No.	0	Ve	ify F8) 00 3B 4	4 00 00	;D;D.	:	~
Log Verifying target - 102400 bytes, 1 range, 0x0 - 0x18FFF - cherking if selected data fits into selected			Re- Sta	rt Application F9					8 ×
- st - F] - 20 - st - Er - St - Er - St - Er - St - St - Er - St - St - Er - St - St - St - St - St - St - St - St	eart of determin d of determinin lash bank info 00 = 512 bytes eart of preparing art of determinin 00 speed could art of verifying d of verifying art of restoring	<pre>ining flash info (Bank 0) ing flash info @ 0x00000000 ing flash programming g flash programming ining dirty areas in flas ing dirty areas not be measured. ing flash g flash g flash g</pre>	@ 0x0000000) h cache						
- Ta	rget verified	successfully - Completed	after 0.406	sec					~

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