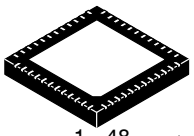
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

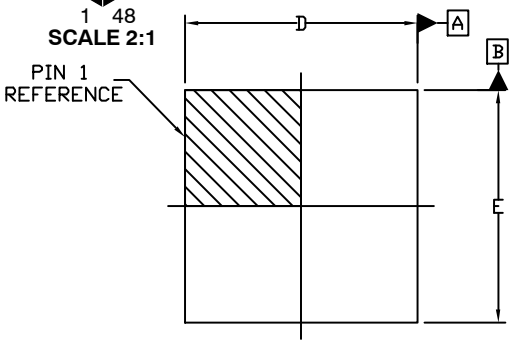
ON Semiconductor®

QFN48 7x7, 0.5P
CASE 485K−02
ISSUE D

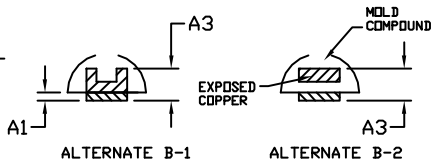
DATE 08 JAN 2019



1 48
SCALE 2:1

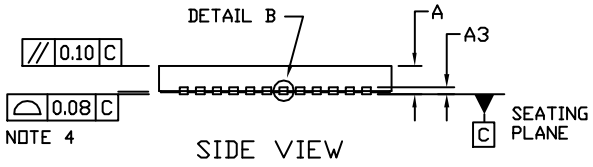


TOP VIEW

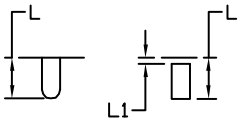


ALTERNATE B-1 ALTERNATE B-2

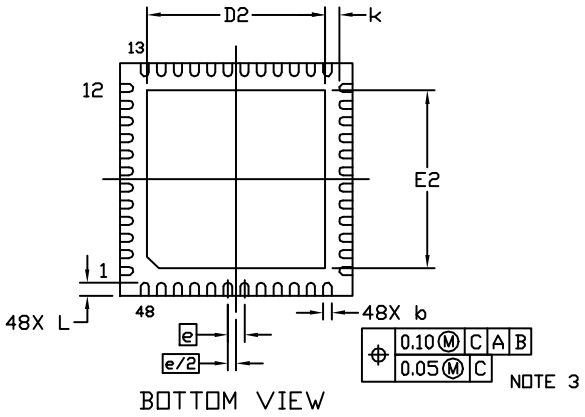
DETAIL B
ALTERNATE
CONSTRUCTION



SIDE VIEW



DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

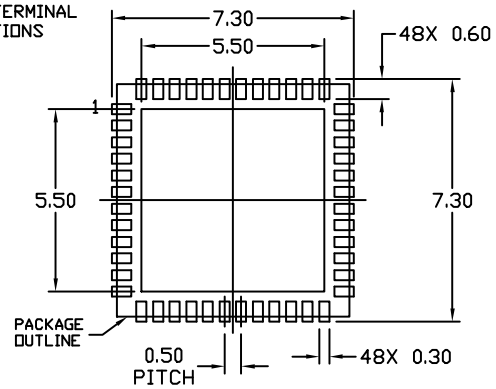


BOTTOM VIEW

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

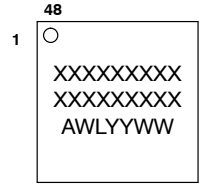
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.80	0.90	1.00
A1	0.00	---	0.05
A3	0.20 REF		
b	0.20	0.25	0.30
D	6.90	7.00	7.10
D2	5.26	5.36	5.46
E	6.90	7.00	7.10
E2	5.26	5.36	5.46
e	0.50 BSC		
K	0.39	---	---
L	0.30	0.40	0.50
L1	---	---	0.05



RECOMMENDED
MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**QFN48 7x7, 0.5P**		**PAGE 1 OF 1**