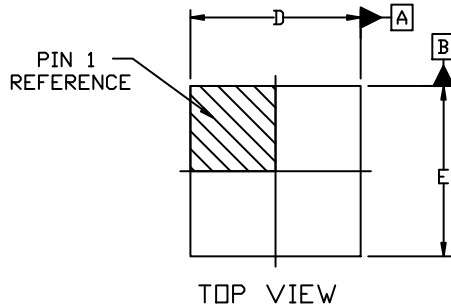
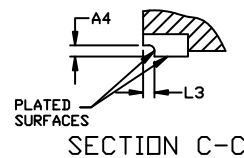
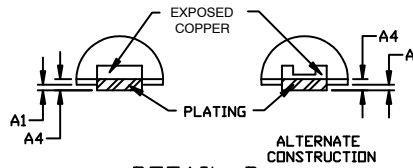
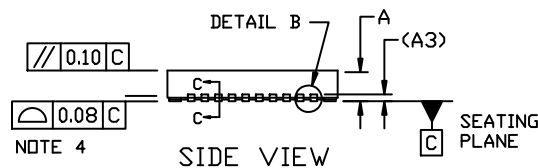

**QFNW40 5x5, 0.4P**  
**CASE 484AK**  
**ISSUE B**

DATE 19 FEB 2020

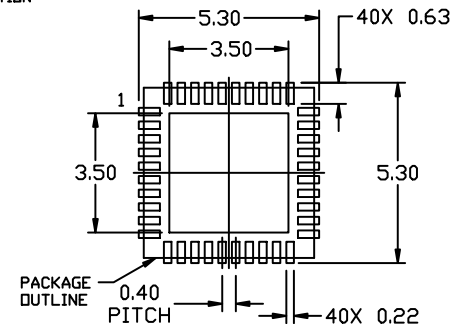
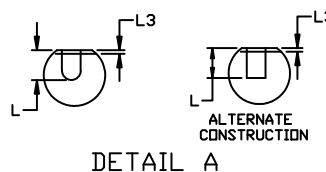
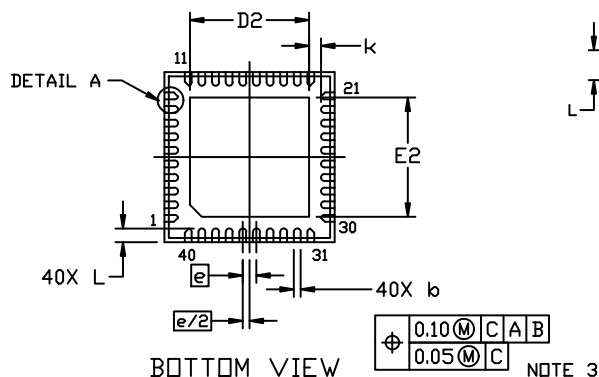
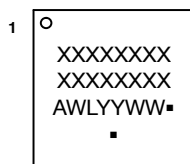


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



| DIM | MILLIMETERS |      |      |
|-----|-------------|------|------|
|     | MIN.        | NDM. | MAX. |
| A   | 0.80        | 0.85 | 0.90 |
| A1  | 0.00        | ---  | 0.05 |
| A3  | 0.20 REF    |      |      |
| A4  | 0.10        | ---  | ---  |
| b   | 0.15        | 0.20 | 0.25 |
| D   | 4.90        | 5.00 | 5.10 |
| D2  | 3.40        | 3.50 | 3.60 |
| E   | 4.90        | 5.00 | 5.10 |
| E2  | 3.40        | 3.50 | 3.60 |
| e   | 0.40 BSC    |      |      |
| K   | 0.35 REF    |      |      |
| L   | 0.30        | 0.40 | 0.50 |
| L2  | 0.12 REF    |      |      |
| L3  | ---         | ---  | 0.09 |


**GENERIC MARKING DIAGRAM\***


XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
YY = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

|                         |                         |  |
|-------------------------|-------------------------|--|
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| <b>DESCRIPTION:</b>     | <b>QFNW40 5x5, 0.4P</b> | <b>PAGE 1 OF 1</b>   |

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