NCP1655MM500WGEVB Test Procedure

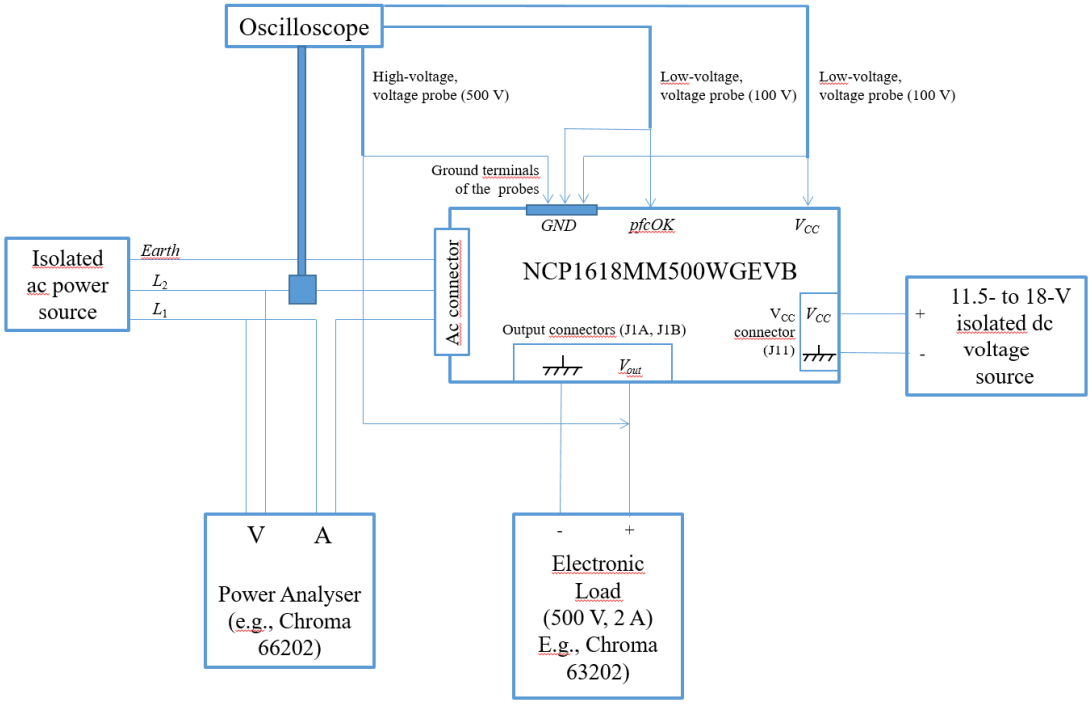

Figure 1 – Set-up for board testing – Simplified schematic

Note that no circuitry to discharge the X2 capacitors of the EMI filter is implemented Also note that the EVB delivers a voltage in the range of 400 V (V_{out} = 388 V nominally), leading to the risk of a severe electric chock, if improperly handled. Get sure that the output capacitor is properly discharged before manipulating the board. The electronic load can be used to discharge V_{OUT}.

1. Equipments for measurement.

The board testing set-up is shown in Figure 1:

- Apply an electronic load across the output (between the "V_{OUT}" and "GND" terminals of the board). This equipment will adjust the current I_{LOAD} that loads the evaluation board.
- Place a power analyzer able to measure the power factor ("PF") and the Total Harmonic Distortion ("THD") of the current absorbed from the ac power source.
- Connect the board to a 600-W or more, 50-Hz/60-Hz, isolated ac power source. This source will adjust the sinusoidal input voltage, V_{in}, that is applied to the evaluation board. The rms value of V_{in} must stay below 265 V.
- Apply an isolated dc power source to the J11 socket to provide the circuit V_{CC} voltage. This power source must deliver a voltage between 11.5 V and 18.0 V and a current of 50 mA
- The cable connecting the EVB ac connector to the isolated ac power source must allow the connection of a current probe. This cable must be able to see 8 A rms. Note that if high (0.2 Ω or more), the series resistor can cause a significant voltage drop between the voltage provided by the ac source and the voltage actually applied to the EVB.

The board contains high-voltage and hot, live parts.
It must not be handled except by experienced professionals.
Be very cautious when manipulating or testing it. It is the responsibility of the board users, to take all the precautions to avoid electric hazards and any other pains.

- The output cable placed between the EVB output and the electronic load must be able to sustain 500 V / 2 A dc or more.
- The sequencing should be:
  - Power on:
    i. Turn on the electronic load and set the load current
    ii. Turn on the isolated ac power source and the V_{CC} isolated dc voltage source in any order unless specified
  - Power off:
    i. Turn off the isolated ac power source and the V_{CC} dc voltage source in any order unless specified
    ii. Turn off the electronic load. Before disabling the electronic load, **it is recommended to get sure that the output capacitor is discharged**.

2. Measurements

Startup Sequences

A "cold startup phase" is performed at low line (115 V rms) and full load (1.3 A). The time Δt denotes the delay from the moment when the EVB is powered to the moment when the output voltage (signal V_{out} of Figure 2) is high enough to enable the downstream converter (see Figure 2).
Actually, two cases can be tested:

- The board is plugged in while the circuit is already fed. See the "Startup sequence, V_{CC} being applied first" section.
- The board is first plugged in and operation is started when the circuit is powered. See the "Startup sequence, V_{in} being applied first" section.

Below plots were obtained with 16 V being provided by the V_{CC} dc voltage source

- Startup sequence, V_{CC} being applied first

The board powering instant can be detected by observing the line current. This is the moment when I_{LINE} abruptly takes place to charge the output voltage to the line peak voltage. On the other hand, the pfcOK signal turns high when the output voltage is high enough to enable the downstream converter. Hence time Δt can be measured as the time interval between the moment when the output voltage starts to charge to the line peak voltage and the moment when pfcOK gets high. See below.
Δt must be less than 200 ms.

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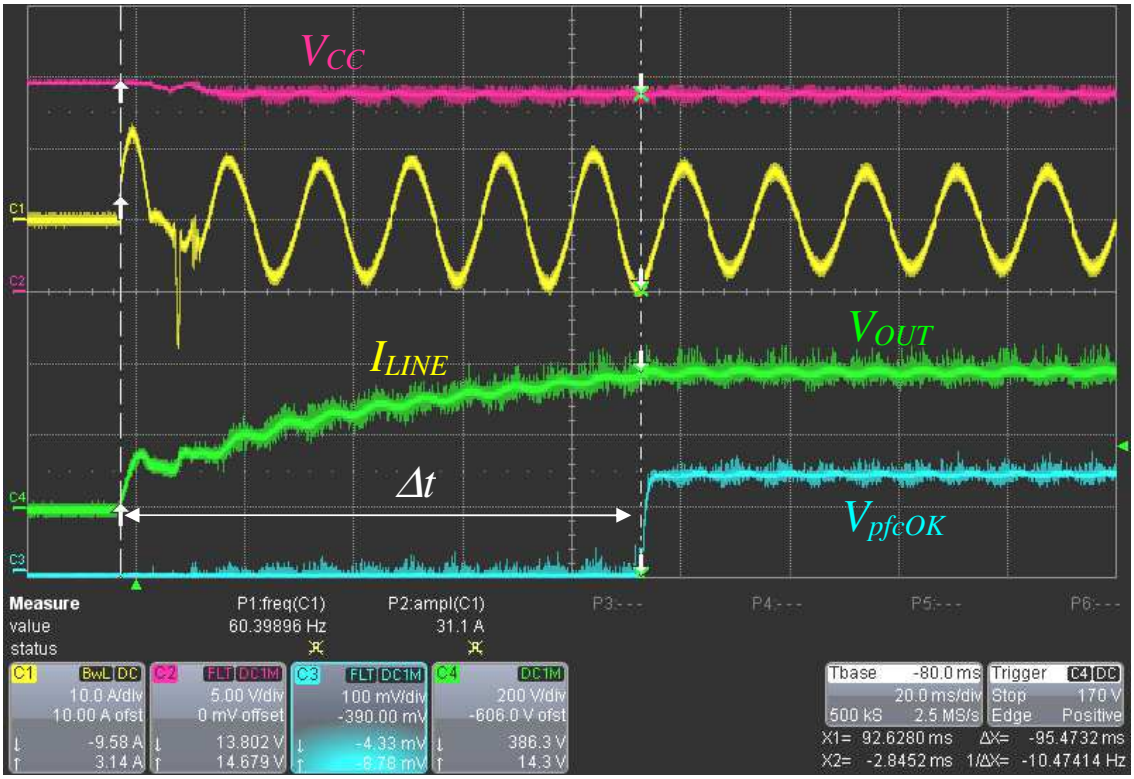

Figure 2 – Start-up phase

- **Startup sequence, V_{in} being applied first**

The ac input voltage is first applied to the board, leading the output voltage to charge to the line peak voltage. However, the PFC stage remains off until the NCP1655 is powered by the V_{CC} dc voltage source. At that moment, the PFC stage enters operation mode. Again, the pfcOK signal turns high when the output voltage is high enough to enable the downstream converter. Hence time ***Δt*** can be measured as the time interval between the moment when the NCP1655 V_{CC} voltage is applied and the moment when pfcOK gets high. See below. ***Δt* must be less than 200 ms**.

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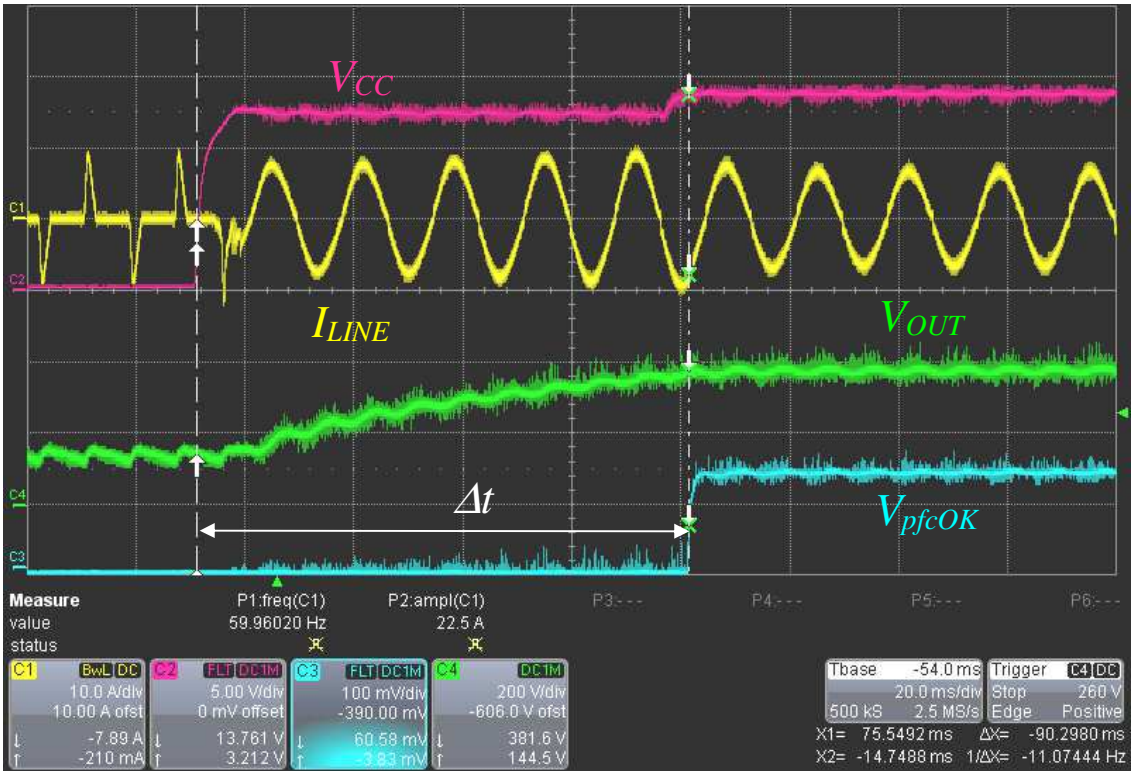
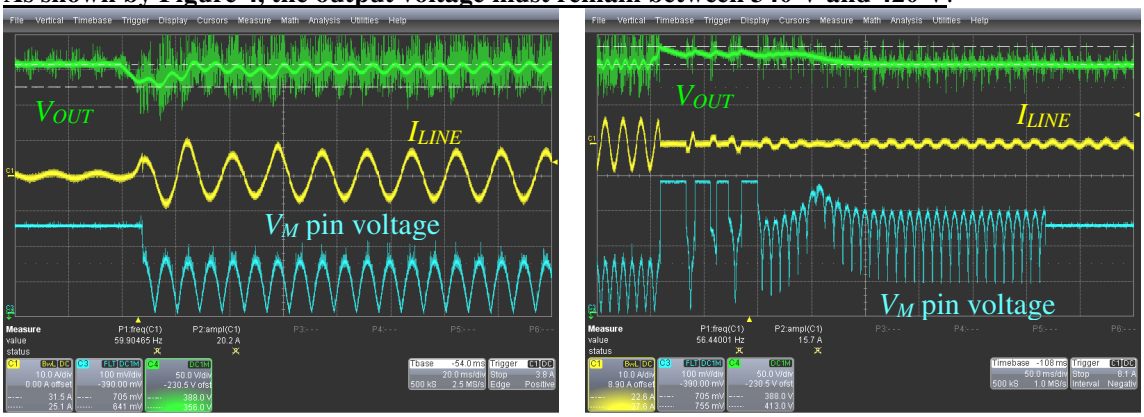


Figure 3 – Start-up phase

Load Steps

At 115 V rms, the load is abruptly changed every second, from 0.13 A to 1.30 A (respectively 10% and 100% of the full load) and vice versa, with 2-A/µs edges.

As shown by Figure 4, the output voltage must remain between 340 V and 420 V.



a) Rising load step b) Falling load step

Figure 4 – 10% to 100% load steps at 115 V rms

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V_{OUT}, PF and THD measurements:

The average value of the output voltage (V_{OUT}) can be measured using the electronic load. If not allowed by the electronic load, a volt-meter can be used instead.

Proposed measurements:

Parameters	Comments	Limits
$V_{in,rms}$ = 115 V, I_{LOAD} = 0.4 A		
V_{OUT}	Voltage measured between "V_{OUT}" and "GND"	370 V < V_{OUT} < 400 V
PF	Power Factor	> 0.980
THD	Total Harmonic Distortion	< 10 %
$V_{in,rms}$ = 115 V, I_{LOAD} = 1.2 A		
V_{OUT}	Voltage measured between "V_{OUT}" and "GND"	370 V < V_{OUT} < 400 V
PF	Power Factor	> 0.990
THD	Total Harmonic Distortion	< 10 %
$V_{in,rms}$ = 230 V, I_{LOAD} = 0.4 A		
V_{OUT}	Voltage measured between "V_{OUT}" and "GND"	370 V < V_{OUT} < 400 V
PF	Power Factor	> 0.960
THD	Total Harmonic Distortion	< 20 %
$V_{in,rms}$ = 230 V, I_{LOAD} = 1.2 A		
V_{OUT}	Voltage measured between "V_{OUT}" and "GND"	370 V < V_{OUT} < 400 V
PF	Power Factor	> 0.980
THD	Total Harmonic Distortion	< 20 %

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