NCP1618MM500WGEVB Test Procedure

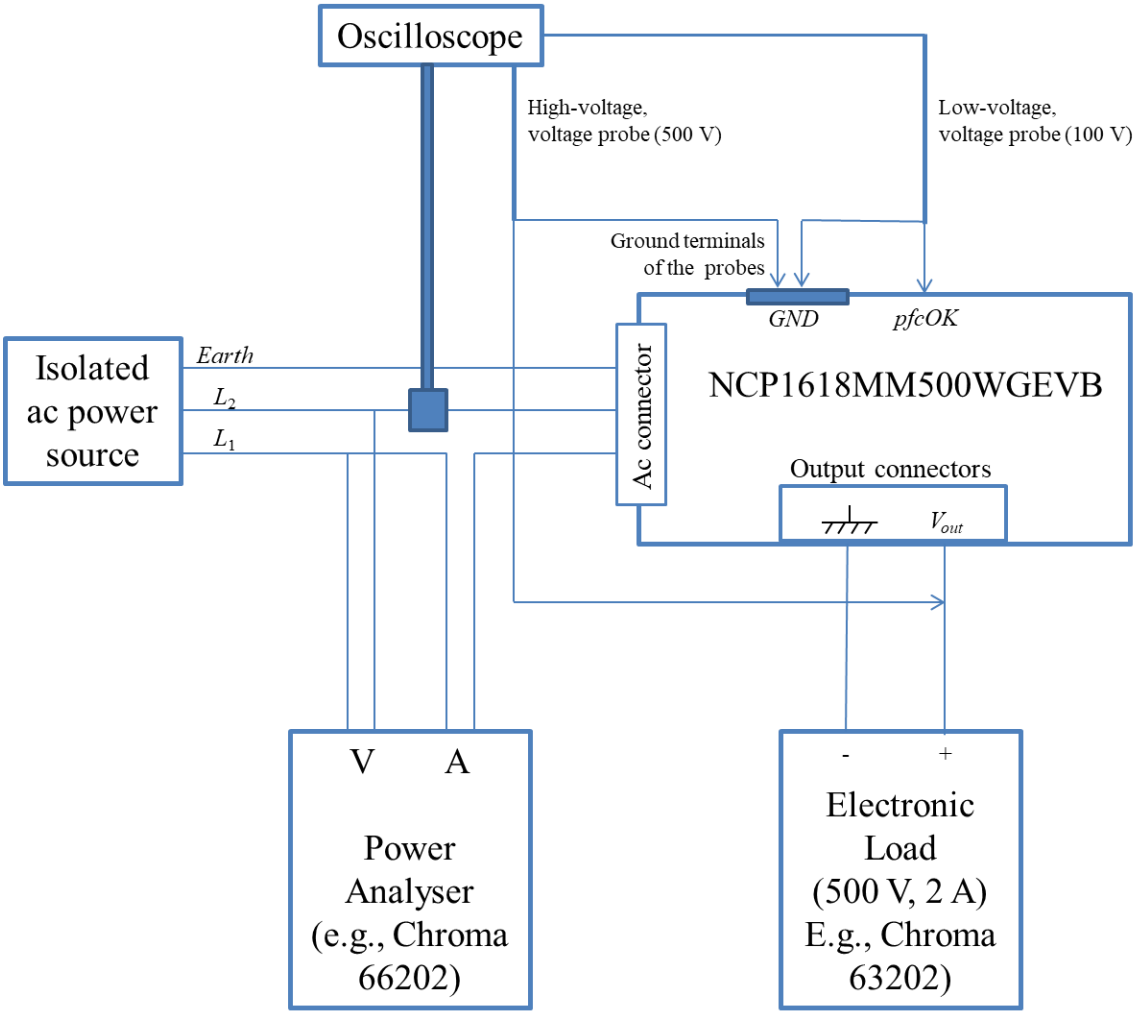

Figure 1 – Set-up for board testing – Simplified schematic

The EVB delivers a voltage in the range of 400 V (V_{out} = 388 V nominally), leading to the risk of a severe electric chock, if improperly handled. Get sure that the bulk capacitor is properly discharged before manipulating the board. The electronic load can be used to discharge V_{out}.

1. Equipments for measurement.

The board testing set-up is shown in Figure 1:

- Apply an electronic load across the output (between the "V_{OUT}" and "GND" terminals of the board). This equipment will adjust the current $\boldsymbol{I_{LOAD}}$ that loads the evaluation board.
- Place a power analyzer able to measure the power factor ("PF") and the Total Harmonic Distortion ("THD") of the current absorbed from the ac power source.

The board contains high-voltage and hot, live parts. It must not be handled except by experienced power supply professionals.

Be very cautious when manipulating or testing it. It is the responsibility of the board users, to take all the precautions to avoid electric hazards and any other pains.

- Connect the board to a 600-W or more, 50-Hz/60-Hz, isolated ac power source. This source will adjust the sinusoidal input voltage, V_{in}, that is applied to the evaluation board. The rms value of V_{in} must stay below 265 V.
- The cable connecting the EVB ac connector to the isolated ac power source must allow the connection of a current probe. This cable must be able to see 8 A rms. Note that if high (0.2 Ω or more), the series resistor can cause a significant voltage drop between the voltage provided by the ac source and the voltage actually applied to the EVB.
- The output cable placed between the EVB output and the electronic load must be able to sustain 500 V / 2 A dc or more.

2. Measurements

- **Startup Sequence**

A "cold startup phase" is performed at low line (115 V rms) and full load (1.3 A). The time Δt denotes the delay from the moment when the EVB is powered to the moment when the output voltage (signal V_{BULK} of Figure 2) is high enough to enable the downstream converter (see Figure 2).
The board powering instant can be detected by observing the output voltage. This is the moment when V_{BULK} abruptly charges up to the line peak voltage. On the other hand, the pfcOK signal turns high when the output voltage is high enough to enable the downstream converter. Hence time Δt can be measured as the time interval between the moment when the output voltage has charged to the line peak voltage and the moment when pfcOK gets high. See below.
Δt must be less than 650 ms.

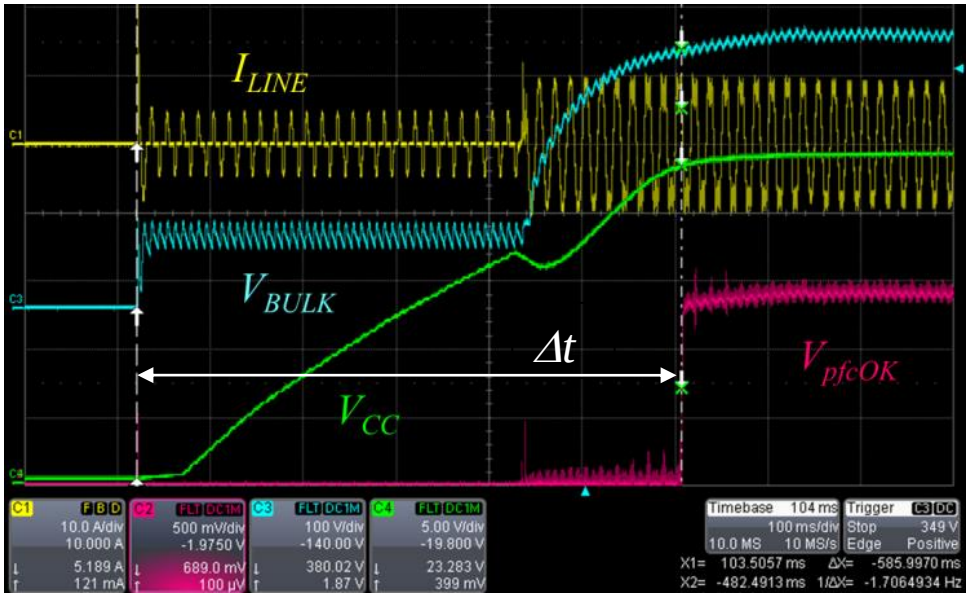

Figure 2 – Start-up phase

- **Load Steps**

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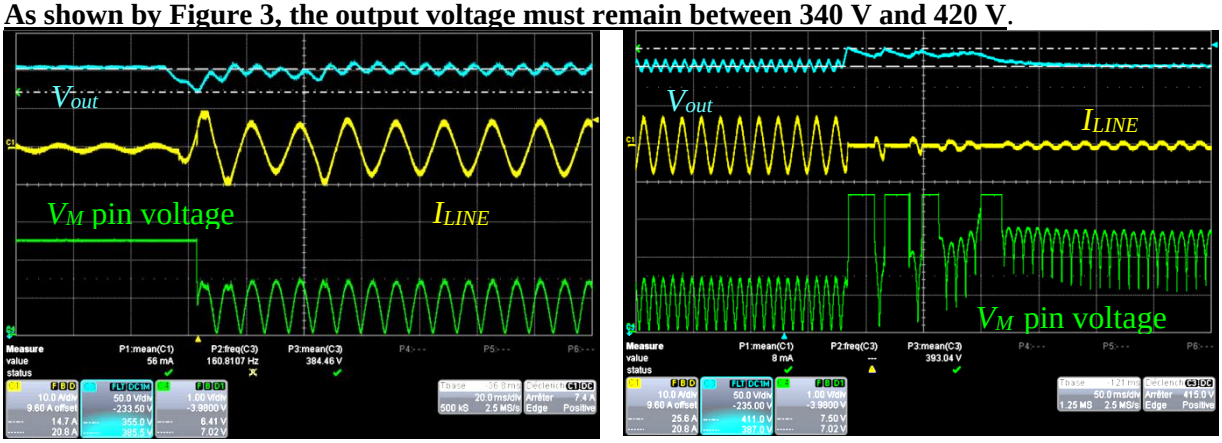
At 115 V rms, the load is abruptly changed every second, from 0.13 A to 1.30 A (respectively 10% and 100% of the full load) and vice versa, with 2-A/µs edges.
As shown by Figure 3, the output voltage must remain between 340 V and 420 V.



a) Rising load step b) Falling load step

Figure 3 – 10% to 100% load steps at 115 V rms

- ***V*$_{BULK}$, PF and THD measurements:**

The average value of the output voltage (V_{BULK}) can be measured using the electronic load. If not allowed by the electronic load, a volt-meter may be used instead.

Proposed measurements:

Parameters	Comments	Limits
$V_{in,rms}$ = 115 V, I_{LOAD} = 0.4 A		
V_{BULK}	Voltage measured between "V_{OUT}" and "GND"	380 V < V_{BULK} < 400 V
PF	Power Factor	> 0.980
THD	Total Harmonic Distortion	< 10 %
$V_{in,rms}$ = 115 V, I_{LOAD} = 1.2 A		
V_{BULK}	Voltage measured between "V_{OUT}" and "GND"	380 V < V_{BULK} < 400 V
PF	Power Factor	> 0.990
THD	Total Harmonic Distortion	< 10 %
$V_{in,rms}$ = 230 V, I_{LOAD} = 0.4 A		
V_{BULK}	Voltage measured between "V_{OUT}" and "GND"	380 V < V_{BULK} < 400 V
PF	Power Factor	> 0.950
THD	Total Harmonic Distortion	< 10 %
$V_{in,rms}$ = 230 V, I_{LOAD} = 1.2 A		
V_{BULK}	Voltage measured between "V_{OUT}" and "GND"	380 V < V_{BULK} < 400 V
PF	Power Factor	> 0.975

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THD	Total Harmonic Distortion	< 20 %

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