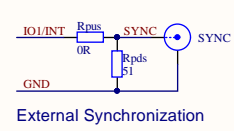
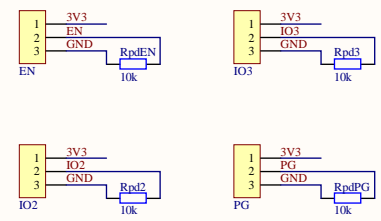


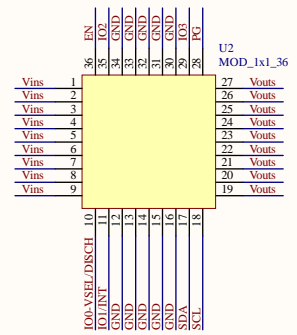
0.5x0.5 inch PCB Module



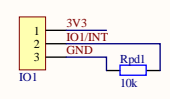
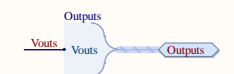
External Synchronization



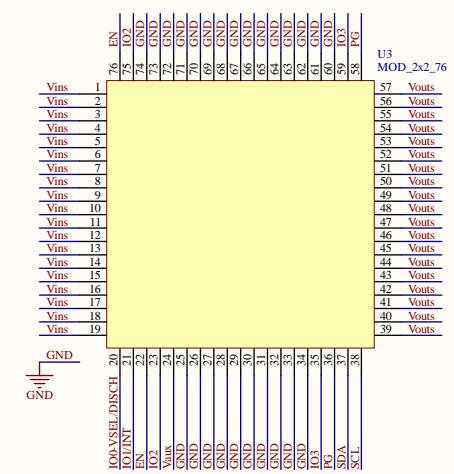
IO Control, Connection and Test Pins



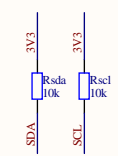
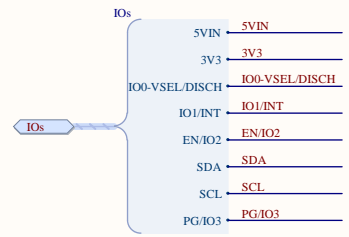
1x1 inch PCB Module



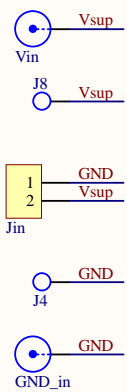
IO Control, Connection and Test Pins



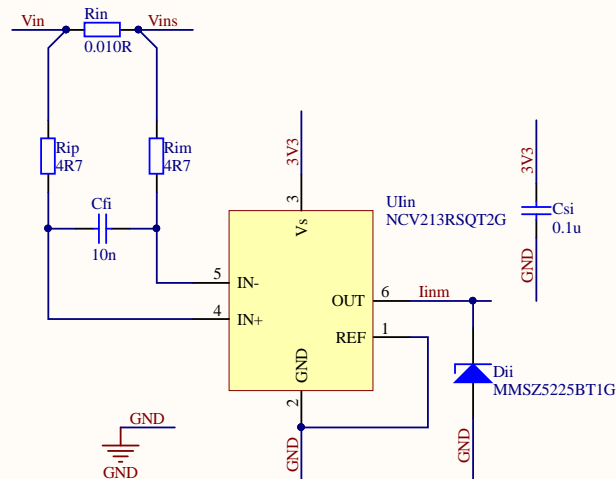
2x2 inch PCB Module



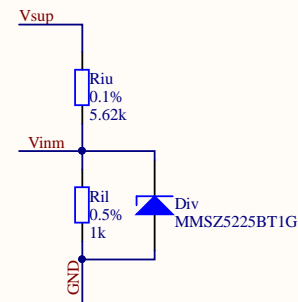
ON Semiconductor			
Title			
Size A3	Document Number		Rev 1
Date: 7/10/2020	12:14:19 PM	Sheet 1 of 5	
File: Modules.SchDoc	Drawn by: F. Valero / T. Krecsek		



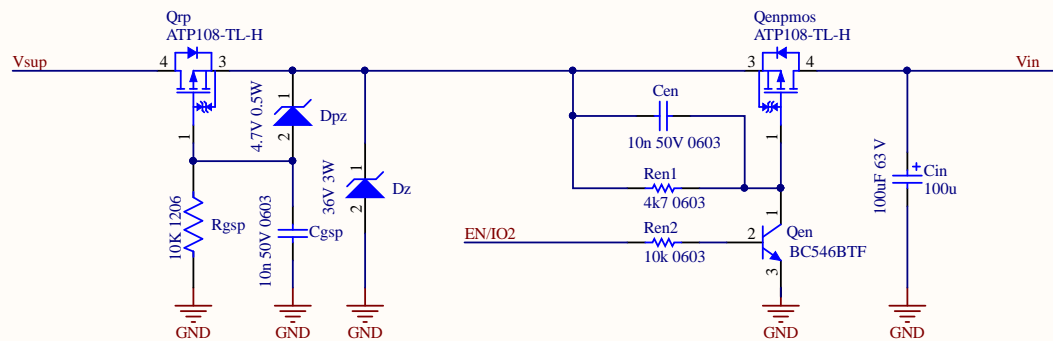
Input Terminals and Test Pins



Input Current Measurement  
Max. 5 A DC !!!

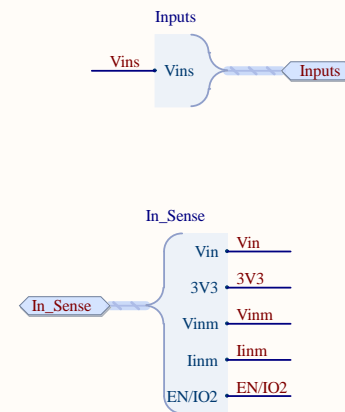


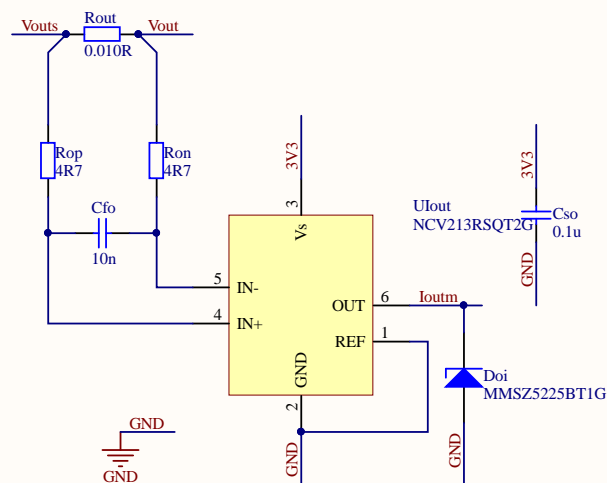
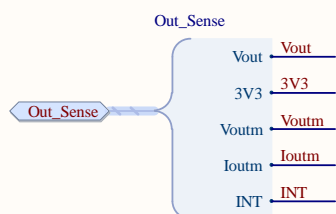
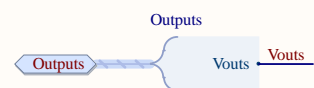
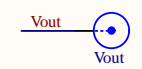
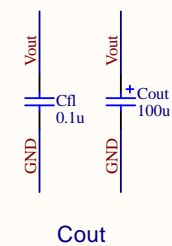
Input Voltage Measurement  
Max. 20 V DC !!!




Reverse Polarity

Enable if input voltage is good





Output Current Measurement  
Max. 5 A DC !!!

 <b>Semiconductor</b>			
<b>Title</b> <b>Strata PCB Module Evaluation Board</b>			
<b>Size</b> <b>A4</b>	<b>Document Number</b>		<b>Rev</b> <b>1</b>
<b>Date:</b> 7/10/2020	12:14:19 PM	<b>Sheet</b>	<b>of</b> 5
<b>File:</b> Output_Terminals_Sensing.SchDoc		<b>Drawn by:</b> F. Valero / T. Kreck	

A

B

C

D

A

B

C

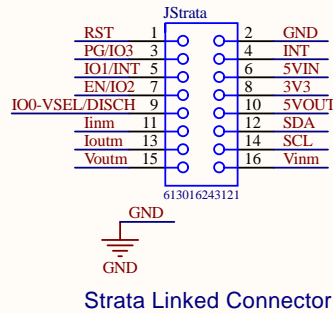
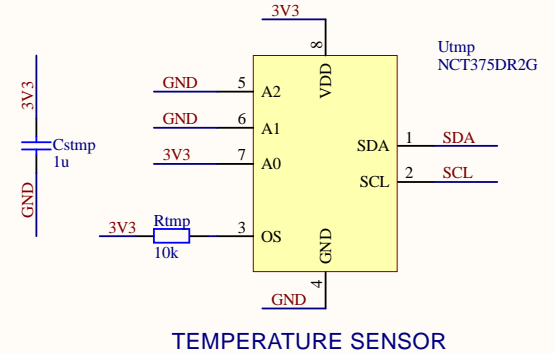
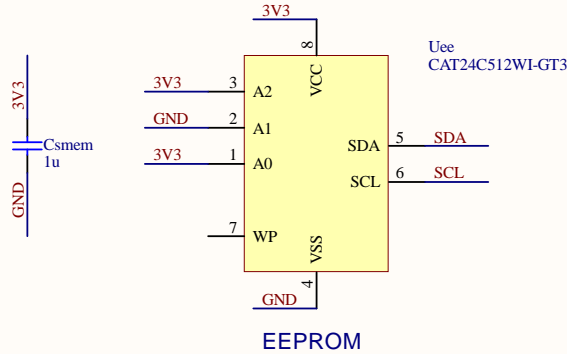
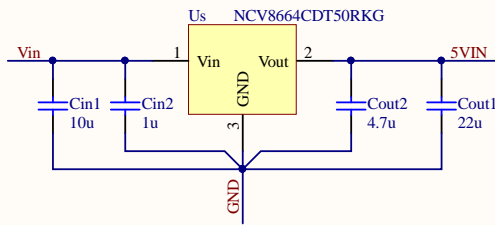
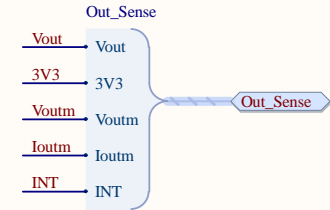
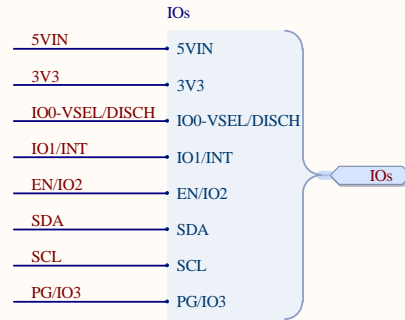
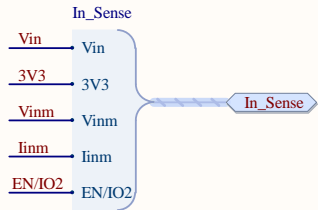
D

1

2

3

4



Connect A0, A1, and A2 depending on type of PCB

Slave address  
000 - 0x55 - General purpose  
001 - 0x51 - Reserved  
010 - 0x52 - Reserved  
011 - 0x53 - Reserved  
100 - 0x54 - Front end (ADC)  
101 - 0x55 - Middle (DAC) <-Slave Addressed Used  
110 - 0x56 - Other logic  
111 - 0x57 - Strata use only (DUT board)

Title			
Strata PCB Module Evaluation Board			
Size A4	Document Number		Rev 1
Date:	7/10/2020	12:14:19 PM	Sheet of 5
File:	Strata_Circuits	Terminals.SchDoc	Drawn by: F. Valero / T. Krecek

1

2

3

4

1

A

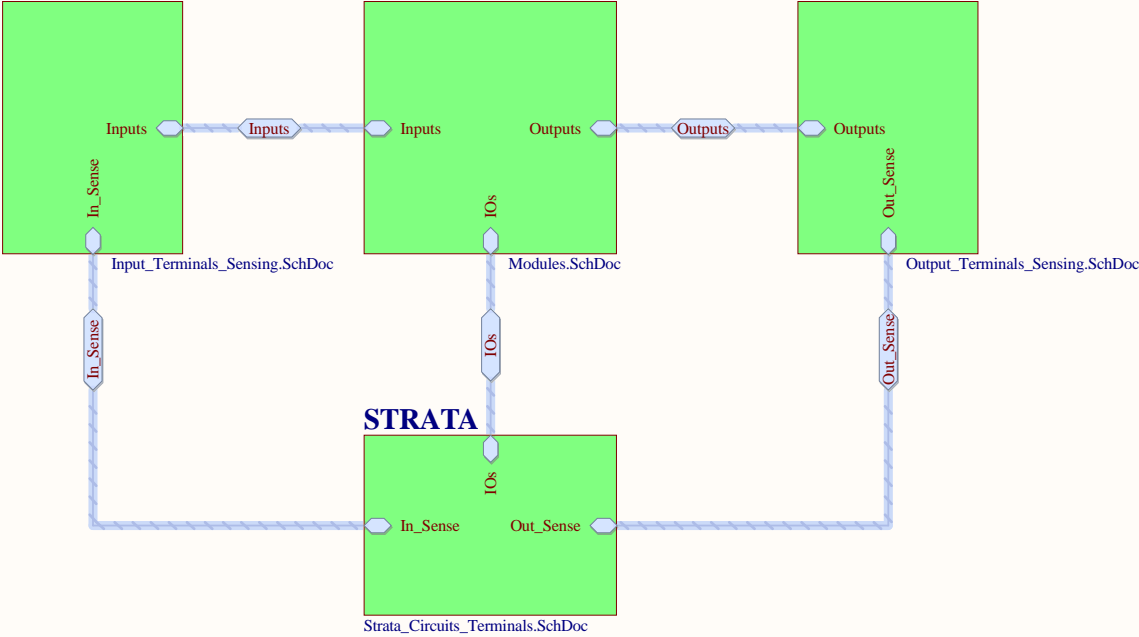
INPUT MEASUREMENTS

2

PCB MODULES

3

OUTPUT MEASUREMENTS



D

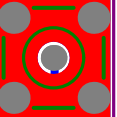
Semiconductor			
Title Strata PCB Module Evaluation Board			
Size A4	Document Number		Rev 1
Date: 7/10/2020	12:14:20 PM	Sheet of 5	
File: Strata_Motherboard_TOP.SchDoc		Drawn by: F. Valero / T. Krecek	

D

# Strata LV DC-DC Ecosystem



LOAD TRANSIENT



GND\_in

GND\_out

U3

EN 102

GND

103 PG

V<sub>in</sub>

V<sub>in</sub>

V<sub>in</sub>

V<sub>in</sub>

V<sub>out</sub>

V<sub>out</sub>

V<sub>out</sub>

J<sub>out</sub>

C<sub>out</sub>

V<sub>out</sub>

V<sub>out</sub>

100

101

EN

102

V<sub>aux</sub>

GND

103

PG

SDA

SCL

No jumpers for 100, 101, EN, 102 headers when Strata MCU board is plugged in!

Wireless Strata  
Linked PS140

No jumpers for 103, PG headers when Strata MCU board is plugged in!

RoHS Compliant