


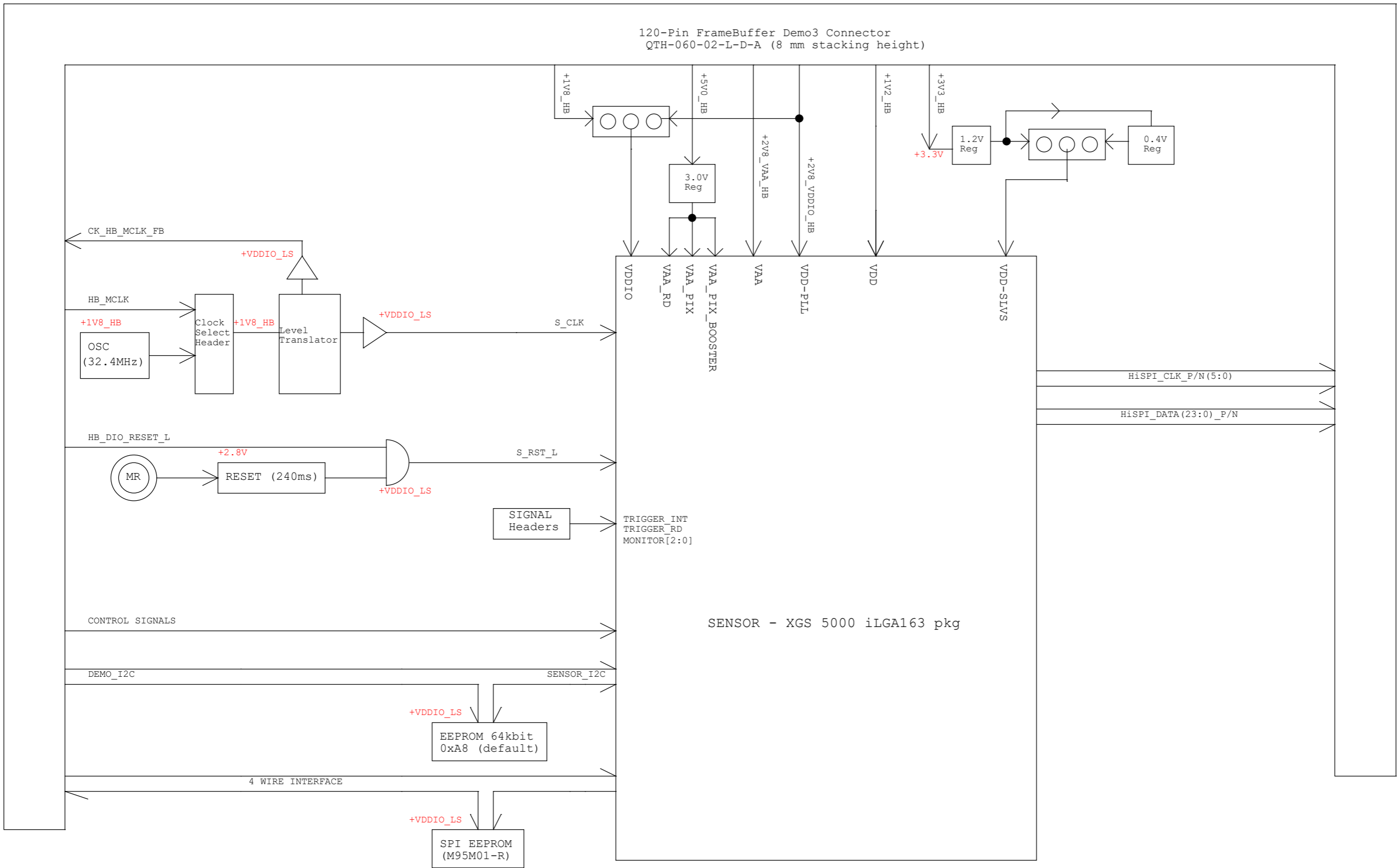
# XGS 5000\_iLGA163\_SER\_FBD\_HEAD

Page	Description
1	Title Page
2	Block Diagram
3	Sensor
4	Power
5	Clock and Reset
6	External Interfaces

Rev	Who	Date	Description
Rev 0.0	aralex	01MAR19	Initial; Reuse of XGS16000 in LGA163 package Framebuffer demo headboard design This PCB is a resilk of the XGS 16000 FBD Headboard REV 0. Only the sensor is changed to XGS 5000 in this design.
Rev 0.1	aralex anahar	05APR19 23NOV20	Changed Part number of U7 to a device with Threshold voltage of 2.32V in same family and footprint. No electrical change Updated P2 and P15 Jumpers setting default as 1-2 instead of open. Refer HARDWARE-3335, dt. 20NOV2020
Rev 1.0	anahar	5MAR21 16APR21	Initial; Reuse of XGS16000 rev1 Framebuffer demo headboard design. Added P4 Header text as Closed

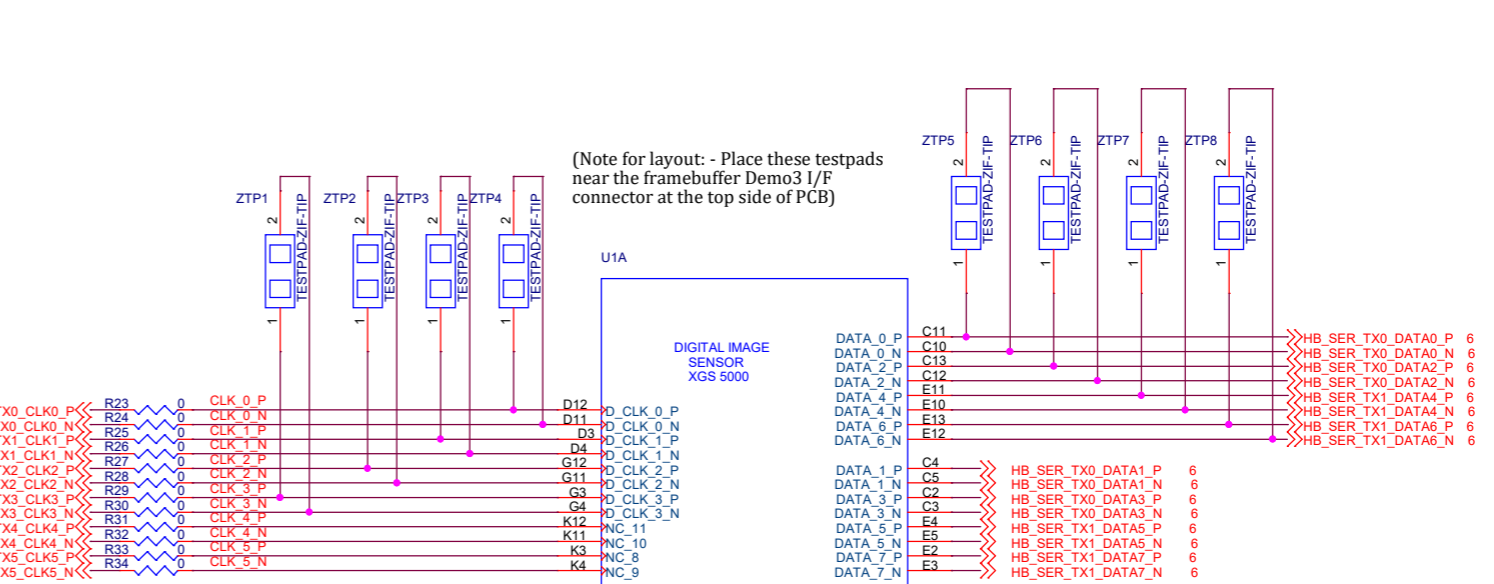
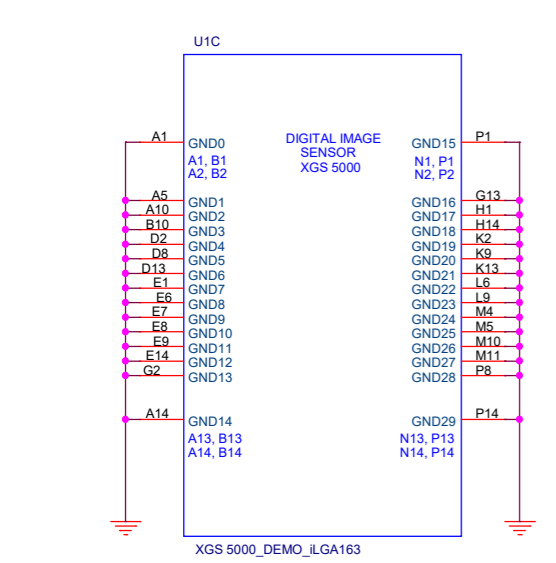
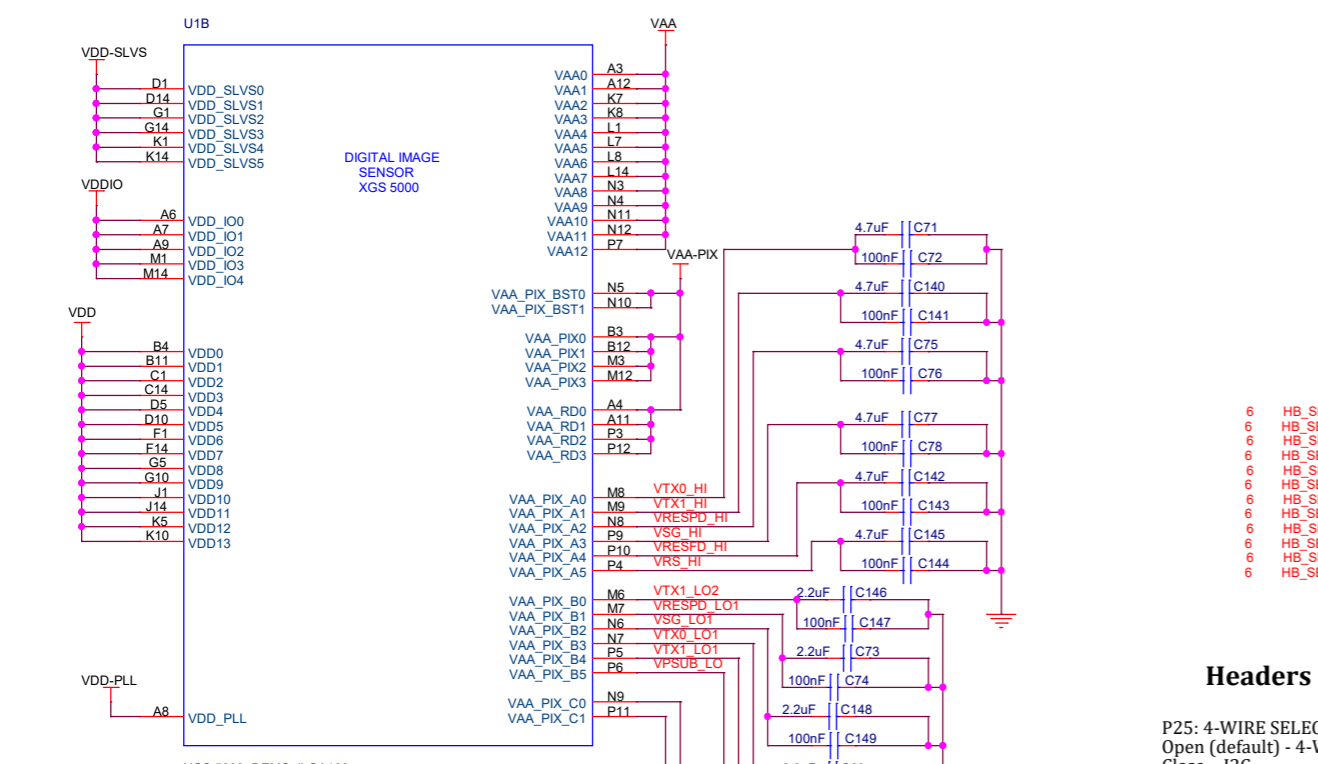
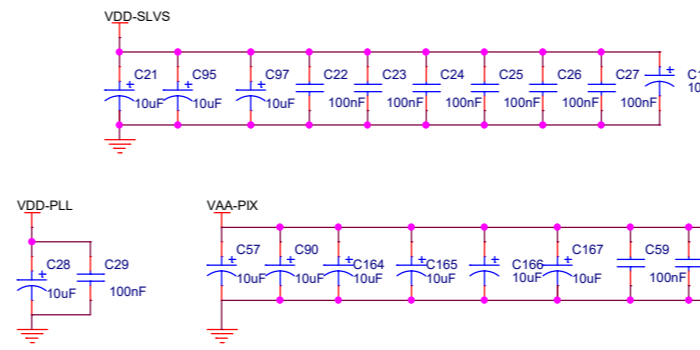
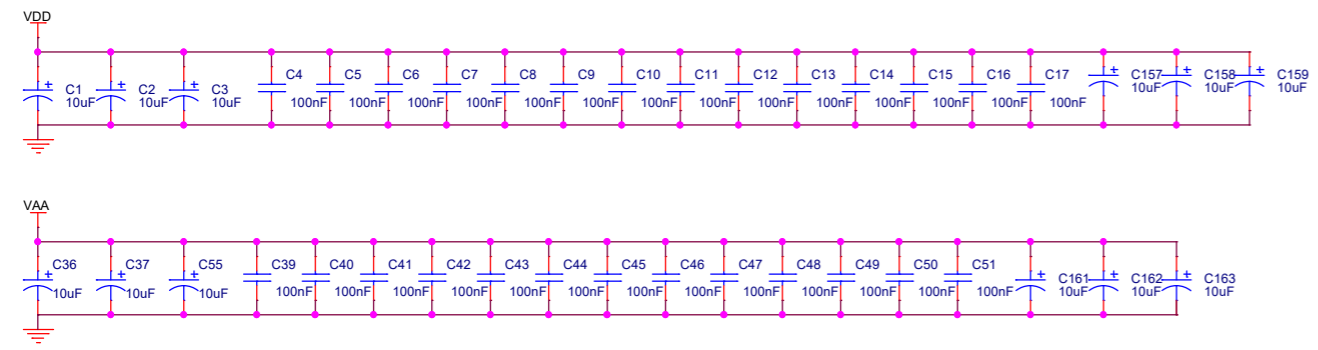
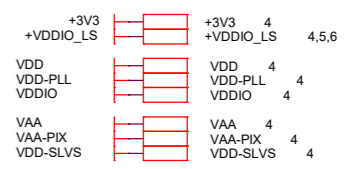
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Title Page		
Size C	Document Name XGS 5000_iLGA163_SER_FBD_HEAD	Rev 1.0
Date: Friday, April 16, 2021	Sheet 1 of 6	

# Block Diagram



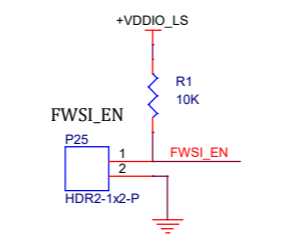
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Title: Block Diagram		
Size: C	Document Name: XGS 5000_iLGA163_SER_FBD_HEAD	Rev: 1.0
Date: Friday, March 05, 2021	Sheet: 2	of 6

# XGS 5000 in iLGA163 pkg

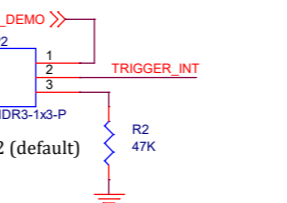


## Headers

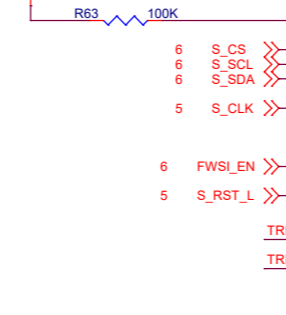
P25: 4-WIRE SELECTION / I2C  
Open (default) - 4-WIRE  
Close - I2C



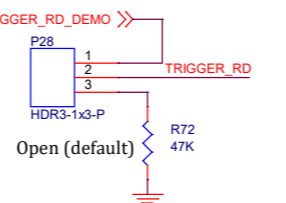
TRIGGER\_INT



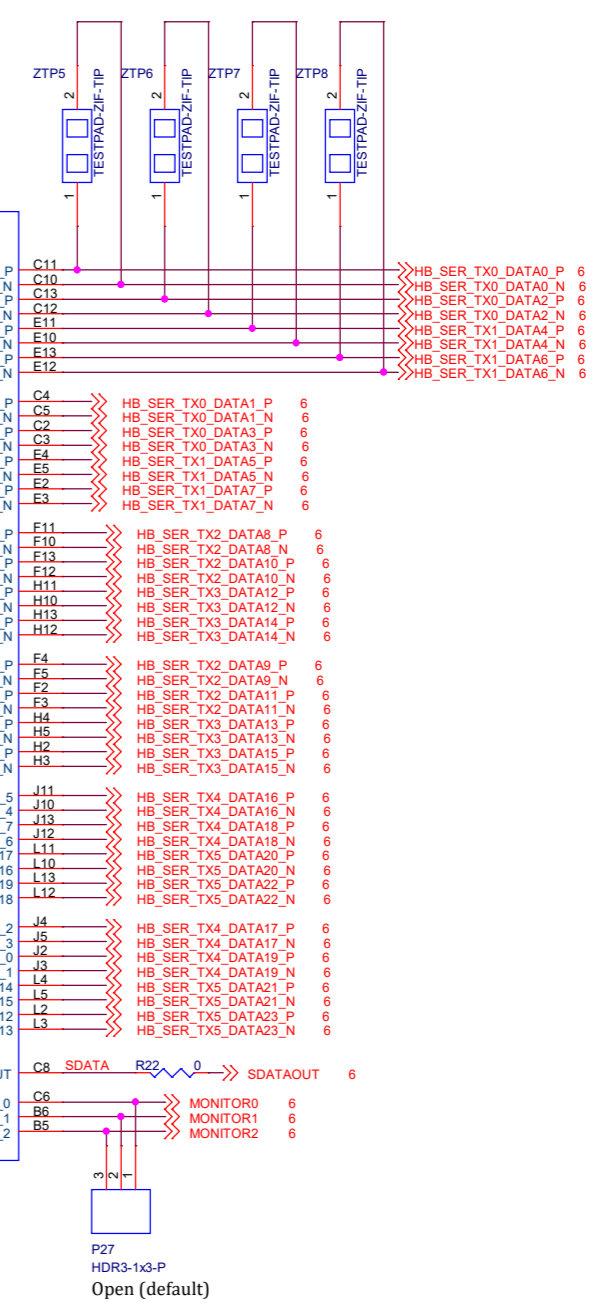
+VDDIO\_LS



TRIGGER\_RD



(Note for layout: - Place these testpads near the framebuffer Demo3 I/F connector at the top side of PCB)

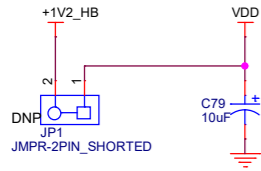


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Title: Sensor  
Document Name: XGS 5000\_ILGA163\_SER\_FBD\_HEAD  
Rev: 1.0  
Date: Friday, March 05, 2021  
Sheet: 3 of 6

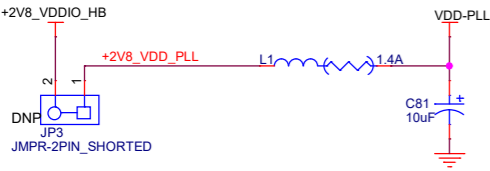
Debug Headers: Cut away the shorted trace and mount header for power debugging

# Power

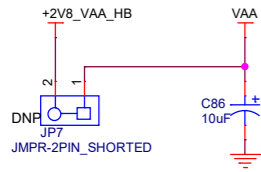
## VDD 1.2V SUPPLY



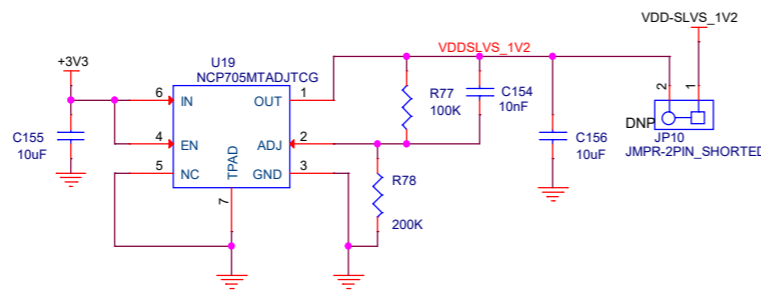
## VDD-PLL 2.8V SUPPLY



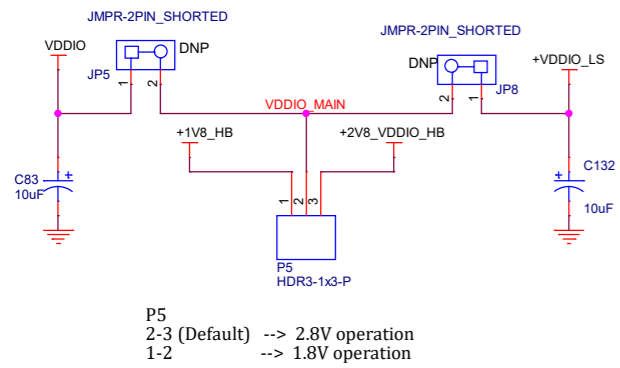
## VAA 2.8V SUPPLY



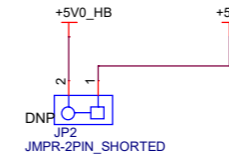
## VDDSLVSPHY 1.2V SUPPLY



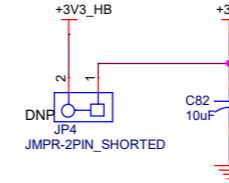
## VDDIO 1.8V / 2.8V SUPPLY



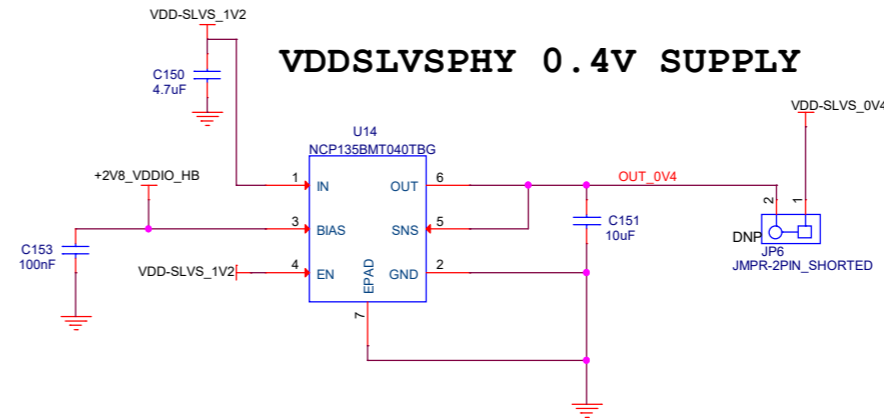
## PERIPHERAL 5.0V SUPPLY



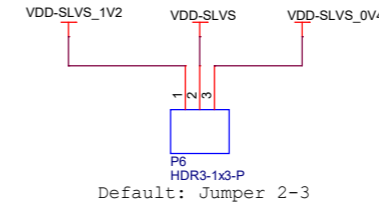
## PERIPHERAL 3.3V SUPPLY



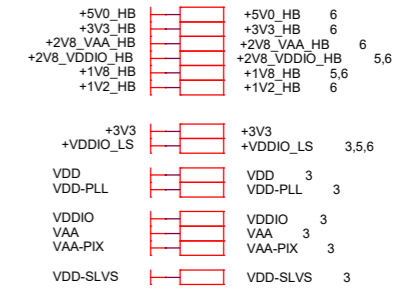
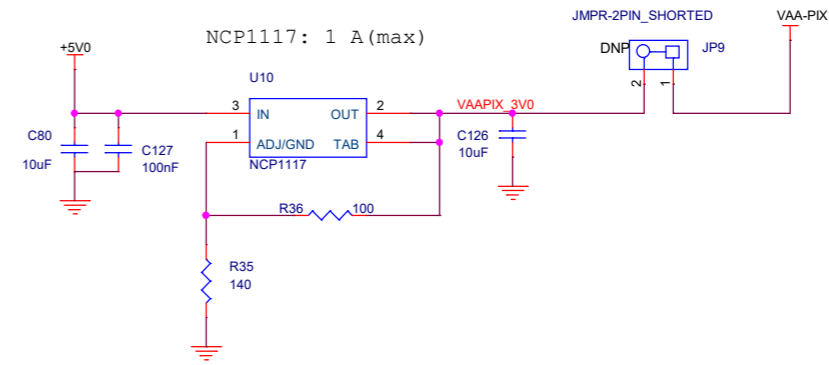
## VDDSLVSPHY 0.4V SUPPLY



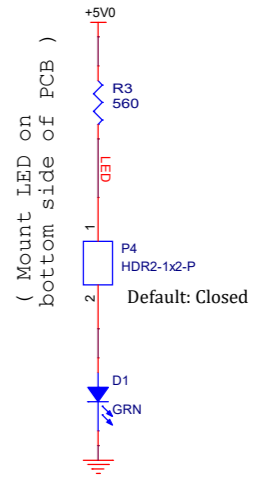
## VDD-SLVS 1.2V / 0.4V SUPPLY



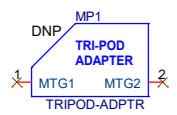
## VAAPIX 3.0V SUPPLY



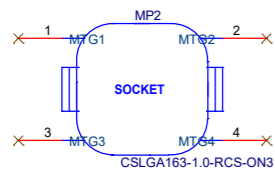
## 5V LED



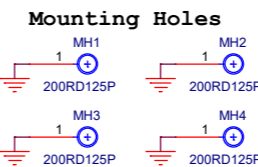
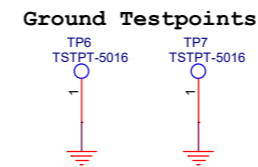
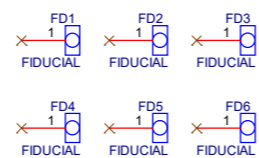
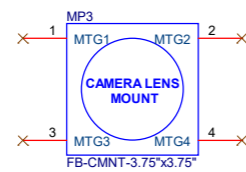
## Tripod Mount



## Socket



## Lens Mount



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Title: Power

Document Name: XGS 5000\_ILGA163\_SER\_FBD\_HEAD

Date: Friday, April 16, 2021

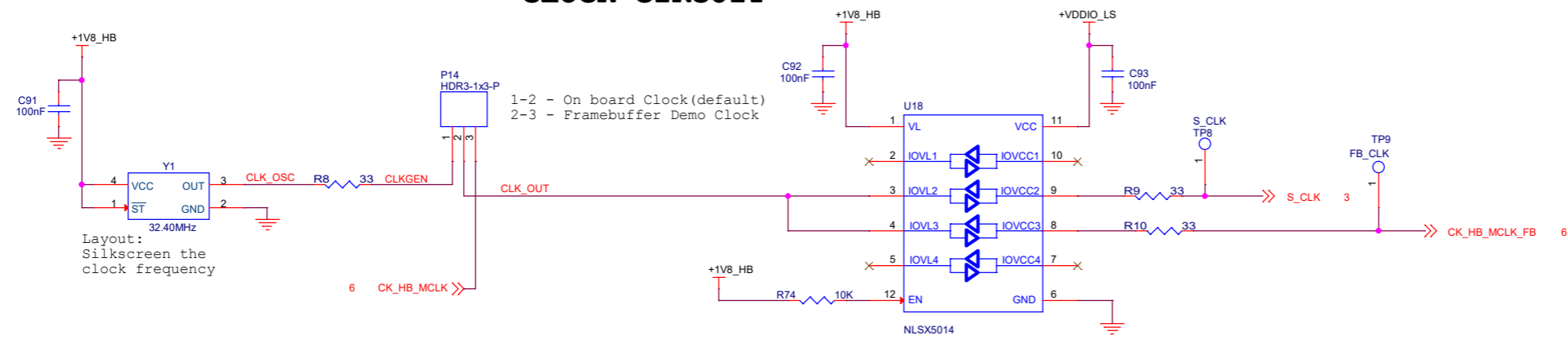
Rev: 1.0

Sheet: 4 of 6

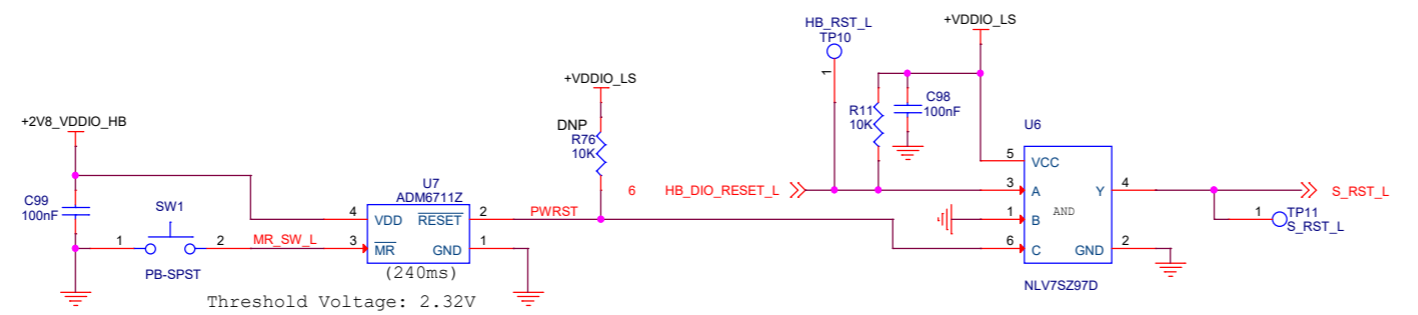
# Clock and Reset

+5V0 4  
+3V3 4  
+VDDIO\_LS 3,4,6

## CLOCK CIRCUIT



## RESET CIRCUIT



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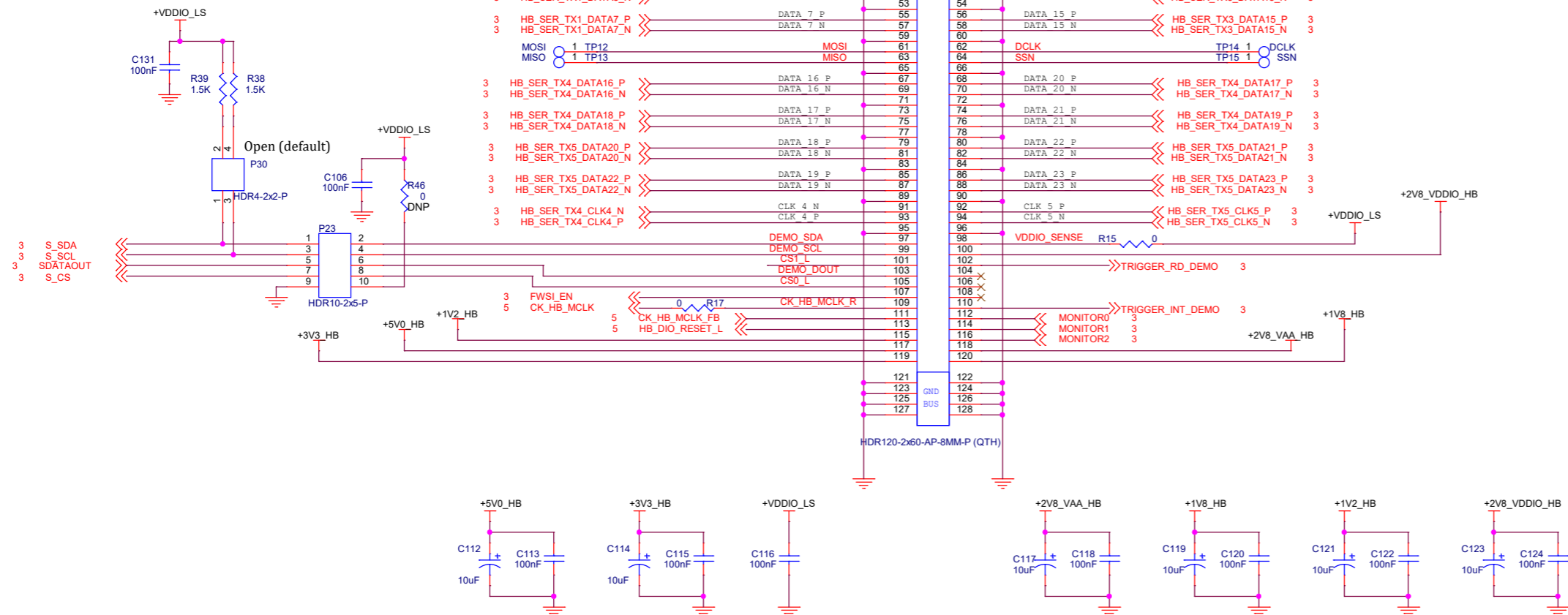
Title Clock and Reset		
Size C	Document Name XGS 5000_ILGA163_SER_FBD_HEAD	Rev 1.0
Date: Friday, March 05, 2021	Sheet 5	of 6

# External Interface

+5V0_HB	4	+5V0_HB	4
+3V3_HB	4	+3V3_HB	4
+2V8_VAA_HB	4	+2V8_VAA_HB	4
+2V8_VDDIO_HB	4,5	+2V8_VDDIO_HB	4,5
+1V8_HB	4	+1V8_HB	4
+1V2_HB	4	+1V2_HB	4
+3V3_VDDIO_LS	4	+3V3_VDDIO_LS	4
		+3V3_VDDIO_LS	3,4,5

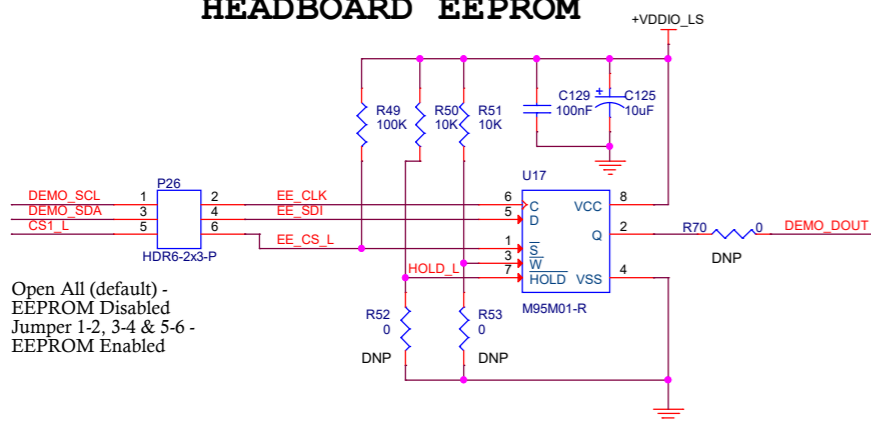
## I2C / 4-WIRE DEBUG HEADER

P23  
 Jumper 1-2, 3-4, 5-6 & 7-8 (default) - 4-WIRE Enabled  
 Jumper 1-2, 3-4 & 7-9 - I2C Enabled  
 Open All & Connect to external debugger - Test purpose



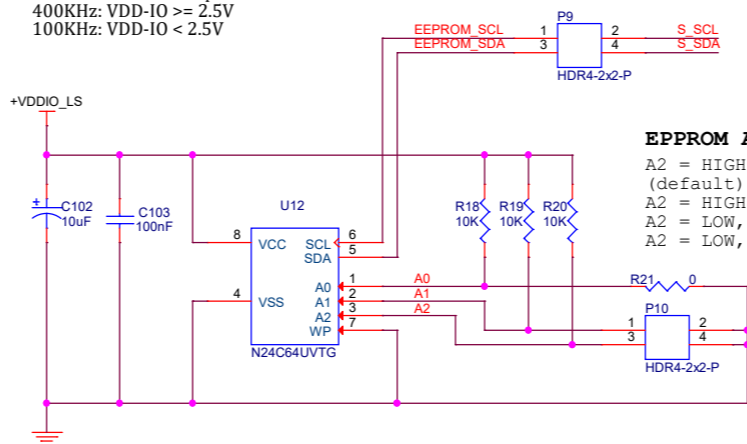
## LENS CORRECTION EEPROM

### HEADBOARD EEPROM



NOTE: EEPROM I2C speed:  
 400KHz: VDD-IO >= 2.5V  
 100KHz: VDD-IO < 2.5V

Jumper 1-2 & 3-4 (default) - I2C EEPROM Enabled  
 Open All - I2C EEPROM Disabled



### EEPROM Address Switch Settings (P10):

- A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
- A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xAC
- A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4
- A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0

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Title: External Interface

Size	Document Name	Rev
C	XGS 5000_ILGA163_SER_FBD_HEAD	1.0

Date: Friday, March 05, 2021 Sheet 6 of 6