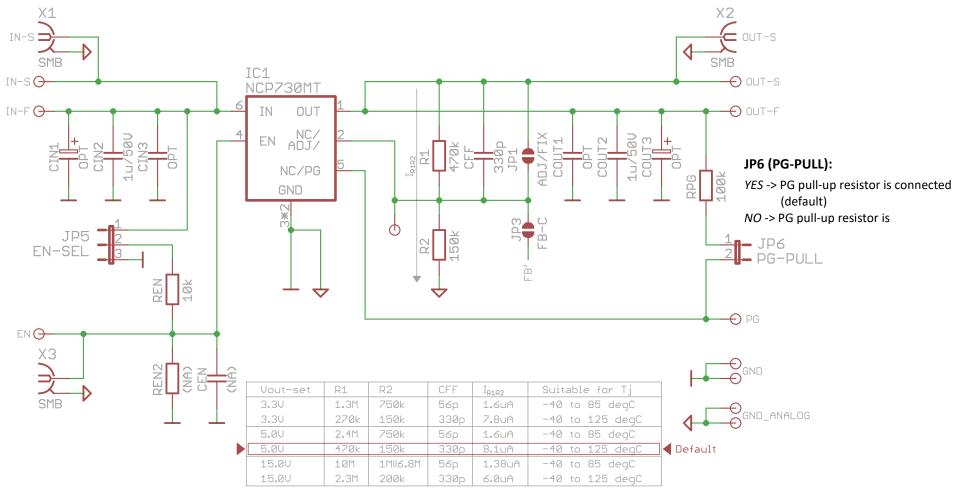
ON Semiconductor[®]

NCV8730BMTWADJTBGEVB (DFN-6) Evaluation Board – Schematic

Main part



JP1 (ADJ/FIX):

Leave this jumper open all the times (for ADJ and FIX versions as well). Could be used (shorted) for testing of ADJ version without R_1 and R_2 (V_{OUT} =1.2V) only.

JP3 (FB-C):

Open -> ADJ/PG pin not connected to PCB edge connector (default) *Short* -> ADJ/PG pin connected to PCB edge connector

JP5 (EN-SEL):

1 - 2 -> LDO is enabled (default)
2 - 3 -> LDO is disabled
NO -> LDO is controlled by externa EN signal

R_1 , R_2 , C_{FF} :

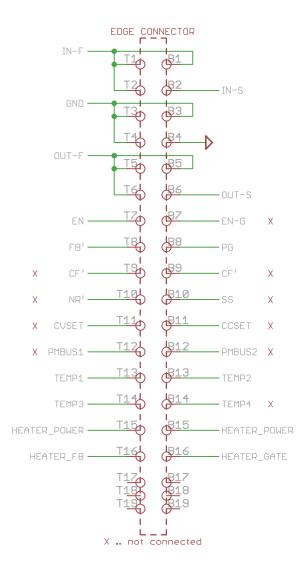
ADJ non-PG or PG versions (pin-2 = ADJ): Use R₁, R₂ and C_{FF} from the table above to set V_{OUT} voltage to desired level. For more information see datasheet. FIX non-PG or PG versions (pin-2 = NC): Remove R₁, R₂ (and C_{FF}) from PCB as they have no functionality, R₁ and R₂ just consumes current I_{R1R2}.





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PCB edge connector (optional test I/F)



Appropriate receptacle type is SAMTEC MECF-20-01-L-DV-WT