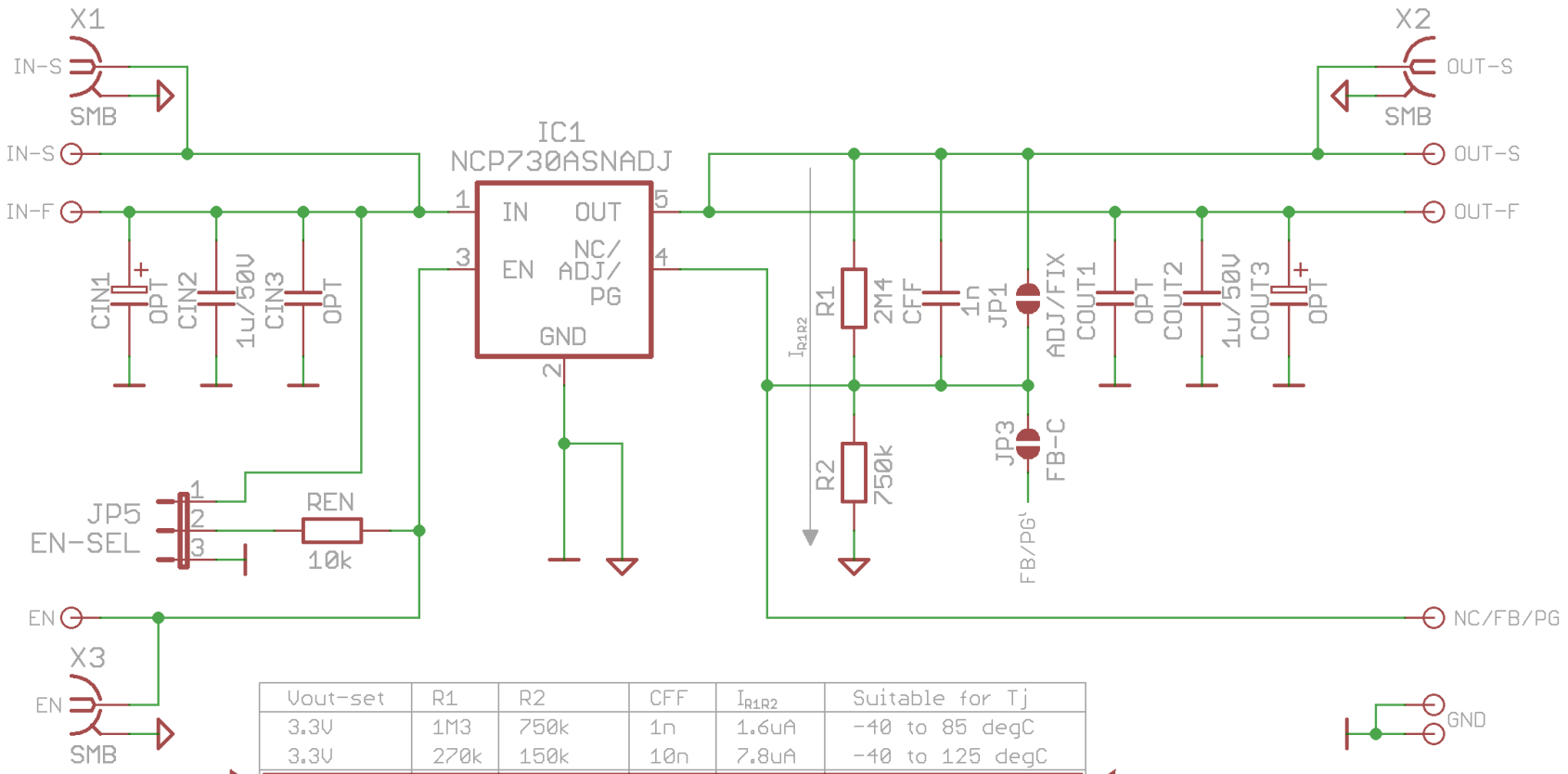
NCP730ASNADJT1GEVB (TSOP-5) Evaluation Board – Schematic

Main part



Vout-set	R1	R2	CFF	I_{R1R2}	Suitable for Tj
3.3V	1M3	750k	1n	1.6uA	-40 to 85 degC
3.3V	270k	150k	10n	7.8uA	-40 to 125 degC
5.0V	2M4	750k	1n	1.6uA	-40 to 85 degC
5.0V	470k	150k	10n	8.1uA	-40 to 125 degC
15.0V	10M	1M||6M8	1n	1.38uA	-40 to 85 degC
15.0V	2M2	200k||4M7	10n	6.0uA	-40 to 125 degC

Default

JP1 (ADJ/FIX):

Leave this jumper open all the times (for ADJ and FIX versions as well). Could be used (shorted) for testing of ADJ version without R_1 and R_2 (V_{OUT}=1.2V) only.

JP3 (FB-C):

Open -> ADJ/PG pin not connected to PCB edge connector (default)
Short -> ADJ/PG pin connected to PCB edge connector

JP5 (EN-SEL):

1 – 2 -> LDO is enabled (default)
2 – 3 -> LDO is disabled
NO -> LDO is controlled by externa EN signal

R_1, R_2, C_{FF}:

ADJ version (pin-4 = ADJ): Use R_1, R_2 and C_{FF} from the table above to set V_{OUT} voltage to desired level. For more information see datasheet.

FIX non-PG version (pin-4 = NC): Remove R_1, R_2 (and C_{FF}) from PCB as they have no functionality, R1 and R2 just consumes current I_{R1R2}.

FIX PG version (pin-4 = PG): Use R_1 as a PG pull-up resistor (100 kOhm for example) to OUT, remove R_2 and C_{FF}.

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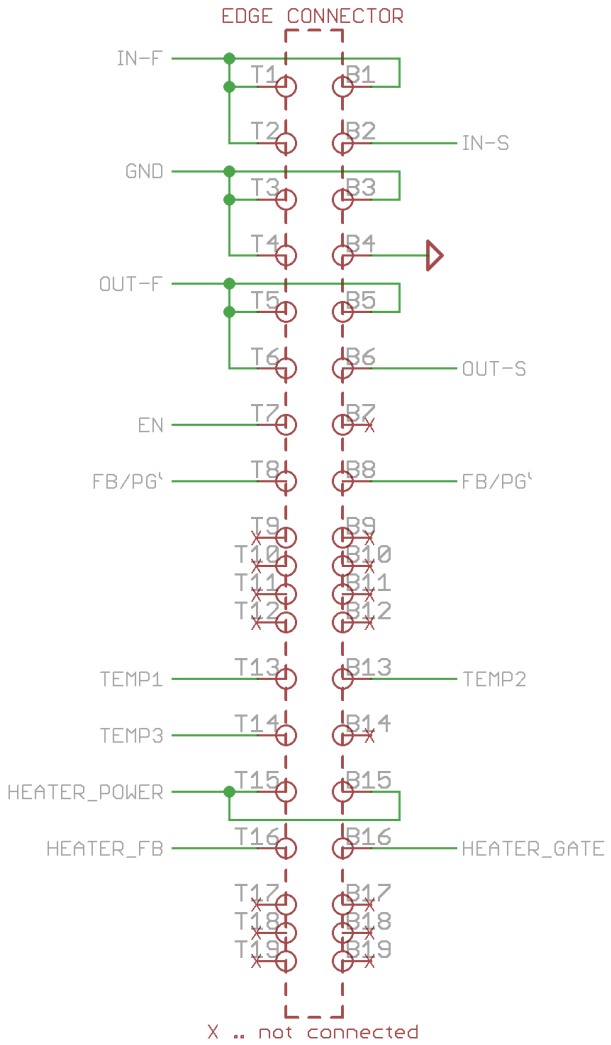
PCB edge connector (optional test I/F)



Appropriate receptacle type is SAMTEC MECF−20−01−L−DV−WT