AR0234_CSP83_Demo3Head

Rev	Who	Date	Description
Rev 0.0	aralex	02/16/18	Reused AR0234 iBGA76 schematic design and placed CSP sensor
Rev 0.1	aralex	02/19/18	Replaced C102, C103, C118, C121, C142, C124, C125, C145, C174, C154 from tantalum type to MLCC type
	aralex	02/20/18	Updated with Joe's and Sanjeev's review feedback
	aralex	03/02/18	Added net alias for U1.3 CSP socket added for AR0234 Sensor
Rev 0.2	aralex	03/09/18	Decaps C170-C173 part updated with modified part from library. Only BOM change, no electrical change
	aralex	03/19/18	Added default jumper position for P15. No electrical change, only aesthetic
Rev 0.3	aralex	06/20/18	Corrected default position of P48 Header to 'Open'. No electrical change
Rev 1.0	aralex	09/03/18	Deleted JP7, JP8 and added P51, P52; Added adjustable on-board supply for VDD, VDD-PHY Changed C177 to 10nF ; updated block diagram on Page 2
	skumar	07/17/19	Updated block diagram for SHUTDOWN signal to be active high and changed the default position of P23 to 2-3 from open
		16APR20	Updated block diagram to update slave address of sensor to 0x20(Default)/0x30

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Title: Title Page		
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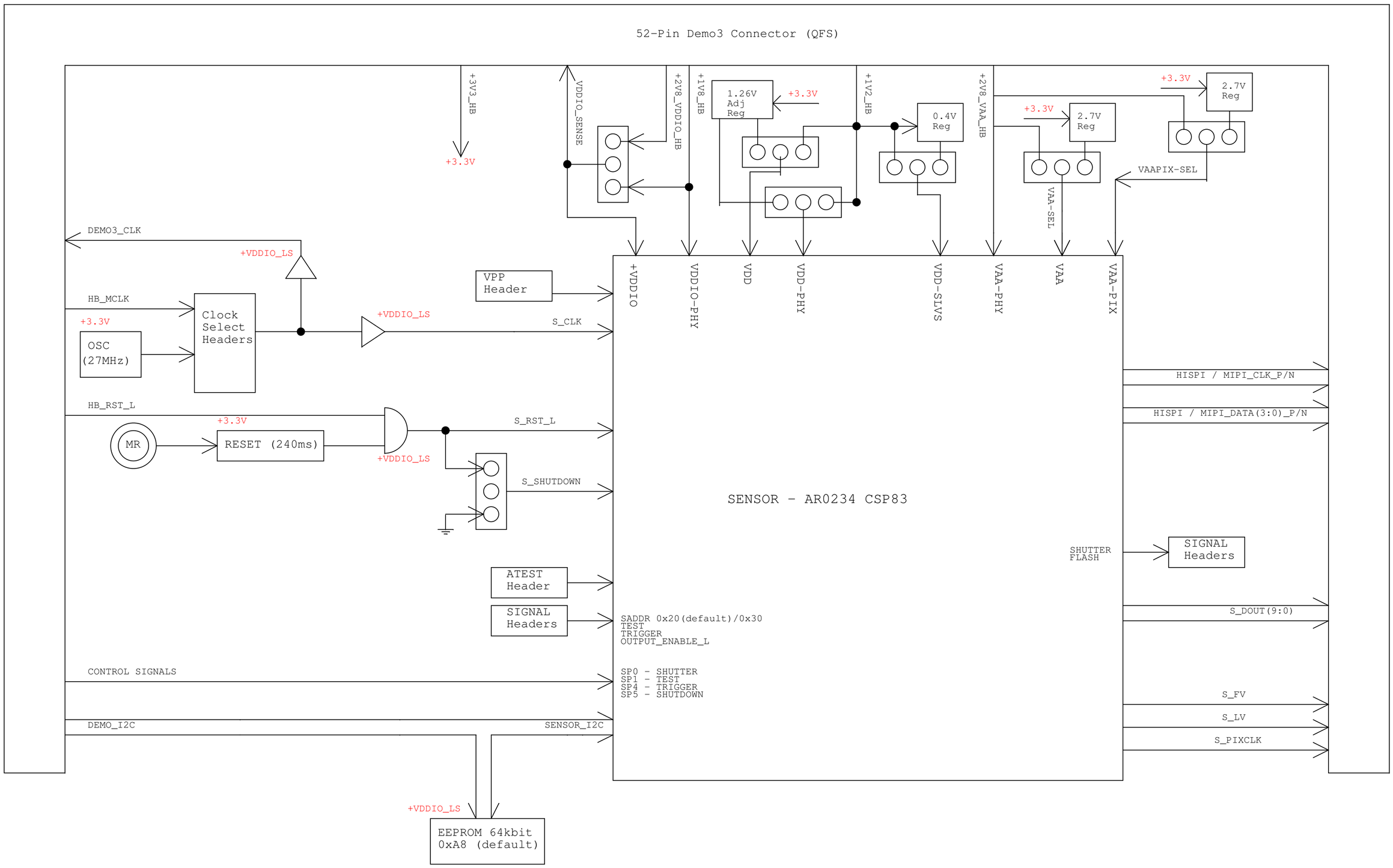
Script executed

Block Diagram



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Title	Block Diagram	
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AR0234_CSP83

+5V0 4
+3V3 4,5
+VDDIO_LS 4,5,6

VDD 4
VDD-PHY 4
VDD-SLVS 4
VDD-IO 4
VDDIO-PHY 4
VAA 4
VAA-PIX 4
VAA-PHY 4

TEST
+VDDIO_LS R85 10K Default: Close
P41 2 1 HDR2-1x2-P S_TEST

OUTPUT_ENABLE_L
+VDDIO_LS R86 10K Default: Close
P42 2 1 HDR2-1x2-P S_OUTPUT_ENABLE_L

SHUTTER
P43 HDR3-1x3-P 1 2 3 +VDDIO_LS R96 10K S_SHUTTER Default: Open

TRIGGER
+VDDIO_LS R88 10K DNP Default: Open
6 S_TRIGGER
R97 10K DNP
P44 2 1 HDR2-1x2-P TRIGGER

SADDR
+VDDIO_LS R89 10K Default: Close
P45 2 1 HDR2-1x2-P S_SADDR

FLASH
+5V0 +3V3
C14 100nF R94 0 R95 0 DNP C15 100nF
P47 HDR4-1x4-P 1 2 3 4 S_FLASH Default: Open

ATEST1
P48 2 1 HDR2-1x2-P S_ATEST1
C101 DNP 100nF
Default: Open

U9-1
AR0234-DEMO_CSP83

5	S_CLK	G11	EXTCLK	PIXCLK	C6 PIXCLK
				FRAME_VALID	B7 FV
				LINE_VALID	C7 LV
6	S_TEST	F5	TEST		
6	S_SCL	F6	SCL	DOUT0	F3 DATA0
6	S_SDA	E6	SDA	DOUT1	G4 DATA1
				DOUT2	G5 DATA2
	S_ATEST1	A11	ATEST	DOUT3	E3 DATA3
				DOUT4	D1 DATA4
	S_SADDR	A5	SADDR	DOUT5	D2 DATA5
				DOUT6	B3 DATA6
	TRIGGER	D5	TRIGGER	DOUT7	E4 DATA7
				DOUT8	D4 DATA8
				DOUT9	C4 DATA9
	S_OUTPUT_ENABLE_L	B6	OUTPUT_EN_N		
				SLVSCP	D11 H_M_CLK_P
				SLVSCN	D12 H_M_CLK_N
5	S_RST_L	F7	RESET_N	SLVS0P	C9 H_M_DATA0_P
				SLVS0N	C10 H_M_DATA0_N
5,6	S_SHUTDOWN_L	F10	SHUTDOWN	SLVS1P	C12 H_M_DATA1_P
				SLVS1N	C11 H_M_DATA1_N
				SLVS2P	E9 H_M_DATA2_P
		F12	CAP_1UF_PHY	SLVS2N	E10 H_M_DATA2_N
				SLVS3P	E11 H_M_DATA3_P
				SLVS3N	E12 H_M_DATA3_N
				FLASH	E5 S_FLASH
				SHUTTER	F4 S_SHUTTER 6

AR0234 CSP83 DEMO

C169 1uF

U9-2
AR0234-DEMO_CSP83

VAA					
VAA-PIX		A10	VAA2V8_0	AGND0	A9
		B1	VAA2V8_1	AGND1	C3
		G2	VAA2V8_2	AGND2	G3
		G7	VAA2V8_3	AGND3	G6
		B8	VAAPIX_0		
		C2	VAAPIX_1		
VAA-PHY		G1	VAAPIX_2		
		G9	VAAPIX_3		
VDD-IO		F8	VAA2V8_PHY	DGND0	A2
				DGND1	A3
		B4	VDDIO2V8R1V8_0	DGND2	A6
		B5	VDDIO2V8R1V8_1	DGND3	B2
		D6	VDDIO2V8R1V8_2	DGND4	C1
		A7	VDDIO2V8R1V8_3	DGND5	C5
		B11	VDDIO2V8R1V8_4	DGND6	D8
		D3	VDDIO2V8R1V8_5	DGND7	D9
		F1	VDDIO2V8R1V8_6	DGND8	E2
		G12	VDDIO2V8R1V8_7	DGND9	E8
				DGND10	F2
VDD	VDDIO-PHY	D10	VDDIO1V8_PHY	DGND11	F9
				DGND12	G10
		A4	DVDD1V2_0		
		A8	DVDD1V2_1		
		A12	DVDD1V2_2		
		B10	DVDD1V2_3	GNDIO_PHY_1	B12
		D7	DVDD1V2_4	GNDIO_PHY_2	E7
		E1	DVDD1V2_5		
VDD-PHY		G8	DVDD1V2_6		
		C8	DVDD1V2_PHY	VAAHV_NPIX	B9 VPP0
VDD-SLVS		F11	DVDD_SLVS_PHY		

AR0234 CSP82 DEMO

(Note for layout: - Place these testpads near the Demo3 I/F connector at the top side of PCB)

ZTP1 ZTP2 ZTP3 ZTP4 ZTP5 TESTPAD-2IF-TIP

H_M_CLK_P 6
H_M_CLK_N 6
H_M_DATA0_P 6
H_M_DATA0_N 6
H_M_DATA1_P 6
H_M_DATA1_N 6
H_M_DATA2_P 6
H_M_DATA2_N 6
H_M_DATA3_P 6
H_M_DATA3_N 6

RP1 22
PIXCLK 1 2 FV 3 LV 4 8 7 6 5
S_PIXCLK 6
S_FV 6
S_LV 6
TP1 S_LV
TP2 S_FV
TP3 S_PIX

RP2 22
DATA0 1 DATA1 2 DATA2 3 DATA3 4 8 7 6 5
TP4 S_D0
TP5 S_D1
S_DATA0 6
S_DATA1 6
S_DATA2 6
S_DATA3 6

RP3 22
DATA4 1 DATA5 2 DATA6 3 DATA7 4 8 7 6 5
S_DATA4 6
S_DATA5 6
S_DATA6 6
S_DATA7 6

RP4 22
DATA8 1 DATA9 2 3 4 8 7 6 5
S_DATA8 6
S_DATA9 6

+2V8_VAA_HB
R2 10K
P3 HDR3-1x3-P 1 2 3 DNP VPP0
C9 1uF
Jumper open = Normal Operation(Default)

VDD: C102 10uF; C103 10uF; C104 C105 C106 C107 C108 C109 C110 100nF
VDD-PHY: C118 10uF; C119 100nF
VDD-SLVS: C121 10uF; C122 100nF
VDDIO-PHY: C142 10uF; C143 100nF
VDD-IO: C124 10uF; C125 10uF; C126 C127 C128 C129 C130 C131 C132 100nF
VAA: C145 10uF; C150 C151 C152 C153 100nF
VAA-PHY: C174 10uF; C175 100nF
VAA-PIX: C154 10uF; C156 C158 C160 C176 100nF

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Title	Sensor		
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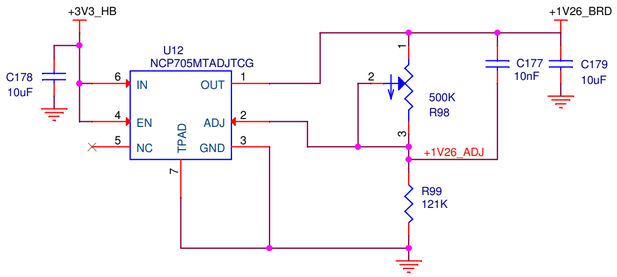
Debug Headers: Cut away the shorted trace
and mount header for power debugging

Power

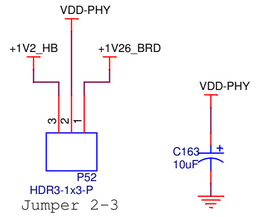
*Note: * Pls take care to load the jumpers on P51 and P52 the same way, ie. either both are 2-3 or both 1-2*

Adjustable On-board Supply for VDD, VDD-PHY

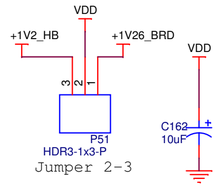


*Note: * Pls UNMOUNT Jumpers on P51 and P52. Adjust the R98 to set U12 Regulator voltage to 1.26V. THEN ONLY mount jumpers on P51 and P52 **

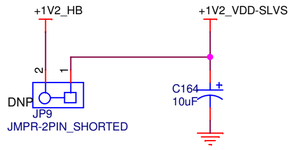
VDD-PHY 1.2V SUPPLY



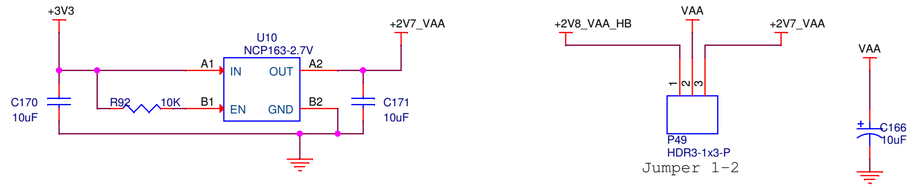
VDD 1.2V SUPPLY



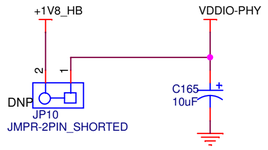
VDD-SLVS 1.2V SUPPLY



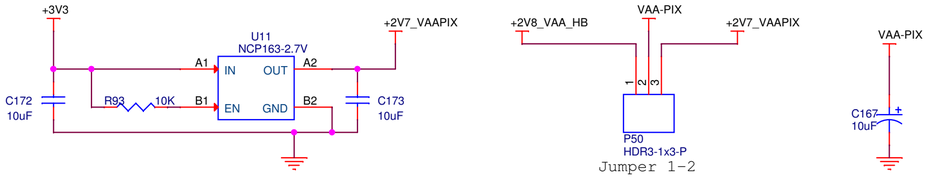
VAA 2.8V SUPPLY



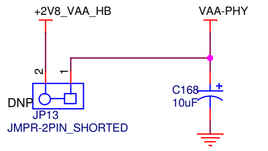
VDDIO-PHY 1.8V SUPPLY



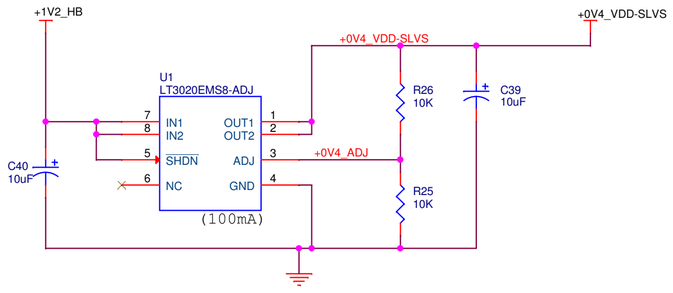
VAA-PIX 2.8V SUPPLY

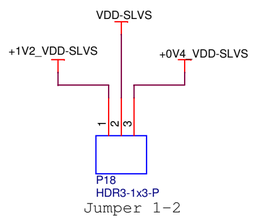


VAA-PHY 2.8V SUPPLY



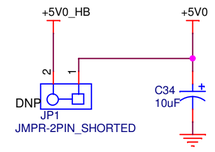
VDDSLVSPHY 0.4V SUPPLY



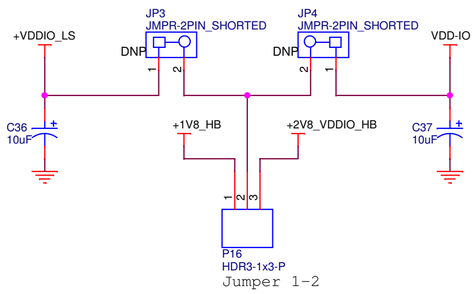


Selection of 0.4V or 1.2V for VDDSLVSPHY supply

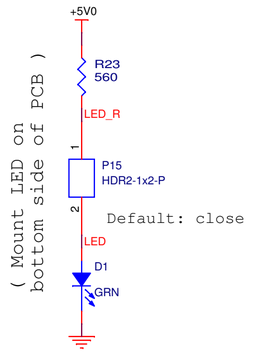
PERIPHERAL 3.3V SUPPLY

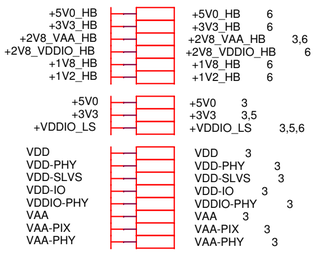


VDDIO & VDDIO_LS 1.8V/2.8V SUPPLY

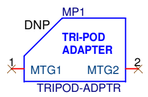


5V LED

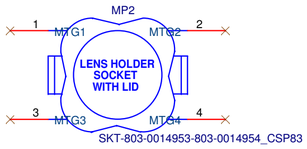


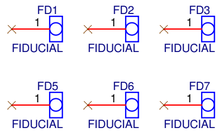


Tripod Mount

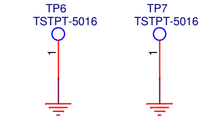


Socket/Lens Mount

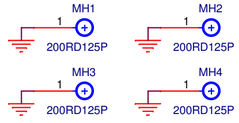




Ground Testpoints



Mounting Holes



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Title	Power	
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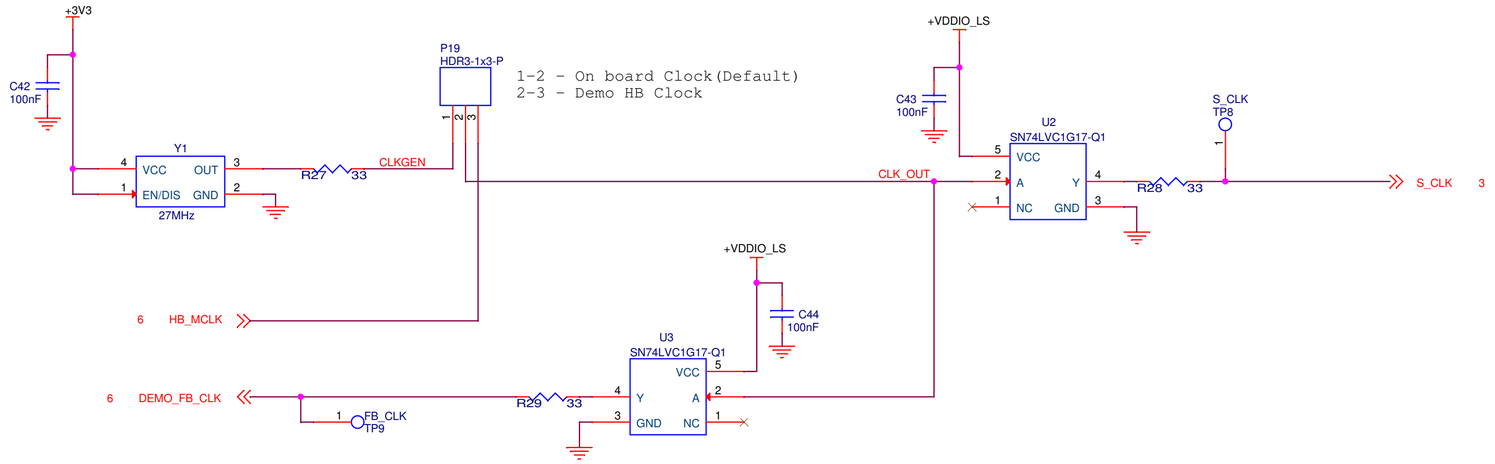
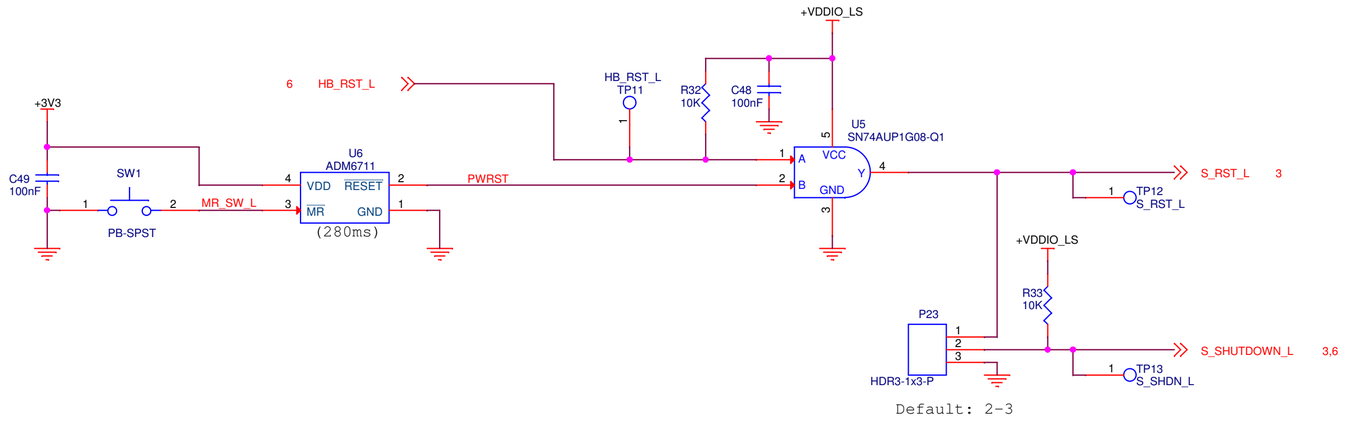
Clock and Reset

+5V0 +5V0 3,4
+3V3 +3V3 3,4
+VDDIO_LS +VDDIO_LS 3,4,6

CLOCK CIRCUIT



RESET CIRCUIT



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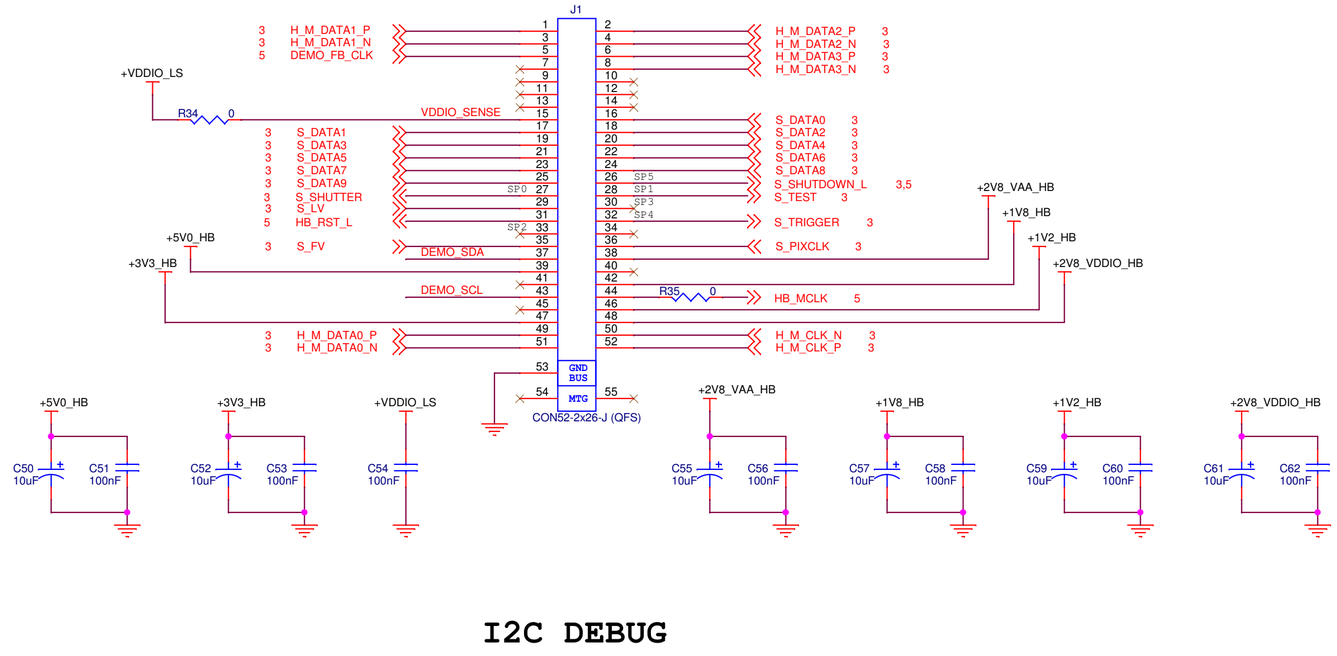
Title: Clock and Reset		
Size: C	Document Name: AR0234-CSP83_Demo3Head	Rev: 1.0
Date: Wednesday, July 17, 2019	Sheet 5 of 6	

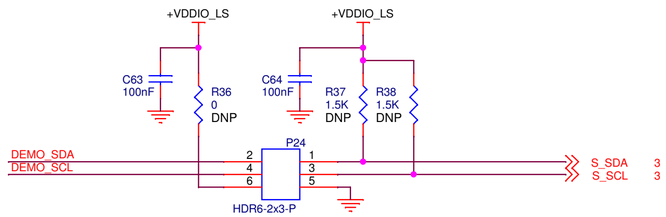
External Interface

+5V0_HB, +3V3_HB, +2V8_VAA_HB, +2V8_VDDIO_HB, +1V8_HB, +1V2_HB
+3V3, +VDDIO_LS

DEMO3 BASEBOARD I/F



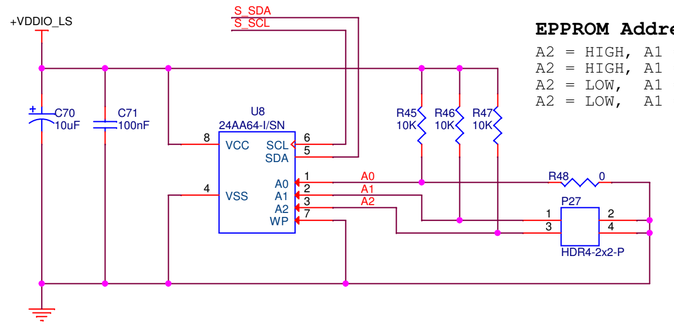
I2C DEBUG



Jumper 1-2 & 3-4

LENS CORRECTION EEPROM

NOTE: EEPROM I2C speed:
400KHz: VDD-IO >= 2.5V
100KHz: VDD-IO < 2.5V



EPPROM Address Switch Settings:

A2 = HIGH, A1 = LOW, A0 = LOW; Address => 0xA8 (default)
A2 = HIGH, A1 = HIGH, A0 = LOW; Address => 0xAC
A2 = LOW, A1 = HIGH, A0 = LOW; Address => 0xA4
A2 = LOW, A1 = LOW, A0 = LOW; Address => 0xA0

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Title: External Interface		
Size: C	Document Name: AR0234-CSP83_Demo3Head	Rev: 1.0
Date: Tuesday, September 04, 2018	Sheet 6 of 6	

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