

FAN4910x Evaluation Board User Guide TinyPower™ Buck Boost Regulator

UM70112/D

DESCRIPTION

The FAN4910X evaluation board is a compact circuit for evaluating **onsemi**'s FAN4910X family of Buck–Boost regulators in a 20-bump Wafer–Level Chip–Scale Package (WLCSP).

The FAN49101 and FAN49103 IC versions include a programmable I^2C interface and the FAN49100 version is a stand–alone IC with MODE (forced PWM or Auto Mode) and PT (forced pass–thru) feature pins. Please visit **onsemi**'s website at https://www.onsemi.com for additional details on these products.

The board also features footprints to accommodate additional input/output capacitors and probe access points to all key circuit nodes so that electrical characteristics can be measured.

Features

- Input Voltage Range: 2.5 V to 5.5 V
- Programmable Output Voltage (I²C Compatible Versions only):
 - 2.5 to 2.8 V in 0.05 V Steps
 - 2.8 to 4.0 in 0.025 V Steps
- 1.8 MHz Fixed-Frequency Operation in PWM Mode
- Seamless Step-up and Step-down Mode Transitions
- Low Ouiescent Current
- Internal Soft-Start
- Optional Output Discharge

- Low Ripple
- Excellent Transient Response
- Safety Protections (UVLO, OTP, SCP, OCP)
- Package: 20 Bump, 0.4 mm pitch WLCSP

Quick Start Connection Guide

- 1. Connect input power supply (3.6 V typical with 2.5 V-5.5 V range) between banana jacks VIN and GND as shown in Figure 1 (labeled Input).
- 2. FAN49101 & FAN49103 Versions:
 Remove jumper from the EN header to
 enable/disable the IC from the GUI. Or set EN to
 (–) when operating the IC in standalone mode
 (without the GUI).
 FAN49100 Versions:
 - Set the EN header to (-) and set the PT and MODE pins to the desired position. Go to Step 5.
- 3. FAN49101 & FAN49103 Versions: Connect the USB Interface POD as shown in Figure 6.
- 4. FAN49101 & FAN49103 Versions: Start up the GUI application. If not installed, refer to section *Installation*.
- 5. Connect the external load between banana jacks VOUT and GND as shown in Figure 1 (labeled Load).
- 6. Set EN to (+) to enable the IC in Softstart.

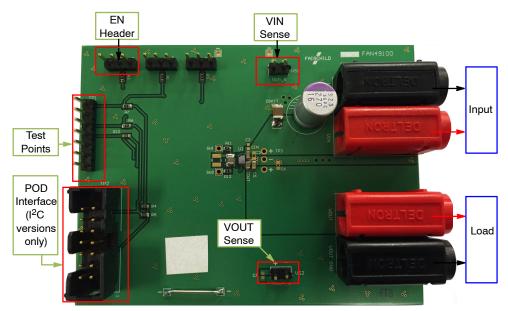


Figure 1. Evaluation Board Connection Diagram

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GUI INSTALLATION

Installation

- a. Run the installer_FAN49103.exe .
- b. Follow the steps as shown in dialog box for the setup.



Figure 2. FAN49103 GUI Installation

c. When prompted for Selecting Components, please check the box for PIC POD Driver to install appropriate drivers needed for USB Interface POD.

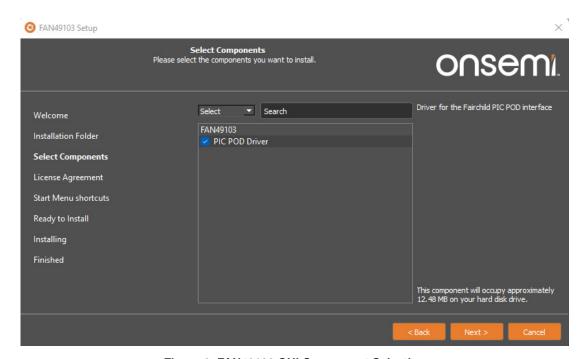


Figure 3. FAN49103 GUI Component Selection

d. Once all steps have been completed, it will start installing the GUI.

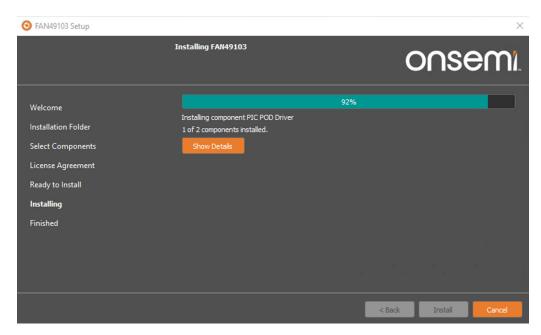


Figure 4. FAN49103 GUI Installation Update

- e. Once the installation is complete, FAN49103 GUI will open automatically
- f. You can find installed GUI at this path: C:\Users*****\onsemi\FAN49103
- g. Below is a screen shot of the FAN49103 GUI that is used to communicate via I²C:

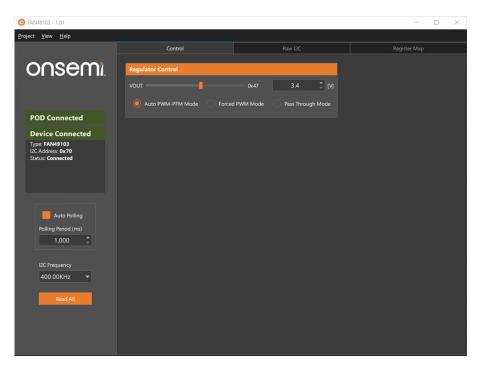


Figure 5. FAN49103 GUI Interface

GUI FEATURES

POD Connection

a. Connect provided USB Interface POD with the device under test as shown in Figure 6.

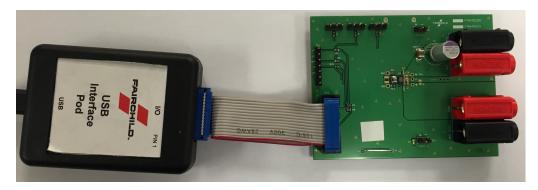


Figure 6. Connection of USB Interface POD to DUT

 b. Once the USB Interface POD is connected, it will show POD Connected on the GUI and if device is not connected it will show Device Disconnected. See Figure 7.

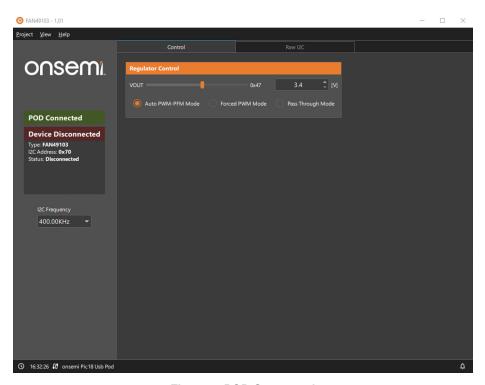


Figure 7. POD Connected

c. If POD is disconnected, it will show No POD Connection as shown in Figure 8.

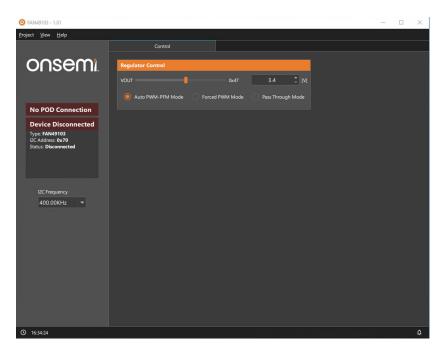


Figure 8. No POD Connection

Device Connection

When device is powered up, GUI will show Device Connected with the I²C slave address identified. Auto Polling is on by default at power on; GUI will poll the

registers automatically with Polling Period specified. If Auto Polling disabled, Read All button can be used to read registers & update the GUI anytime.

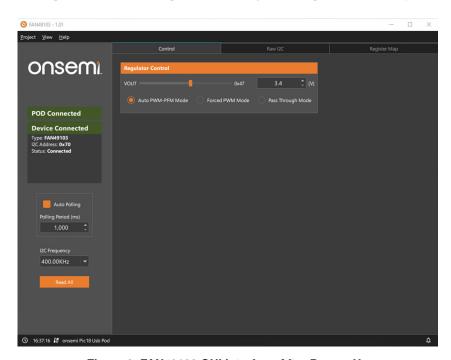


Figure 9. FAN49103 GUI Interface After Power-Up

Control Panel

Control Panel consists of Regulator Control with VOUT slider which sets output voltage from 2.5 V to 4.0 V. There

are options to select either "Auto PWM-PFM Mode" or "Forced PWM Mode" or "Pass-Through Mode".

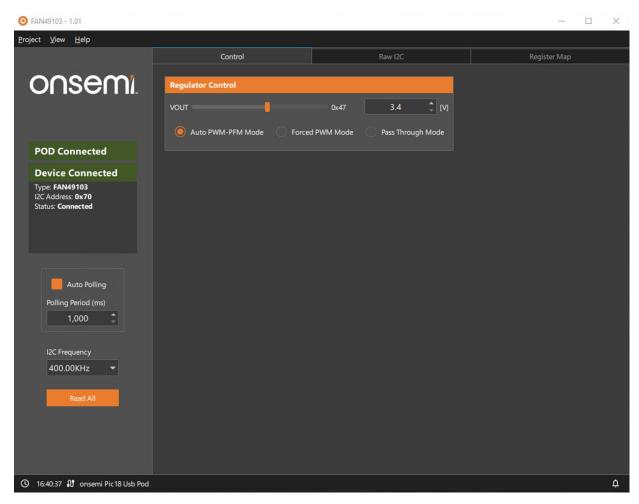


Figure 10. Control Panel

Register Map Panel

- a. Register Map allows control of individual bits of each Register.
- b. *Edit Register Window:* By double clicking on each Register "Edit Register" window will pop-up. Register value can be changed from this window.

Discard Changes: This option will revert the changes made by the user to the current register.

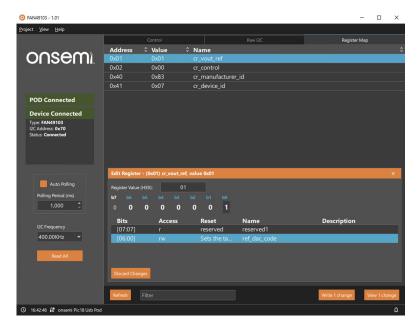


Figure 11. Edit Register Window

c. Write # changes: This option will write all registers changed from the previous settings.

View # changes: This option will allow user to see what changes has been made from the last set of register settings and then write all changes together. Example of View changes Window is shown in Figure 12.



Figure 12. View Changes Window

Raw I²C Panel

a. FAN49103 GUI allow user to write to or read from the known Slave Address with Hex values of data & Register info.

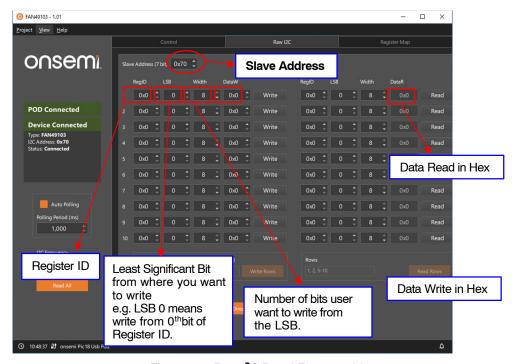


Figure 13. Raw I²C Panel Features (a)

b. GUI has features to select I²C Clock Frequency, write/read registers sequentially, and save/load complete settings to/from .json file.

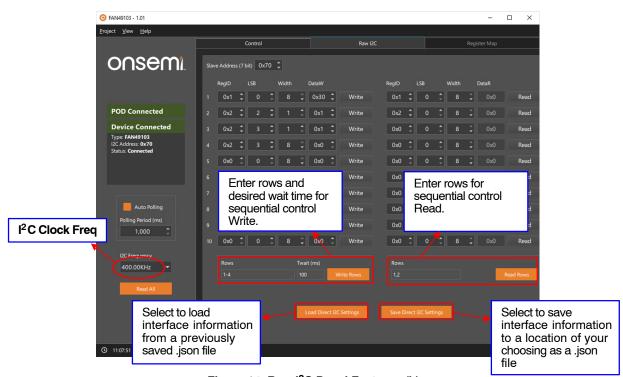


Figure 14. Raw I²C Panel Features (b)

 c. Communication Error: If Slave-Address is not correct or communication with respective Slave Address fails it will give error on Write or Read as in Figure 15, please make sure correct Slave Address is provided and try again.

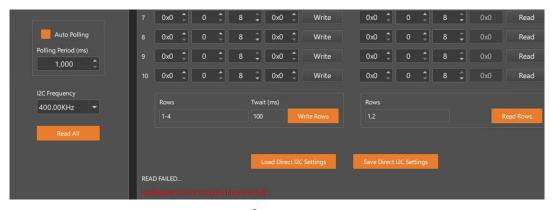


Figure 15. Raw I²C Communication Error

Support

- a. *Windows:* FAN49103 GUI is supported by Windows 10 & 11 Platforms.
- b. Datasheet: Navigate to Help → Datasheet for more information on the device and register information.

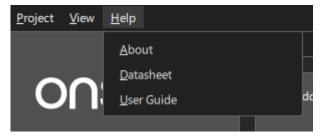


Figure 16. Help on FAN49103 GUI

- c. User Guide: Navigate to Help → User Guide for more information on the GUI.
- d. Log & Communications Log: User can view all communication made to & from IC in Communication log from View → Comms Log.

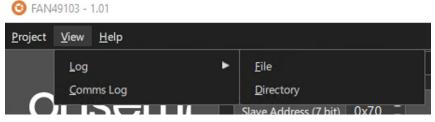


Figure 17. Communication Log

e. Save/Open Configuration: User can save their configuration of Control Panel to a .cfg file and

open the configuration later with the saved .cfg file to retrieve same control panel settings.

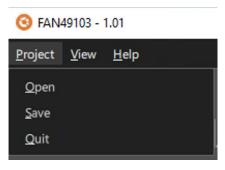


Figure 18. Save/Open Configuration

SCHEMATIC

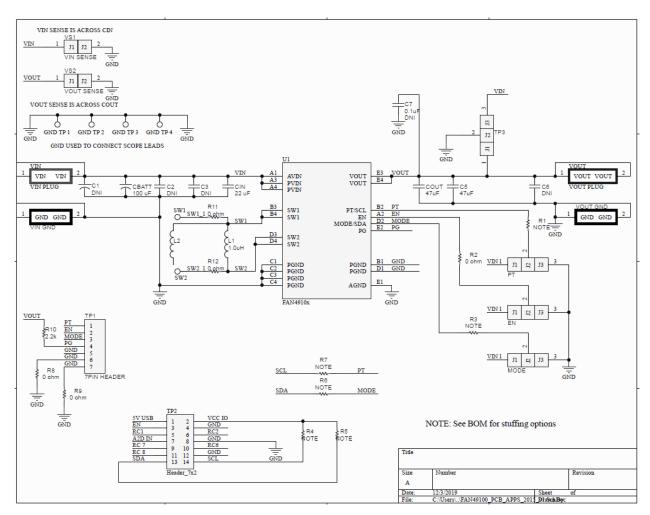


Figure 19. Evaluation Board Schematic

BILL OF MATERIALS

Table 1. BOM

FAN49101 & FAN49103 BOM					
Ref	Qty	Description	Manufacturer		
U1	1	IC, Buck-Boost, WLCSP20	onsemi FAN4910x		
L1	1	1.0 μH , 4.2 Asat, 36 m Ω , 20%, 2016, 1 mm height	Cyntec HTEH20161T-1ROMSR		
CIN	1	22 μF, 6.3 V, 0603 (1608 METRIC)	Murata GRM187R61A226ME15		
COUT, C5	2	47 μF, 6.3 V, 0603 (1608 METRIC)	Murata GRM188R60J476ME15		
CBATT	1	I00 μF, 10 V, 20%, X5R, 1210	Samsung CL32A107MPVNNNE		
R2, R6, R7, R8, R9, R11, R12	7	0 Ω, 0603			
R4, R5, R10	3	2.2 kΩ, 0603			
EN	1	3x1 Header Strip, 125C	DigiKey SAM1098-03		
VS1,VS2	2	2x1 Header Strip, 125C	DigiKey S1011E-02-ND		
TP1	1	7x1 Header strip, 125C			
TP2	1	7x2 Header strip, 125C	DigiKey SAM1094-07		
VOUT, VIN	2	Banana Jack, Red	Delton 571-0500		
			Mouser 164-6219		
GND, GND	2	Banana Jack, Black	Delton 571-0100		
			Mouser 164–6218		
GND	1	Bus Bar			
C1, C2, C3, C6, C7, TP3, PT, MODE, R3, R1	DNI				

FAN49100 BOM				
Ref	Qty	Description	Manufacturer	
U1	1	IC, Buck-Boost, WLCSP20	onsemi FAN4910x	
L1	1	1.0 μH , 4.2 Asat, 36 m Ω , 20%, 2016, 1 mm height	Cyntec HTEH20161T-1ROMSR	
CIN	1	22 μF, 6.3 V, 0603 (1608 METRIC)	Murata GRM187R61A226ME15	
COUT, C5	2	47 μF, 6.3 V, 0603 (1608 METRIC)	Murata GRM188R60J476ME15	
CBATT	1	100 μF, 10 V, 20%, X5R, 1210	Samsung CL32A107MPVNNNE	
RI, R2, R3, R8, R9, R11, R12	7	0 Ω, 0603		
R10	1	2.2 kΩ, 0603		
PT, EN, MODE	3	3x1 Header Strip, 125C	DigiKey SAM1098-03	
VS1, VS2	2	2x1 Header Strip, 125C	DigiKey S1011E-02-ND	
TP1	1	7x1 Header strip, 125C		
VOUT, VIN	2	Banana Jack, Red	Delton 571-0500	
			Mouser 164–6219	
GND, GND	2	Banana Jack, Black	Delton 571-0100	
			Mouser 164-6218	
GND	1	Bus Bar		
C1, C2, C3, C6, C7, TP3, TP2, R4, R5, R6, R7	DNI			

PRINTED CIRCUIT BOARD

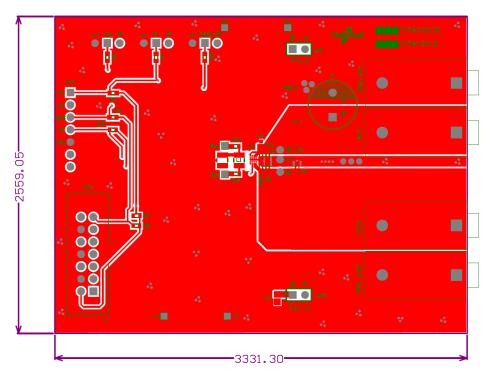


Figure 20. Top Layer

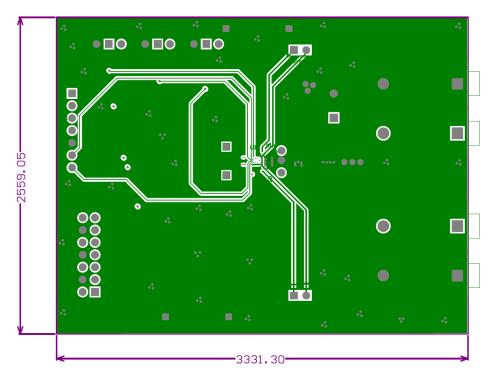


Figure 21. Mid-Layer 1

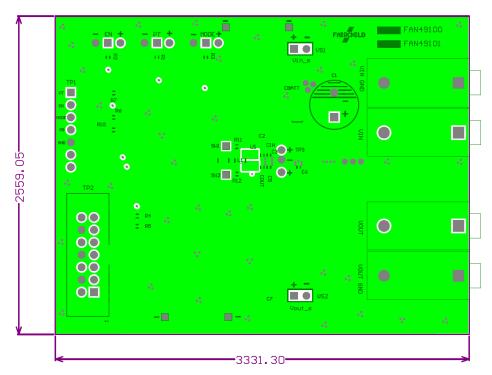


Figure 22. Mid-Layer 2

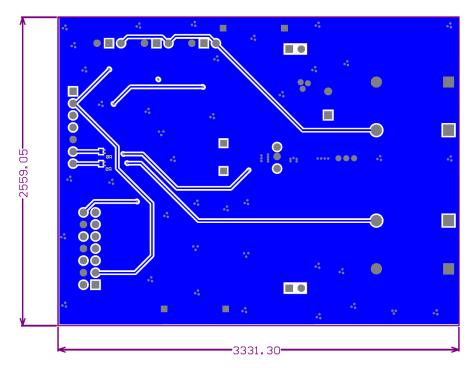


Figure 23. Bottom Layer

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