FAD1110 Evaluation Board User's Manual

EVBUM2952/D

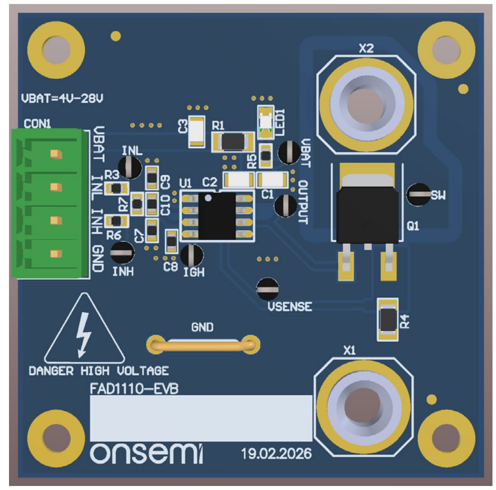

Figure 1. FAD1110EVB Board Picture

Introduction

The FAD1110-F085 is a highly integrated ignition gate driver IC designed for direct control of an automotive ignition IGBT in modern "coil-on-plug" and distributorless ignition systems. Using a differential input stage with built-in spike filtering, the device ensures robust triggering even in harsh environments with significant ground-shift disturbances ranging from –2 V to +3 V. The FAD1110-F085 manages the complete coil-charging cycle, providing precise current limitation through a dedicated V_SENSE input and reliable timing supervision via a programmable maximum dwell time implemented with an external capacitor on the CSSD pin.

To protect the ignition system, the device features an autonomous Hard-Shut-Down (HSD) mechanism that immediately turns off the IGBT when the dwell time exceeds the configured limit, preventing thermal overload and unintended spark events. With its optimized gate-drive output, wide operating-voltage range, and low supply current, the FAD1110-F085 offers a compact and efficient solution for automotive ignition control modules requiring high reliability, predictable timing, and strong immunity to electrical transients.

Evaluation Board Features

- 12 V Battery-Level Supply Input
- Two Supply Connectors for Flexible Powering during Evaluation
- Input Connector for the Differential Ignition Trigger Signal (INH/INL), including Spike-Filtering and Ground-Shift Tolerance from –2 V to +3 V
- Configurable Current-Limit and Current-Sense Network
- Support for Timing-based Hard-Shut-Down
- LED Indicator for Presence VBAT Voltage
- Oscilloscope Test Points on Key Signals
- Additional High-Voltage Isolation Spacing Implemented in Accordance with IPC-2221A Guidelines to Ensure Safe Handling of Ignition-level Transients
- Header for Stacking Multiple Boards or Integrating into a Larger Evaluation Setup

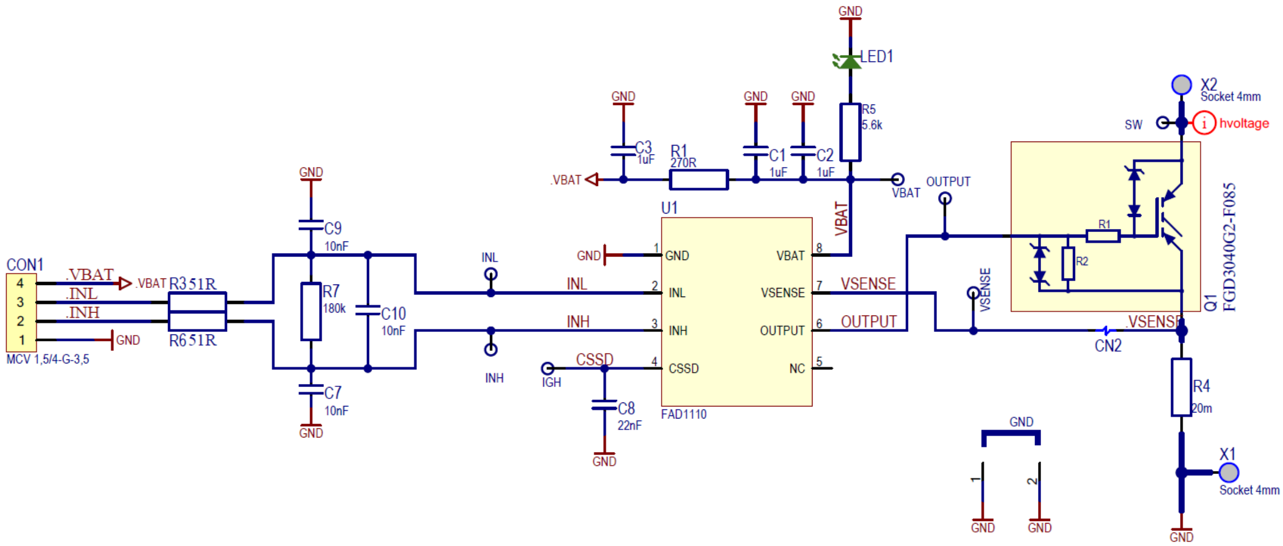

Figure 2. FAD1110 Evaluation Board Schematic

MAXIMUM RATINGS

Rating	External Pin	Min	Max	Unit
VBAT (CON1)	.VBAT	4,5	28	V
INH (CON1)	.INH	–2	18	V
INL (CON1)	.INL	–2	18	V
Collector Voltage	VBATPOWER X2	–400	400	V
Input Current	VBATPOWER X2	0	20	A
VCSSD	VCSSD	–0.3	3.6	V
VOUTPUT	VOUTPUT	–0.3	6.5	V
VSENSE	VSENSE	0	400	mV
FAD1110 Junction Temperature		–50	+150	°C
Board Temperature		–50	+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING RANGES

Rating	External Pin	Min	Max	Unit
VBAT (CON1)	.VBAT	6	16	V
INH (CON1)	.INH	0	5	V
INL (CON1)	.INL	0	5	V
VCM INH-INL (CON1)	Common voltage VCM	–2	3	V
Collector Voltage	VBATPOWER X2	–400	60	V
Input Current	VBATPOWER X2	0	internally limited	A
VCSSD	VCSSD	–0.3	3.6	V
VOUTPUT	VOUTPUT	–0.3	6.5	V
VSENSE	VSENSE	0	215	mV
FAD1110 Junction Temperature		–50	+150	°C
PCB Temperature		–40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

FUNCTIONAL DESCRIPTION

The FAD1110 evaluation board provides a compact and complete platform for demonstrating the operation of the FAD1110 ignition gate driver IC. It integrates the driver together with an ignition IGBT and all essential application circuitry required to evaluate ignition-coil charging, programmable dwell-time control, current-limit behavior, and the device's built-in diagnostic and protection features. The board allows users to observe the FAD1110's timing-supervision mechanism, including the programmable maximum dwell period set by the external CSSD capacitor and the device's Hard-Shut-Down (HSD) response, which immediately disables the IGBT when the dwell limit is exceeded to prevent overheating and unintended spark events.

To ensure reliable operation under ignition-level transient conditions, the PCB incorporates enhanced high-voltage isolation spacing designed according to IPC-2221A guidelines. The platform provides safe access to key measurement points – such as the differential input pins, the gate-drive output, the V_SENSE current-limit node, and the CSSD timing pin – enabling efficient evaluation of the FAD1110 under realistic automotive ignition conditions.

Supply Strategy

The power supply architecture is divided into three main paths:

- **VBAT (CON1)** – Main supply input for the FAD1110 (6–28 V) with internal reverse-battery protection for safe handling during testing.
- **X2** – Direct connection to the ignition-coil primary; this node can experience high-voltage transients during turn-off, so the PCB includes extended creepage and clearance distances.
- **X1** – System ground (GND) connection; must be routed with low impedance to ensure stable switching and minimized EMC emissions.

GETTING STARTED

The **CON1** connector serves as the primary supply interface for the ignition driver. The **VBAT** pin must be connected either to an external DC laboratory supply or to the high-side end of the ignition coil's primary winding, depending on the evaluation setup. The FAD1110 supports a 6–28 V operating range and incorporates internal protection structures suitable for typical automotive power conditions.

The **INH** and **INL** pins form a **differential control input** used to trigger the ignition event. The driver responds when the differential voltage between INH and INL crosses the internal threshold, enabling the IGBT and charging the coil. Pulse duration determines dwell time and thus the delivered ignition energy. Typical dwell pulses range from a few milliseconds up to the allowable maximum dwell period set by the CSSD timing capacitor.

Depending on the intended control method, the inputs may be used in one of two configurations:

- **Differential mode**: both INH and INL are actively driven (symmetrical control).
- **Single-ended mode**: INL is tied to GND at CON1, and only INH is driven (asymmetrical control).
  Both modes are supported by the FAD1110 thanks to its differential input stage with built−in spike filtering and ground-shift tolerance from –2 V to +3 V.

The **GND** pin provides the common reference potential for the DC supply, ignition driver, and external pulse generator. A low-impedance ground return is essential to maintain stable switching behavior and minimize EMC-related disturbances.

The **X2** connector provides the low-side switching output that connects to the low-potential end of the ignition-coil primary. When activated, the FAD1110 drives the IGBT, sinking current through the primary winding. When the input is released or when the maximum dwell time is exceeded, the driver turns the IGBT off, causing the inductive energy stored in the coil to generate a high-voltage ignition pulse on the secondary side.

The driver supports a wide range of inductive loads. The primary load may be any air-core inductor or ignition transformer with a primary inductance in the operational range used by typical automotive coils (approximately 1.5 mH as shown in the reference operating conditions).

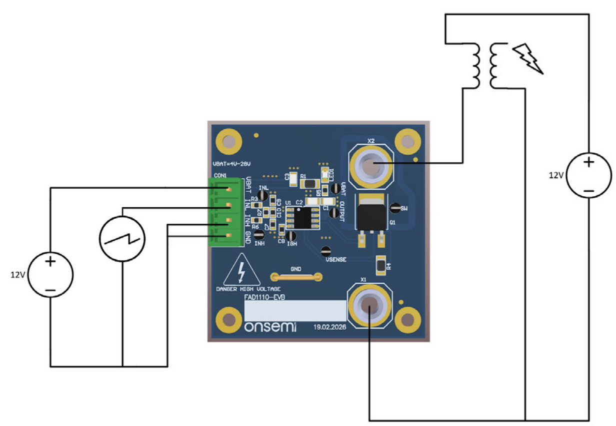

Figure 3. Application Schema for Ignition System

Current Limit

This current-limiting behavior is clearly visible in the waveform. As the primary current rises during the dwell period, the voltage across the sense resistor increases proportionally. Once the sensed voltage reaches the internal **V_SENSE threshold** (typically around 220 mV), the current slope abruptly changes and the waveform transitions from a rising linear ramp into a **flat, regulated plateau**. This plateau corresponds to the maximum allowable coil current defined by the FAD1110's internal limit circuitry.

At the same moment, the gate-drive voltage at the **OUTPUT** pin no longer remains at its maximum drive level. Instead, the driver modulates (reduces) the gate amplitude just enough to keep the current from increasing further. In the waveform, this regulation appears as:

- a **sharp transition** from rising current to a controlled constant-current region,
- followed by a **stable, nearly horizontal current level** maintained until the input command ends or until the maximum dwell-time timer forces a Hard-Shutdown event.

This visual flattening of the current curve confirms that the FAD1110 is actively regulating the coil current to prevent overstress of the IGBT and the ignition transformer.

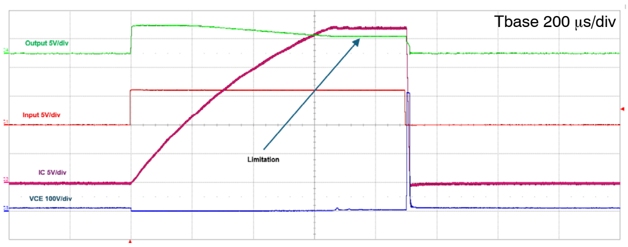

Figure 4. Current Limitation of Induction Load

Maximum Dwell Time and Hard-Shutdown (HSD)

During operation of the FAD1110, the ignition coil is not switched off through a controlled soft-decay process. Instead, if the applied input pulse exceeds the maximum dwell time, the device activates its Hard-Shutdown (HSD) mechanism, which **immediately turns off the IGBT** without entering a controlled resistive region of the collector-emitter characteristic.

This means that:

- The IGBT does **not** transition into a regulated resistive mode,
- There is **no gradual reduction** of gate-drive voltage for controlled current decay,
- The stored inductive energy is released according to the natural ignition-coil behavior, not dissipated as controlled heat inside the IGBT.

The purpose of the HSD function is to:

- Prevent extended dwell that could overheat the IGBT,
- Protect the ignition driver from excessive conduction time,
- Ensure that the coil is turned off rapidly once the dwell limit is exceeded.

As indicated in the FAD1110 timing diagram, reaching the V_SENSE limit produces a **current plateau**, and reaching the dwell-time limit (TDMAX) causes an **immediate drop of the current** when the IGBT is switched off (HSD).

In the waveform, this appears as a **sharp end of the current plateau** without the linear, ramp-down decay characteristic typical of Soft-Shutdown systems.

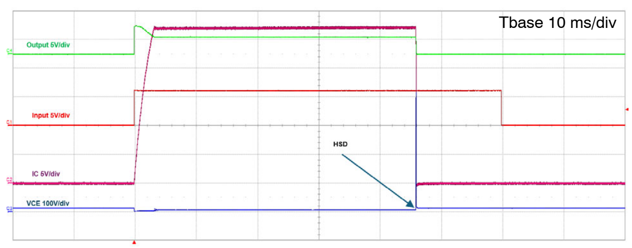

Figure 5. HSD Protection for Switch-Off Induction Load

PCB DRAWINGS

Assembly Drawings

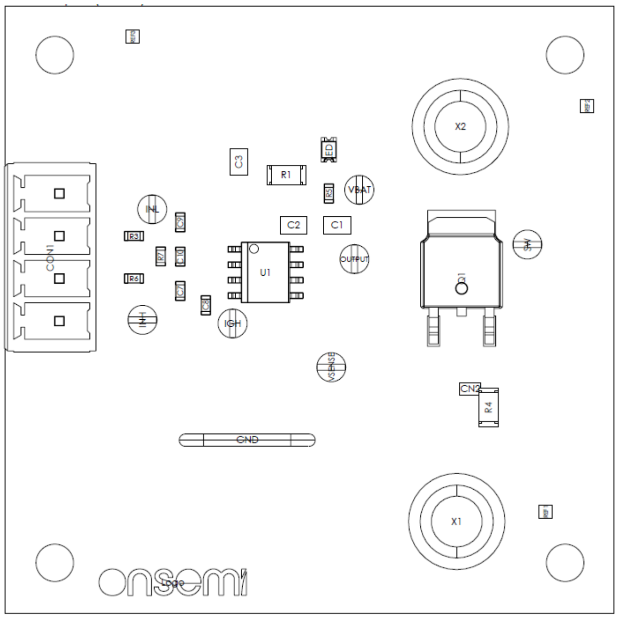

Figure 6. FAD1110EVB PCB Top Assembly Drawing

Composite Drawings

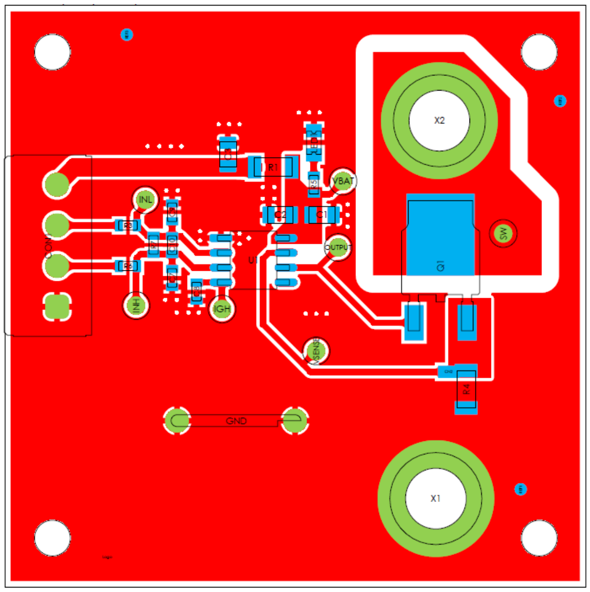

Figure 7. FAD1110EVB PCB Top Composite Drawing

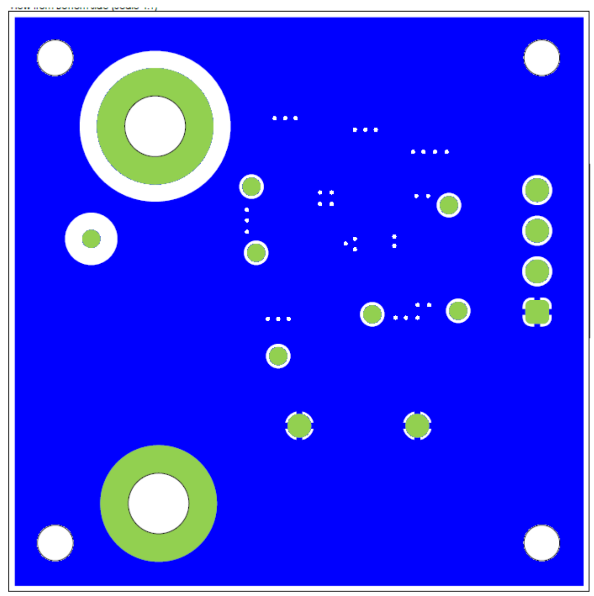

Figure 8. FAD1110EVB PCB Bottom Composite Drawing (bottom view)

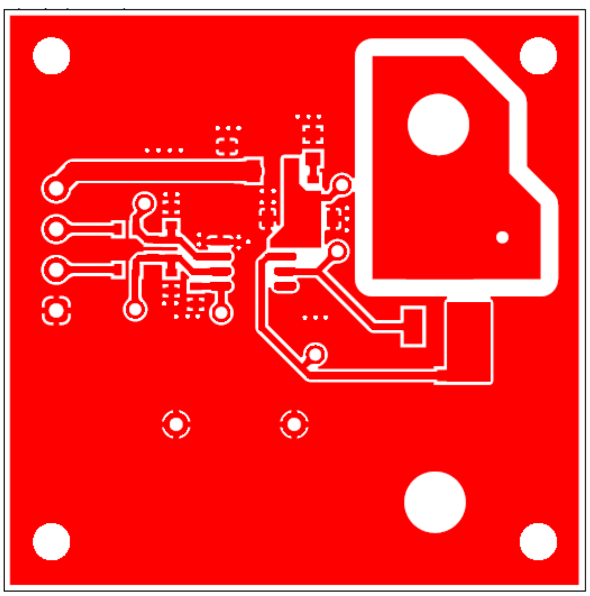

Figure 9. FAD1110EVB PCB Internal Plane 1 Drawing

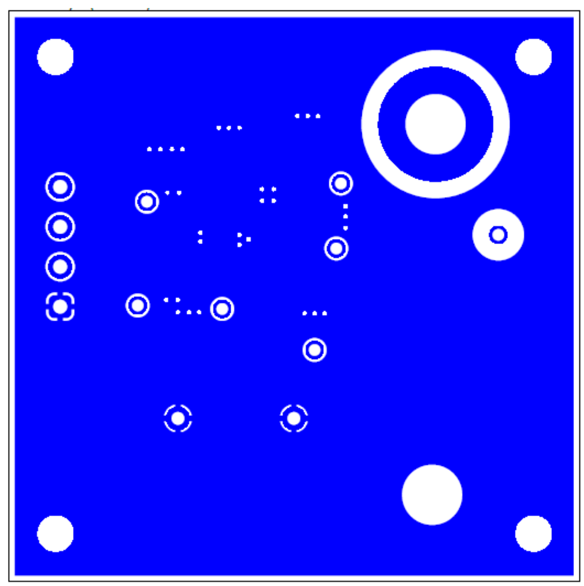

Figure 10. FAD1110EVB PCB Internal Plane 2 Drawing

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	4/14/2026

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales

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