Evaluation Board for 1200 V M3S 2-PACK SiC MOSFET module User's Manual

EVBUM2880G-EVB

Evaluation Board Description

The Evaluation Board supports **onsemi**'s 2−PACK (Half−Bridge) modules in F1 package.

NXH008P120M3F1PTG
NXH010P120M3F1PTG
NXH015P120M3F1PTG
NXH030P120M3F1PTG

(module is not assembled)

These products use SiC M3S technology to be fast and rugged and include system benefits from high efficiency to reduced system size and cost. They are used in energy infrastructure applications such as PV inverters, UPS or EV chargers.

This manual describes the board function, board layout and continuous load test description. It includes details of layout, schematics, and bill of materials.

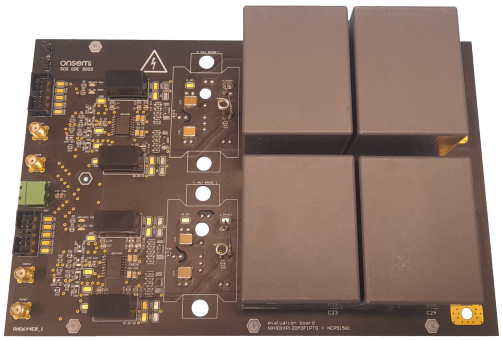
The purpose of the evaluation board is double pulse switching test and open loop power test of **onsemi**'s Half−Bridge modules.

Evaluation Board Operation

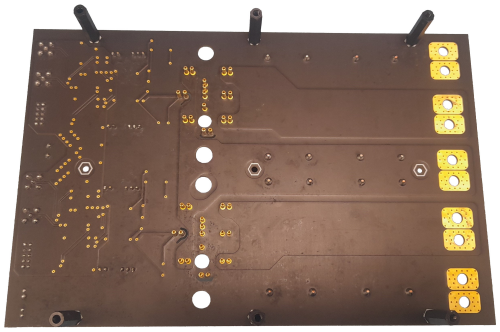
The board is designed as RoHS compliant. Design of the board was not qualified for manufacturing. No tests were made on whole operating temperature range. No lifetime tests were performed. The board must be used in laboratory environment only and must be operated by skilled personal trained on all safety standards. Further details of used components are in their respective datasheets.

Features

- Sockets for Two M3S 2−PACK Modules in F1 Package
- 260 μF Integrated DC−link Shared for Both 2−PACK Modules (Full−Bridge Usage Design)
- Isolated Gate Driver NCP51561 with 5 kV_{RMS} Isolation for Each 2−PACK
- High Thermal Emissivity Using Black PCB Color
- Sockets for Four Isolated DC−DC Sources
- Low Inductance PCB Layout
- Controlling 2−PACK Using Dead−time Generation from Single PWM Input (**Optional**)
- Controlling 2−PACK Using Dead−time Ensuring for 2 Separate PWM Inputs (**Optional**)
- Controlling 2−PACK without Any Modified Output Logic from 2 Separate PWM Inputs (**Optional**)



Top View



Bottom View

Figure 1. Evaluation Board Photo

APPLICATIONS INFORMATION

Evaluation Board Diagram

The evaluation board is logically split into shared DC−link part (260 μF including discharging resistors) and another two separate parts for each Power Integrated Module (PIM).

Shared POWER (+5 V) connector generally provides power for all driving components of both PIMs. Except for this shared POWER (+5 V) connector, both PIMs have fully separate driving options and connector inputs.

Requirement for powering insulated DC−DCs of each gate driver with different input voltage than +5 V may occur, then the Evaluation Board allows to resolder jumper (see Figure 9) to provide powering for insulated DC−DCs separately to each PIM.

DC+ and DC− power connectors are used for powering DC−link. PHASE connectors are used as a power output of each Half−Bridge.

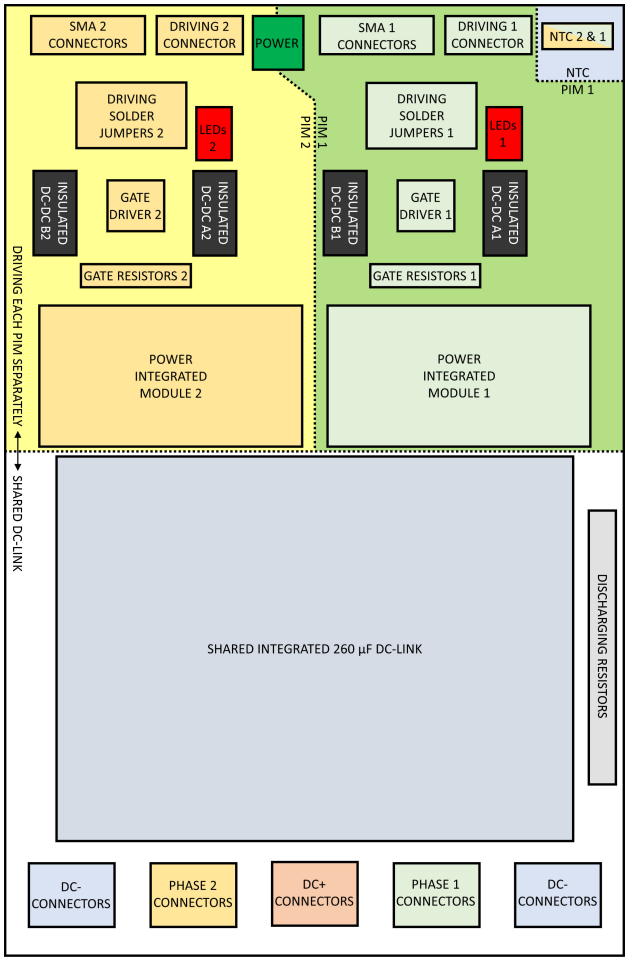


Figure 2. Simplified Block Diagram

Mechanical Dimensions

Evaluation board outline dimensions are 227.4 mm x 147.6 mm. The board outline is shown in Figure 3. Thickness of the main board is 2.0 mm.

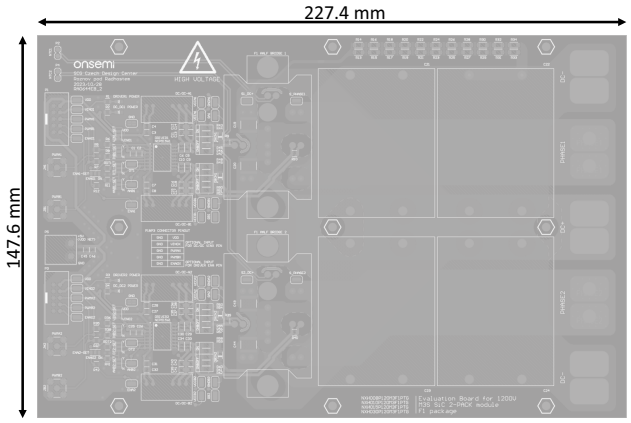


Figure 3. Main Board Dimensions

PCB Stack

Evaluation Board is a 4−layer FR4 PCB. FR4 board stack is depicted in Figure 4.

Solder mask	20 μm
Copper foil	70 μm + 25 μm plating
Prepreg	711 μm
Copper	105 μm
Rigid laminate	248 μm
Copper	105 μm
Prepreg	700 μm
Copper foil	70 μm + 25 μm plating
Solder mask	20 μm

Figure 4. 4−Layer FR4 Board Stack

Electrical Rating

The board is rated to DC nominal voltage input 800 V_{DC}. Maximum voltage in the DC link is 1000 V. There is no protection for exceeding maximum DC link voltage or for reverse polarity. No inrush current limitation is present on the board.

Driving Options for Each Power Integrated Module (PIM)

Options described below use marking without last digit (1 or 2) and this last digit is replaced with “x”. Both used

PIMs on the evaluation board have same independent driving options and jumpers differ only in last digit.

Gate driver NCP51561 is used in a version with enable (ENA) input on the Evaluation Board. If active LOW is on driver's ENA PIN set, then both outputs of a driver are connected to V_{EE} (both switches on a Half−Bridge are turned off).

This evaluation board allows using external enable input (pull−downed in absence of an input signal) or allows each gate driver to be permanently enabled.

Setting enable mode is shown in Figure 5 (on the top: using external enable signal with pull−down, in the bottom: driver is always enabled and independent of the input signal).

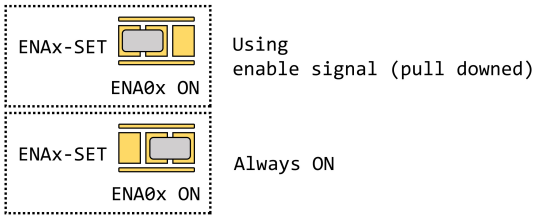


Figure 5. Solder Jumper for Enable Function

Used gate driver NCP51561 provides dead−time generation and output logic in 3 modes.

Mode 1 is driving high side and low side only from one PWM connected to high side PWM input (PWMAx). This PWM input drives high side with same logic as its input signal (only dead time is added). Low side PWM is generated as a complementary channel to the high side (if PWM input in this mode is active LOW, low side is opened). Only active LOW on ENA0x input with proper solder jumper status (Figure 5) can turn off low side gate in this mode.

Mode 2 is driving high side and low side individually, but a minimum length of dead−time (set with RDTx resistor) is ensured when a dead−time of both complementary PWM inputs is shorter. This mode also ensures that high side and low side will not be opened simultaneously.

Mode 3 is driving high side and low side fully independently from dead−time correction and high side and low side overlapping protection.

Setting dead−time generation mode is shown in Figure 6 (in the left: **Mode 1**, in the middle: **Mode 2**, in the right: **Mode 3**)

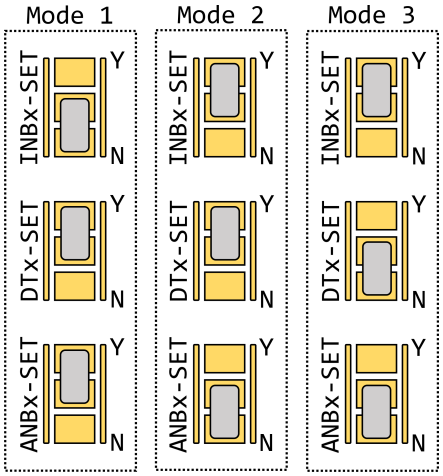


Figure 6. Solder Jumpers for Dead−time Generation Modes

Dead−time is adjusted according to an external resistance RDTx.

$$t_{DT}\ (\text{in ns}) = 10 \cdot \text{RDTx}\ (\text{in k}\Omega)$$

Please, refer to the NCP51561 manual, which provides full description of dead time generation modes.

DRIVING CONNECTOR PINout

Options described below use marking without last digit (1 or 2) and this last digit is replaced with "x".

Both used DRIVING connectors (shown in Figure 2, on PCB marked as P1 and P3) have same independent PINout, but only VDD and GND PINs are common between these connectors.

The DRIVING connector PINout is shown in Figure 7.

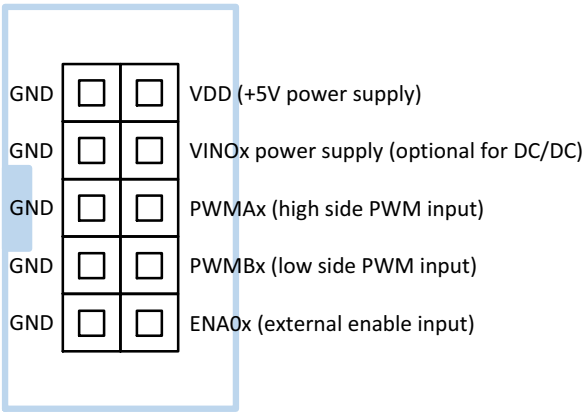


Figure 7. DRIVING (P1 and P3) Connector PINout

Evaluation Board Usage

Necessary equipment to use the board:

- 5 V / 1.5 A laboratory source
- High Voltage power supply
- PWM generator
- Common laboratory measuring equipment

Turning on procedure:

- Ensure that all power sources are turned−off
- Ensure that setup is fully prepared (check solder jumpers status, connection of all necessary power sources, used gate resistors, used DC−DCs, load connection, probes, cooling of used components etc.)
- Ensure that all PWM inputs are active LOW
- Turn on 5 V / 1.5 A laboratory source connected to P5
- Turn on alternative power source(s) for insulated DC/DCs (**by default leave out this step**, please refer to the “Gate Driver Supply Manual” for using alternative power supply for insulated DC−DCs)
- Make sure that all LEDs glow
- Verify that all high side Gate to Source voltages are equal to V_{EE} (−3.9 V while using default DC−DCs)
- Verify that all low side Gate to Source voltages are equal to V_{EE} or V_{CC} and must correspond to the solder jumpers status and status of external enable input (please do refer to the “Driving options for each PIM”)
- Turn on High Voltage source
- Start PWM operation

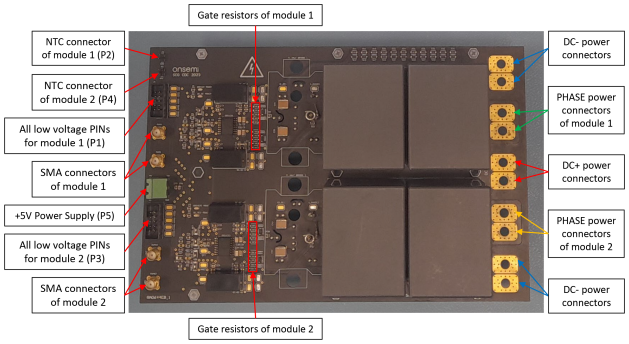


Figure 8. Board Connection

Power Supply Manual

Regulated voltage source 5 V / 1.5 A must be connected to P5. DRIVER1 POWER and DRIVER2 POWER LEDs indicate that the primary side of each gate driver is powered.

Both solder jumpers for each PIM (shown in the left in Figure 9) are by default set to V_{DD} power (V_{DD} voltage is always +5 V from common P5 power source), then all DC−DCs are also powered and DC_DC1 POWER and DC_DC2 POWER LEDs indicate input power of DC−DCs for powering secondary side of each gate driver.

Using default power option from P5 power source is recommended.

In case of no usage of any connected PIM it’s necessary to ensure no absence of its gate to its kelvin−source driving voltages. Using V_{EE} output logic to high side and low side is in this case recommended. V_{EE} output logic can be set by using external enable input (Figure 5) for unused PIM and this external enable input must be active low or floating.

Absence of a driving voltage on any gate to its kelvin−source PINs may cause Half−Bridge’s cross conduction.

It’s recommended to use high voltage source (connected to DC+ and DC−) with discharging feature and also extra voltage meter to check whether DC−link is fully discharged before any manipulation with setup.

Gate Driver Supply Manual

In case of no insulated DC−DC converters with +5 V power input or any testing requirements, DC−DCs belonging to each PIM can be optionally powered from each VIN0x (VIN01 or VIN02) PIN. These PINs are shown in Figure 7. Then respective solder jumper must be resoldered (Figure 9), and respective VIN0x power input must be ensured with enough current capability voltage source. Also, respective resistors R2 and R4 (in series with LED indicators DC_DC1 POWER and DC_DC2 POWER) must be properly changed to ensure proper lighting of LED indicators.

Setting power input to DC−DC convertors is shown in Figure 9 (in the left: powering from VDD (P5 connector), in the right: powering from respective P1 or P3 connector).

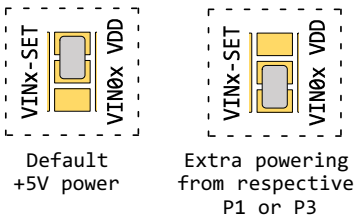


Figure 9. Insulated DC−DC Solder Jumper

Gate Resistances and Insulated DC−DCs Changing

Insulated DC−DCs can be replaced without any soldering. Gate resistances need to be replaced using soldering. Figure 10 shows where insulated DC−DCs and gate resistances are located.

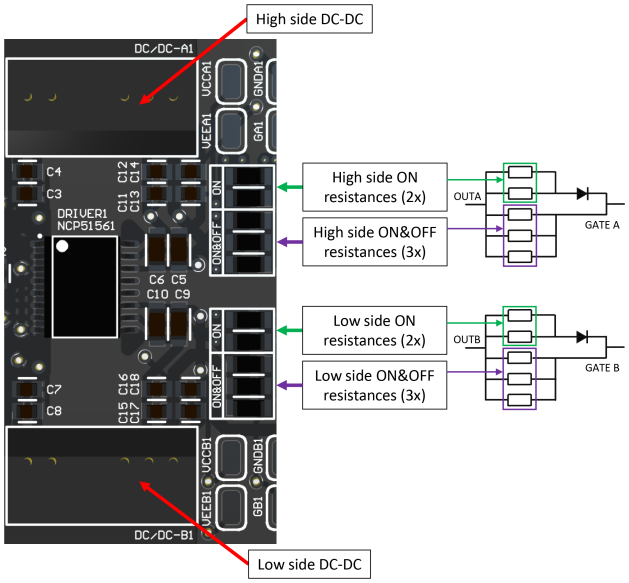


Figure 10. Gate Resistances and Insulated DC−DCs

Overall, 5 gate resistances for each switch are designed to improve thermal performance when high switching frequencies are used.

Using PWM Inputs

Evaluation Board supports only +5 V PWM input. Each PWM input can be connected optionally via SMA or relevant P1 or P3 connector. Using SMA connectors is recommended.

Evaluation Board's Usage Limits

It's recommended not to exceed 80 kHz switching frequency and for this switching frequency it's recommended not to exceed 35 A_{rms} output at each PHASE while 800 V DC−link voltage is used. User must not exceed temperature limit of each component on Evaluation Board defined by its manufacturer's datasheet with enough margin. For more information about used components please refer to the "Bill of Materials".

Switching Losses and Double Pulse Test

The switching was tested on the board with a Double Pulse Test using NXH015P120M3F1PTG, $R_{G\ (on)}$ = 2.7 Ω and $R_{G\ (off)}$ = 2.7 Ω. Tested was low side MOSFET commuting with high side diode. Current was captured by Rogowski coil attached around the pins on the PIM socket (shown in Figure 11).

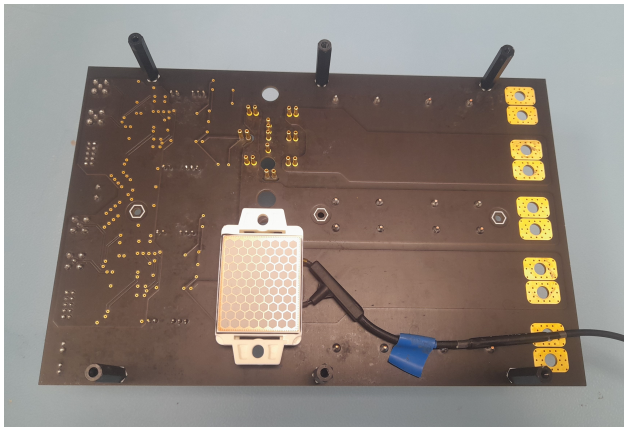


Figure 11. Double Pulse Measurement

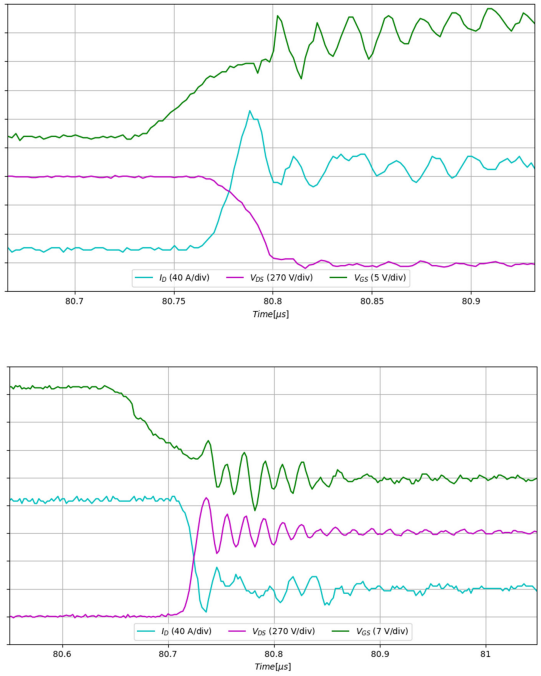


Figure 12. Switching Waveforms – Turquoise I_D, Violet V_{DS}, Green V_{GS}

The waveforms show no oscillations during switching. Voltage overshoot during turn−off for ~120 A is 360 V.

Continuous Load Test

The Evaluation Board was placed on a heatsink and connected to L filter using two NXH008P120M3F1PTG devices, $R_{G(on)}$ = 2 Ω. and $R_{G(off)}$ = 3.3 Ω. L filter was placed between PHASE outputs of both Half−Bridges.

PWM signals were generated from a MCU board. Output was a rippled current generated by a hard switching using 80 kHz switching frequency.

Output signals of a MCU board were complementary channels with constant 800 ns dead−time. Driving logic of a Full−Bridge is shown in the Figure 13.

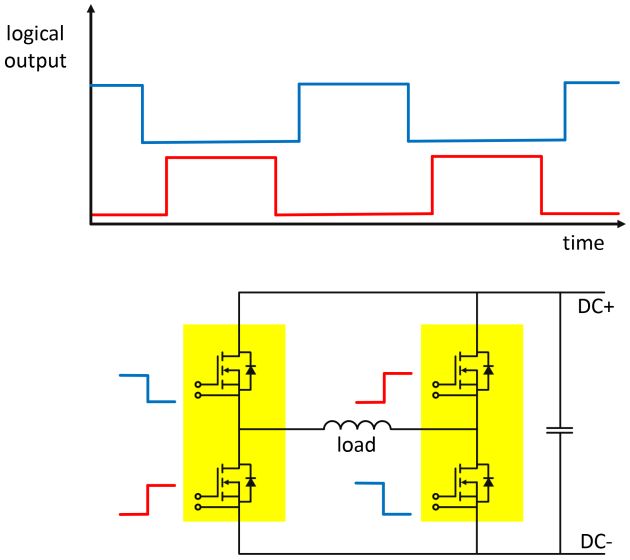


Figure 13. Full−Bridge Driving Logic

When a Pulse Width of both logical outputs (shown in a Figure 13) is the same, then RMS of an output current is minimal. Increasing Pulse Width of one logical output and decreasing Pulse Width of the opposite one logical output increases RMS of an output current. Length of a modulation period is constant and dead−time is also constant in this case. Modifying PWM signals is shown in the Figure 14.

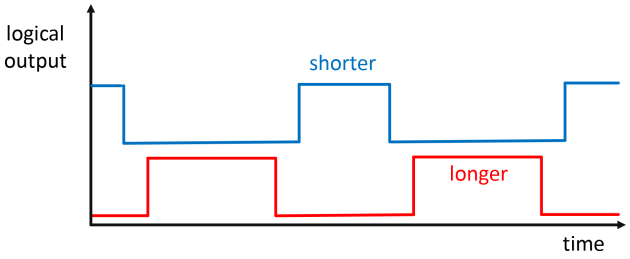


Figure 14. Principal of Increasing RMS of the Output Current

Evaluation Board delivered 35 A_{RMS} at V_{DC} = 800 V condition, reaching NTC condition 105°C in Power Integrated Module.

Figure 15. Application Board Placed on a Heatsink

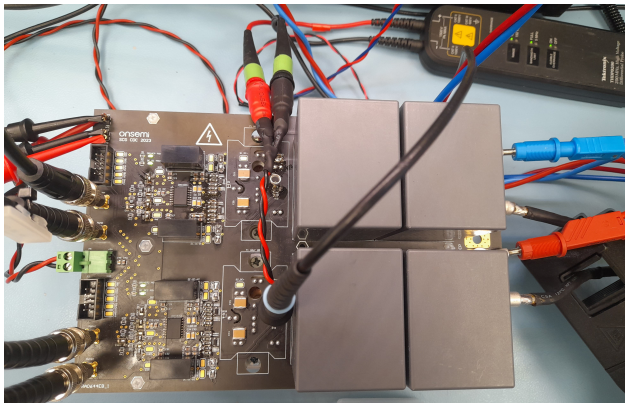


Figure 16. Continuous Load Test Setup

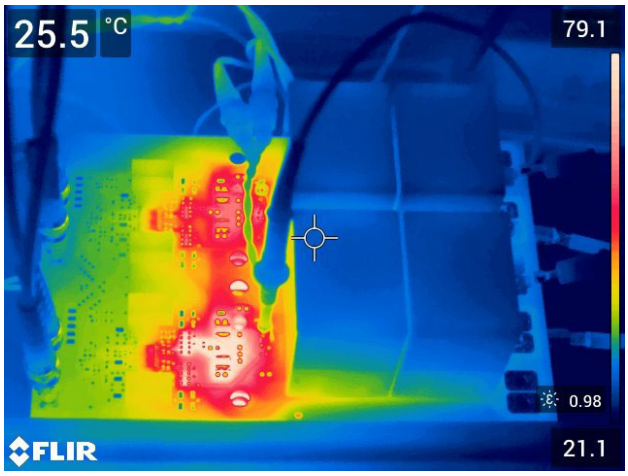


Figure 17. Temperature During Operation

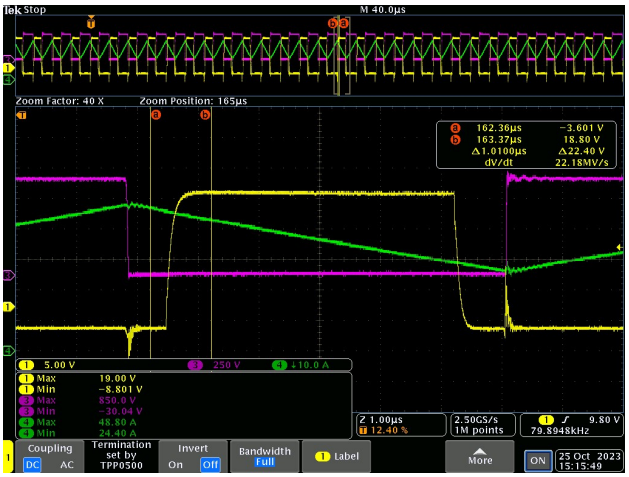


Figure 18. Application Waveforms – Yellow V_{GS}, Violet V_{DS}, Green Coil Current

Schematics

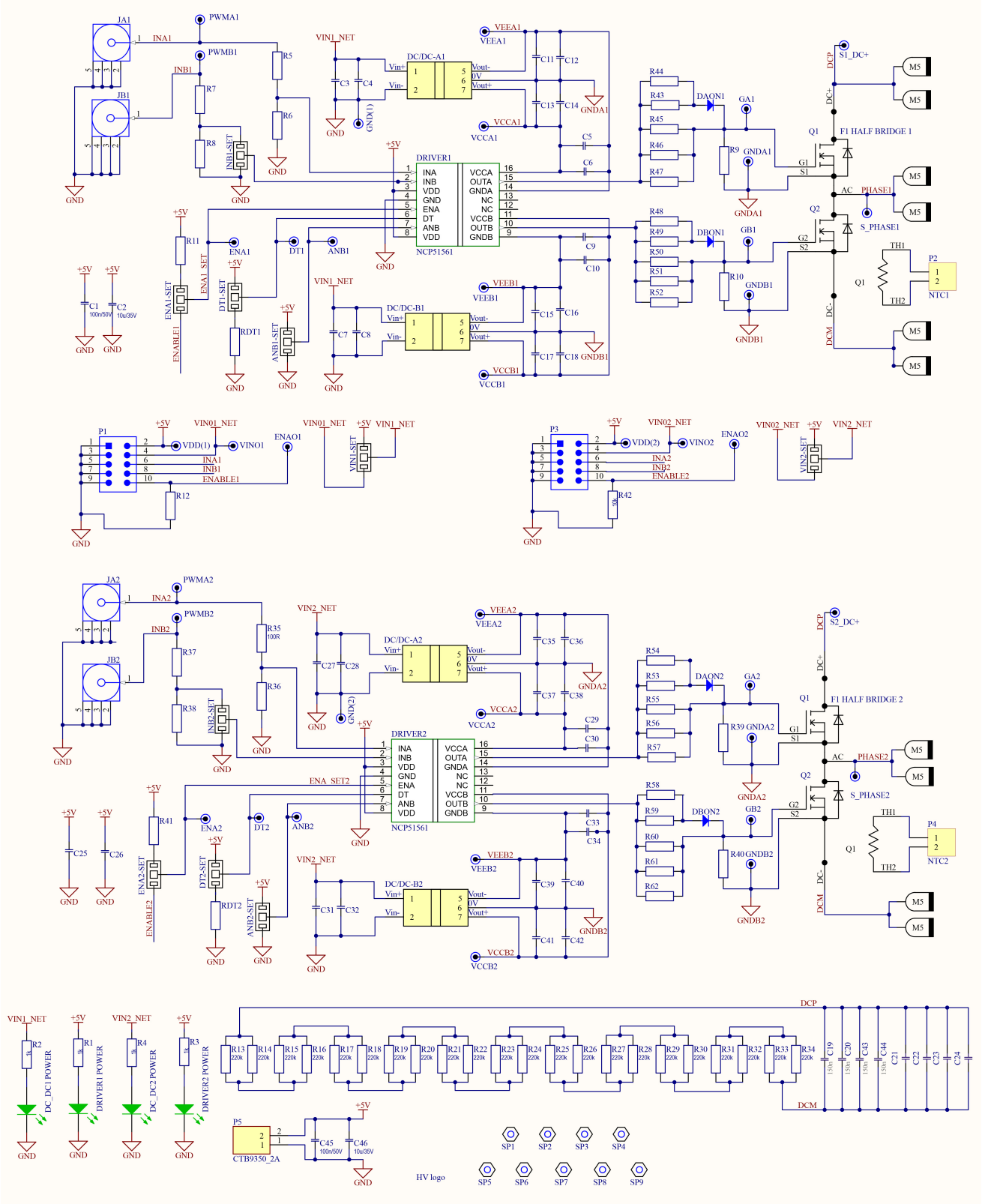


Figure 19. Complete Schematics

Layout of Evaluation Board

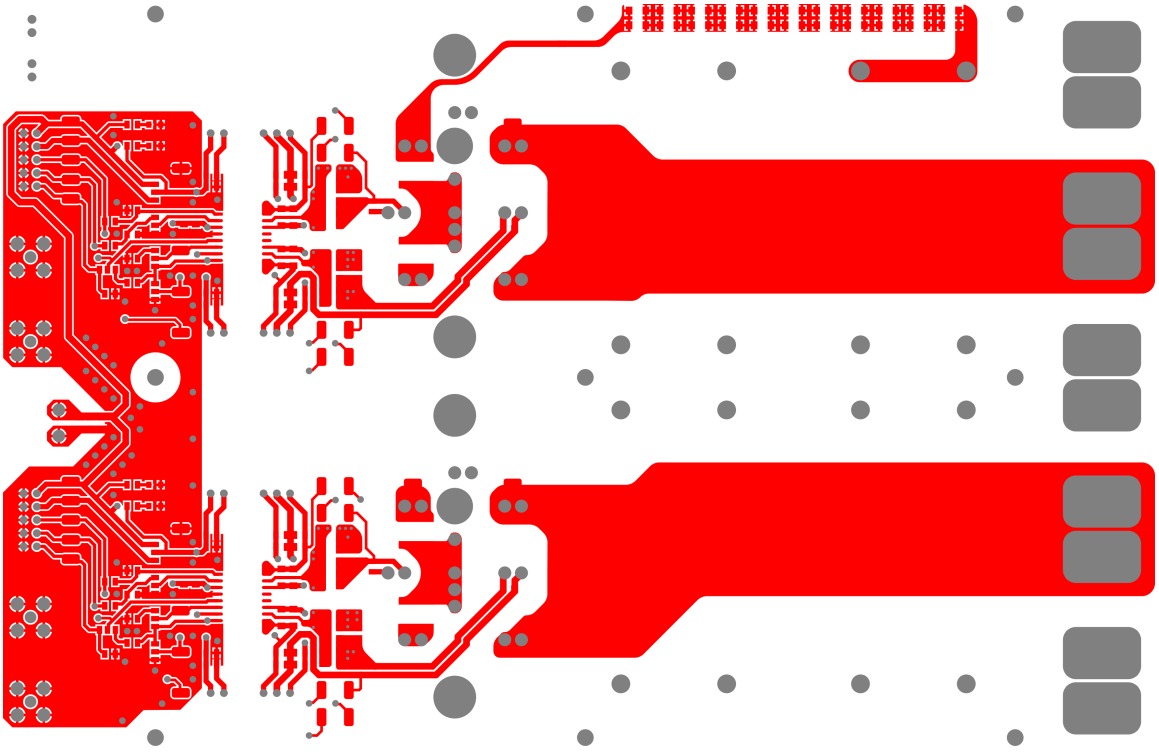


Figure 20. TOP Layer

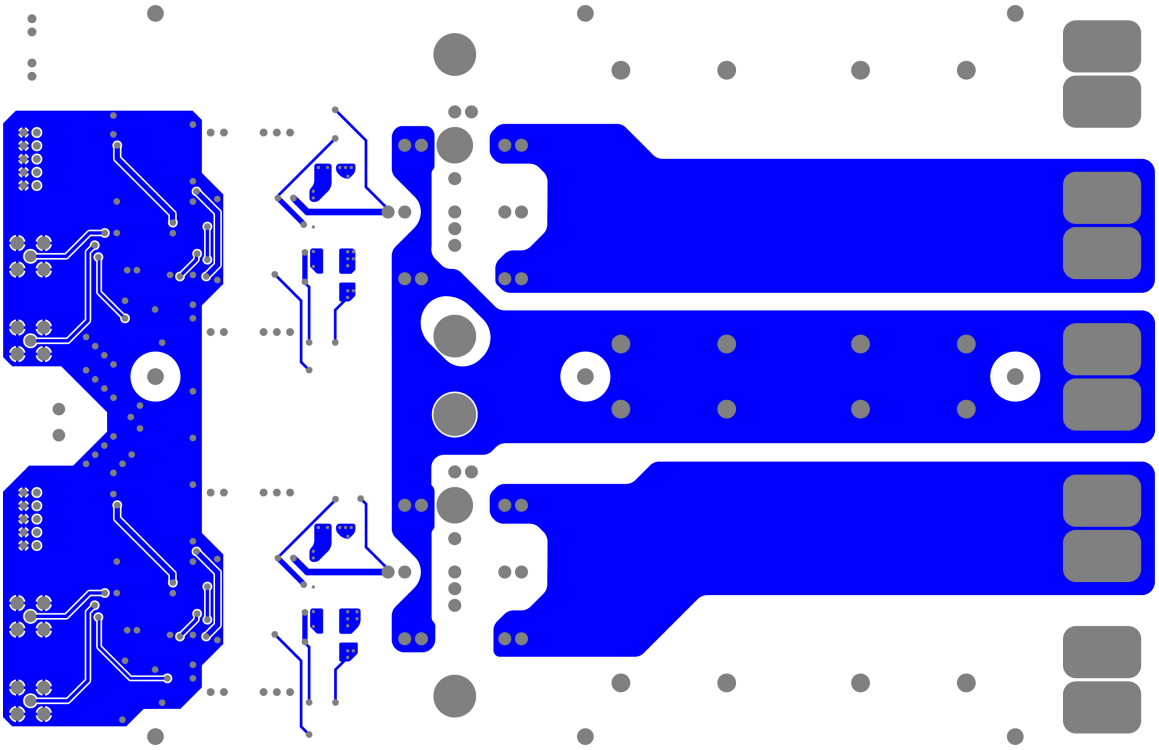


Figure 21. BOTTOM Layer

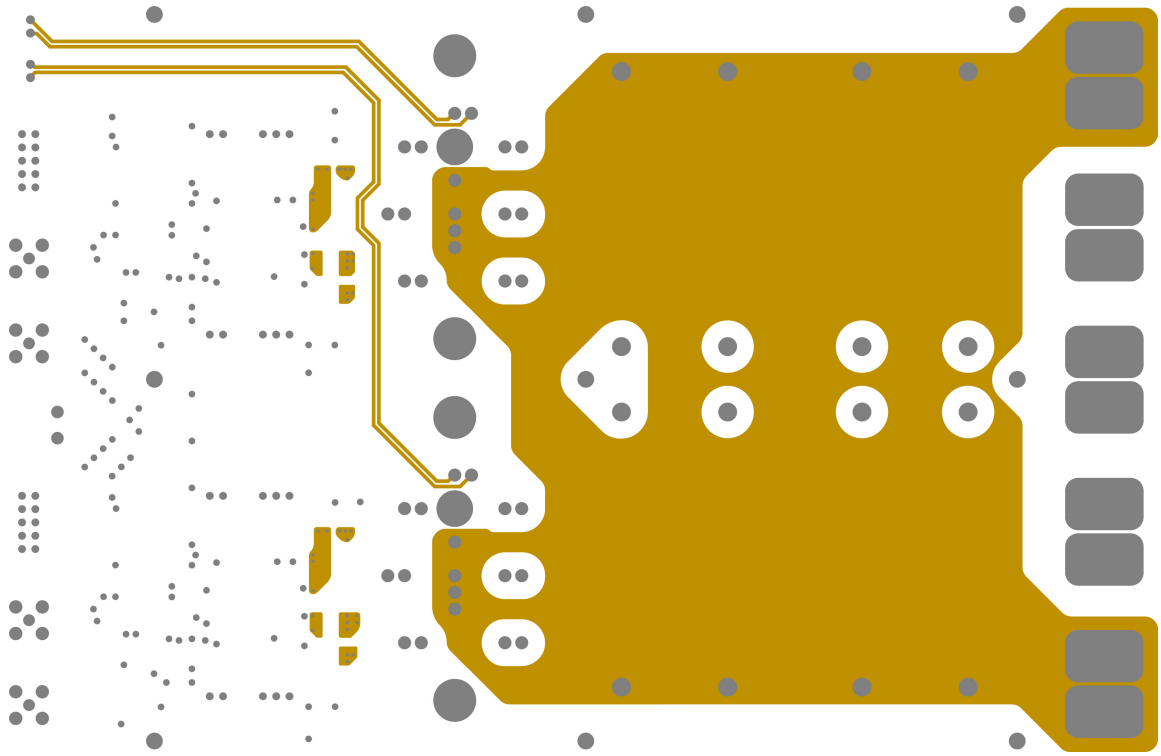


Figure 22. MIDDLE 1 Layer

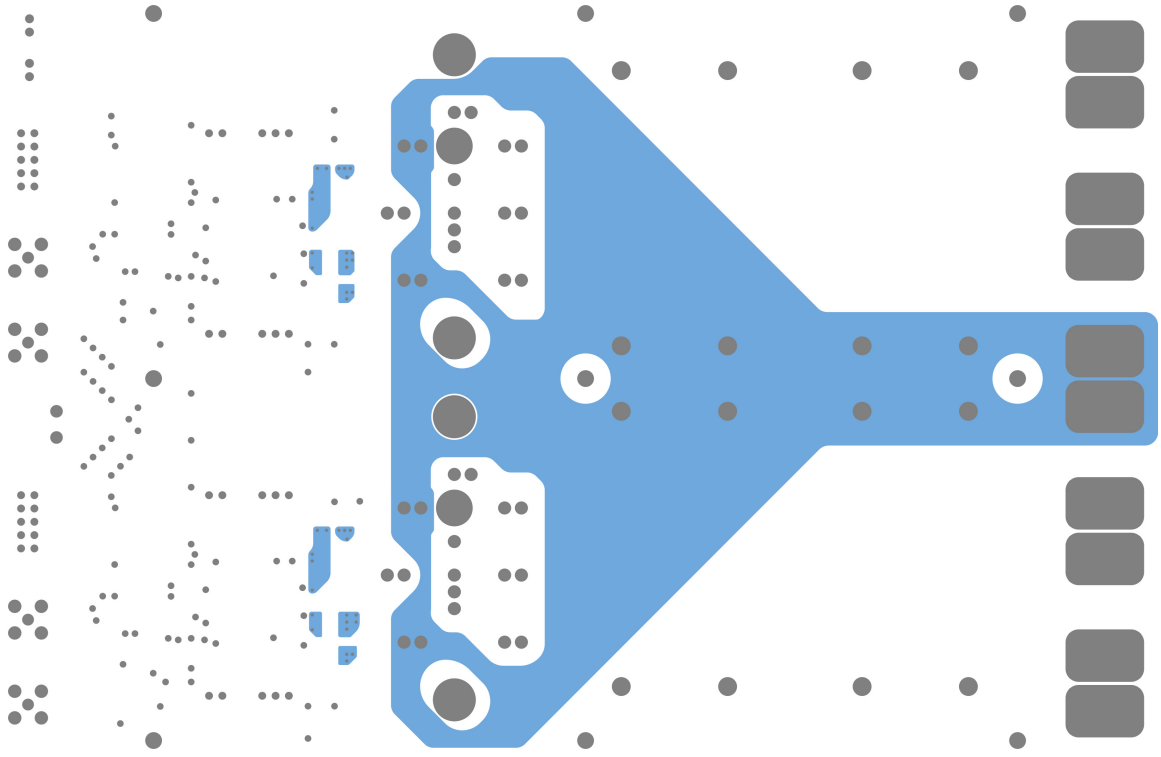


Figure 23. MIDDLE 2 Layer

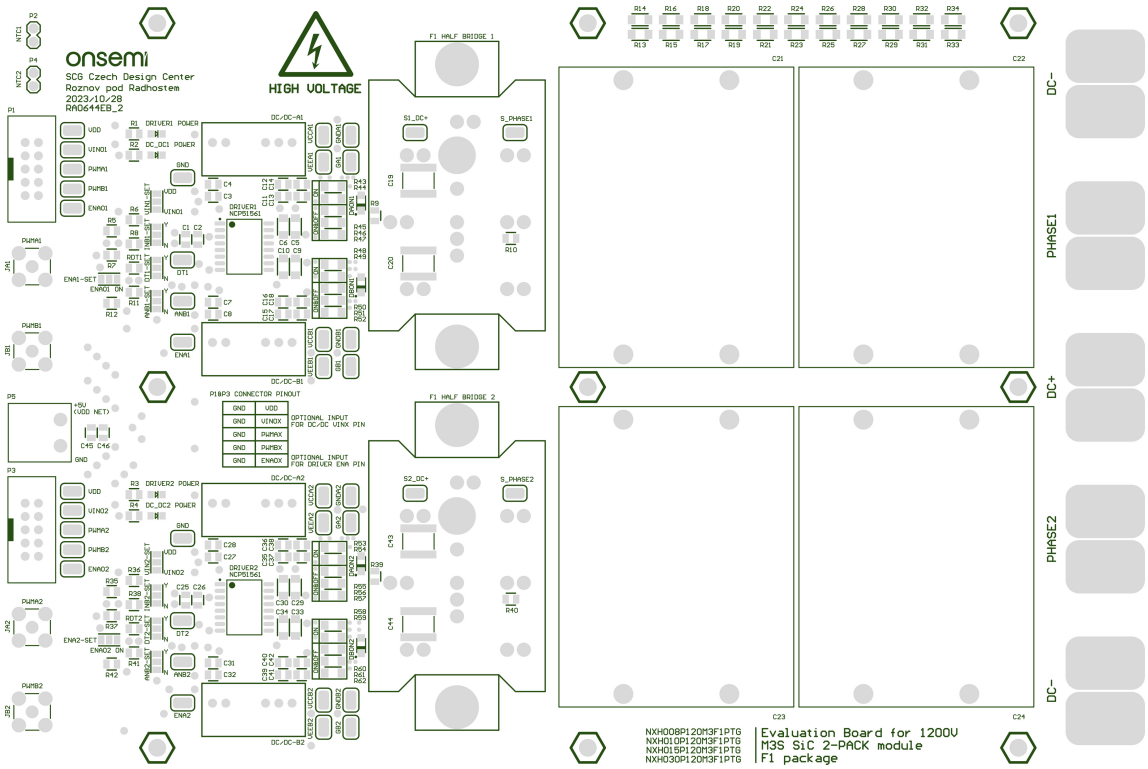


Figure 24. SILKSCREEN Top

Table 1. BILL OF MATERIAL

Designator	#	Description	Value	Manufacturer Part Number
R13, R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R29, R30, R31, R32, R33, R34	22	SMD Chip Resistor, Thick Film, AEC−Q200 WCR Series, 220 kΩ, 200 V, 250 mW	220k	TT ELECTRONICS / WELWYN WCR1206−220KFI
R6, R8, R9, R10, R12, R36, R38, R39, R40, R42	10	SMD Chip Resistor, 10 kΩ, ±5%, 125 mW, Thick Film	10k	MULTICOMP PRO MCHVR05JTEW1002
R5, R7, R35, R37	4	SMD Chip Resistor, 100 Ω, ±5%, 125 mW, Thick Film	100R	MULTICOMP PRO MCSR08X101 JTL
R11, R41	2	SMD Chip Resistor, 4.7 kΩ, ±5%, 125 mW, Thick Film	4k7	TE CONNECTIVITY CRGCQ0805J4K7
RDT1, RDT2	2	SMD Chip Resistor, 100 kΩ, ±5%, 125 mW, Thick Film	100k	TE CONNECTIVITY CRGCQ0805J100K
R1, R2, R3, R4	4	SMD Chip Resistor, 1 kΩ, ±5%, 125 mW, Thick Film	1k	TE CONNECTIVITY CRGCQ0805J1K0
R43, R44, R48, R49, R53, R54, R58, R59	8	SMD Chip Resistor, 15 Ω, ±5%, 333.3 mW, Thick Film, Pulse Withstanding	15R	PANASONIC ERJT08J150V
R45, R46, R47, R50, R51, R52, R55, R56, R57, R60, R61, R62	12	SMD Chip Resistor, 22 Ω, ±5%, 333.3 mW, Thick Film, Pulse Withstanding	22R	PANASONIC ERJT08J220V
C21, C22, C23, C24	4	Power Film Capacitor, Metallized PP, Radial Box − 4 Pin, Through Hole	65u/1100V	KEMET C4AQQEW5650A3BJ
C19, C20, C43, C44	4	SMD Multilayer Ceramic Capacitor, 0.15 μF, 1 kV, ±10%, X7R	150n/1kV	KEMET C2225C154KDRACAUTO

Table 1. BILL OF MATERIAL (continued)

Designator	#	Description	Value	Manufacturer Part Number
C2, C4, C8, C12, C14, C15, C17, C26, C28, C32, C36, C38, C39, C41, C46	15	SMD Multilayer Ceramic Capacitor, 10 μF, 35 V, ±10%, X6S	10u/35V	MURATA GRM21BC8YA106KE11L
C1, C3, C7, C11, C13, C16, C18, C25, C27, C31, C35, C37, C40, C42, C45	15	SMD Multilayer Ceramic Capacitor, 100 nF, 50 V, ±10%, X7R	100n/50V	WURTH ELEKTRONIK 885012207098
C6, C10, C30, C34	4	SMD Multilayer Ceramic Capacitor, 10 μF, 35 V, ±10%, X6S	10u/35V	MURATA GRT31CC8YA106KE01L
C5, C9, C29, C33	4	SMD Multilayer Ceramic Capacitor, 100 nF, 50 V, ±10%, X7R	100n/50V	WURTH ELEKTRONIK 885012208087
DAON1, DAON2, DBON1, DBON2	4	Trench Schottky Rectifier, Very Low Leakage 2 A, 60 V	**onsemi** NRVTS2H60ESF	
DC/DC−A1, DC/DC−A2, DC/DC−B1, DC/DC−B2	4	Isolated Through Hole DC/DC Converter, ITE, 1:1, 2 Output, 18 V, 80 mA	CUI VQA3S−S5−D18−S	
DRIVER1, DRIVER2	2	5 kVrms 4.5−A/9−A Isolated Dual Channel Gate Driver	**onsemi** NCP51561BADWR2G	
DC_DC1 POWER, DC_DC2 POWER, DRIVER1 POWER, DRIVER2 POWER	4	LED, Yellow Green, SMD 0805, 20 mA, 2.1 V, 569 nm	DIALIGHT 599−0160−007F	
P5	1	Terminal Block, Header, Plug, 5 mm, 2 Ways, 20 A, 320 V, Through Hole Right Angle	CAMDENBOSS CTB9350/2A	
JA1, JA2, JB1, JB2	4	RF / Coaxial Connector, SMA Coaxial, Straight Jack, Solder, 50 Ω, RG174	LPRS SMA CONNECTOR	
P1, P3	2	Pin Header, Board−to−Board, 2.54 mm, 2 Rows, 10 Contacts, Through Hole Straight	WURTH ELEKTRONIK 61201021621	
ANB1, ANB2, DT1, DT2, ENA1, ENA2, ENAO1, ENAO2, GA1, GA2, GB1, GB2, GND (2x), GNDA1, GNDA2, GNDB1, GNDB2, PWMA1, PWMA2, PWMB1, PWMB2, S1_DC+, S2_DC+, S_PHASE1, S_PHASE2, VCCA1, VCCA2, VCCB1, VCCB2, VEEA1, VEEA2, VEEB1, VEEB2, VDD (2x), VINO1, VINO2	38	PCB Test Point, S1751 Series, Surface Mount, Brass, Tin Plated Contacts	HARWIN S1751−46	
F1 HALF BRIDGE 1, F1 HALF BRIDGE 2	2	Full SiC **onsemi** 2PACK module	NXH008P120M3F1, NXH010P120M3F1, NXH015P120M3F1, NXH030P120M3F1	
DC/DC−A1, DC/DC−A2, DC/DC−B1, DC/DC−B2	20	Circuit Board Hardware − PCB 10 u AU OVER NI 21 CON	Mill−Max 8975−0−15−15−21−27−10−0	
F1 HALF BRIDGE 1, F1 HALF BRIDGE 2	36	2 mm socket, solder connection, to 1 mm pressfit	Stäubli Electrical Connectors 41.0001	
Printed Circuit Board	1	FR4 Tg 150°C (ISOLA IS400), 2 mm, Copper 70/105/105/70 um, TOP/BOT mask BLACK, TOP labels WHITE, Final Surface HAL PbSn	−−−	
SP1, SP2, SP3, SP4, SP5, SP6, SP7, SP8, SP9	9	Plastic Fastener − Standoff, Nylon 6.6 (Polyamide 6.6), M3, Hex Female, 30 mm, 30 mm	ETTINGER 05.30.330	
SP1, SP2, SP3, SP4, SP5, SP6, SP7, SP8, SP9	9	Plastic Screw − Nylon 6.6, M3, 10 mm Length, WA−SCRW Series	WURTH ELEKTRONIK 97791003111	
P2, P4	2	2 Position Pin Header, 2.54 mm Pitch	samtec TSW−102−07−T−S	

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