Ezairo® 8310 Hardware Evaluation Board User's Manual

EVBUM2877/D

INTRODUCTION

Purpose

IMPORTANT: **onsemi** acknowledges that this document might contain the inappropriate terms "white list", "master" and "slave". We have a plan to work with other companies to identify an industry wide solution that can eradicate non−inclusive terminology but maintains the technical relationship of the original wording. Once new terminologies are agreed upon, future products will contain new terminology.

This group of topics provides information on the configuration and use of the Ezairo 8310 Hardware Demo Board.

The Hardware Demo Board (referred to as the HDB) is designed to be used by engineers and developers along with a software development kit, such as the Ezairo 8300 SDK, to evaluate the performance and capabilities of the Ezairo 8310, and to develop applications for this device.

Conventions

The following conventions are used in this group of topics to signify particular types of information:

`Monospace font`
Macros, functions, defines and addresses.

`CAPITALIZED MONOSPACE FONT`
Component names and pin names.

Italics
File and path names, or any portion of them.

`<angle brackets>`
Optional parameters and placeholders for specific information. To use an optional parameter or replace a placeholder, specify the information within the brackets; do not include the brackets themselves.

Note, Important, Caution, Warning
Information requiring special notice is presented in several attention−grabbing formats depending on the consequences of ignoring the information:
NOTE: Significant supplemental information, hints, or tips.
IMPORTANT: Information that is more significant than a Note; intended to help you avoid frustration.
CAUTION: Information that can prevent you from damaging equipment or software.
WARNING: Information that can prevent harm to humans.

Further Reading

For any technical information not covered in this group of topics, refer to the following documents:

- *Integrated Development Environment User's Guide for Ezairo 8300*
- *CFX DSP Architecture Manual*
- *Ezairo 8300 Hardware Reference*
- *Ezairo 8300 Firmware Reference*
- *Ezairo 8310 Datasheet*

HDB DESIGN AND OVERVIEW

This topic covers an introduction to the Ezairo 8310 Hardware Demo Board, and an overview of its design and features.

Introduction

The Ezairo 8310 is the next generation audio DSP hybrid from onsemi, and is the successor to the Ezairo 7110. The Ezairo 8310 HDB is designed for ease of use when evaluating capabilities of, and developing applications for, the Ezairo 8310 audio DSP. For more information about the Ezairo 8310, consult the Ezairo 8310 datasheet.

When using the HDB, many configuration options are available via standard 0.1−inch header pins. These pins also provide access to many of the Ezairo 8310 device's pins, including all 15 DIOs. The HDB is designed to work with the Ezairo 8300 SDK software tools created by **onsemi**.

The Renesas® microcontroller unit (MCU) that is present on the HDB is used to interface with the Ezairo 8310, via USB with a PC, for easy debugging, data collection, and monitoring. It is also possible to perform the same operations via the 20−pin J−Link header and a J−Link communication device, or via the 6−pin DIN connector using a compatible I2C serial communication device, such as the Promira Serial Interface device. The Ezairo 8310 HDB's main functional blocks are presented in the "Ezairo 8310 HDB Overview" figure (Figure 1), below.

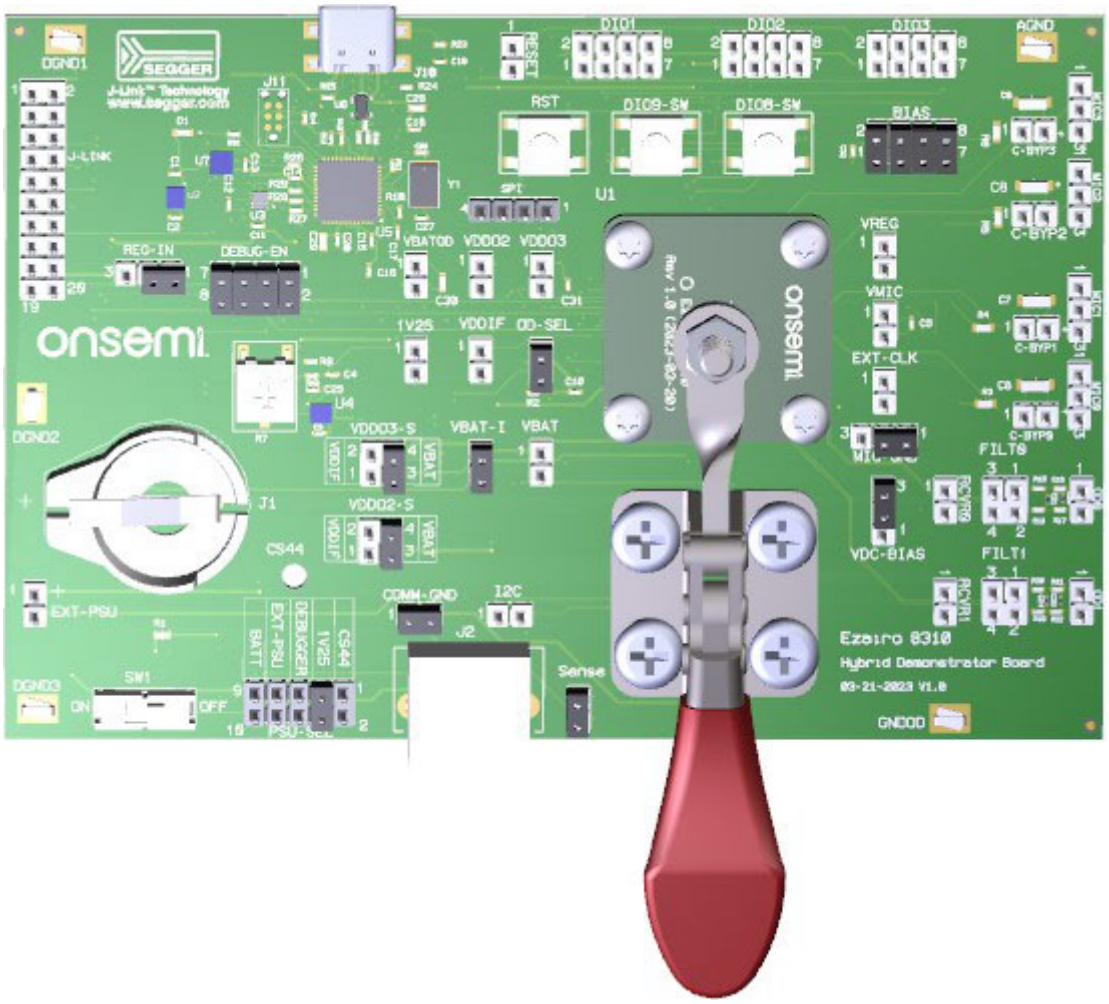

Figure 1. Ezairo 8310 HDB Overview

Ezairo 8310 HDB Features

The Ezairo 8310 HDB enables developers to evaluate the performance and capabilities of the Ezairo 8310, in addition to developing, demonstrating, and debugging applications. Key features of the HDB include:

- Access to all debug interfaces
  - Connectors to connect to external I^{2}C or SWJ−DP debug communications hardware
  - A J−link onboard solution that is accessible via the USB−C port
- Access to all Ezairo 8310 interfaces via standard 0.1−inch headers
- Three push−button switches
  - 1 dedicated to resetting the device via the NRESET pin
  - 1 connected to DIO8
  - 1 connected to DIO9
- Test points and GND hooks for easy probing
- Battery holder
- Current measuring headers
- Easily−configurable power supply options

CONFIGURATION

This group of topics describes how to configure various characteristics of your HDB for use in different circumstances.

Power Supply

The Ezairo 8310 HDB is equipped with a flexible and easy−to−use power supply. The HDB can be powered from any communication device that is connected to it, and can also be powered externally or via an on−board regulator. Configuration of the power supply is achieved with the following configuration headers, shown in the “Power Supply Configuration Headers” table (Table 1).

Table 1. POWER SUPPLY CONFIGURATION HEADERS

Designator	Function
PSU−SEL	Main configuration header, selects the source for VBAT
VBAT−I	Current measurement header for VBAT
REG−IN	Selects the 5V source used for the HDB
OD−SEL	Selects the receiver output voltage source
COMM−GND	Connects the serial communication device's ground to the HDB ground. Keep shorted in normal operation with a serial communication device.
EXT−PSU	Used for connecting an external power supply. For example, it can be used to connect a bench−top power supply.
VDDO2/3	Selects the power supply for the corresponding DIO domain

HDB Power Supply

The Ezairo 8310 can be powered from any one of several sources: the onboard battery connector, an external power supply connected via header pins, or a connected communication device. Shorting two pins together on the PSU_ SEL header chooses which supply source to use; see the "Ezairo 8310 Power Supply Options" table (Table 2) for the options available. Do not connect two different power sources at the same time.

It is also possible to separately turn off the Ezairo 8310 using the on−off switch. This only turns off power to Ezairo 8310, not the onboard Renesas MCU. This can, for example, be used to save battery power when using a battery as the power supply source, because the Atmel MCU is not powered via VBAT. For the Ezairo 8310 to be powered, the VBAT−I header also needs to be shorted. The VBAT−I header optionally provides a location to measure the current consumption of the Ezairo 8310 device.

When configuring the HDB to use the 1.25 V regulator, you can choose which source to power the regulator with the REG−IN header allows the user to power the board either from the 5 V supplied by the USB−C connector or from the J−Link connector. See the "VBAT Supply" table (Table 3) and the "5 V Source Selection" table (Table 4) for more details. The 1.25 V regulator is adjustable through R7 potentiometer.

Table 2. Ezairo 8310 POWER SUPPLY OPTIONS

PSU_SEL	Power Supply Source
Short pin 1 to 2, all others open	CS44 optional connector
Short pin 3 to 4, all others open	1.25 V on−board LDO
Short pin 5 to 6, all others open	Promira Communication Device
Short pin 7 to 8, all others open	External Bench Power Supply
Short pin 9 to 10, all others open	Battery (onboard battery holder)

Table 3. VBAT SUPPLY

Pin Name	Min	Nom	Max
VBAT*	0.9 V	1.25 V	2.0 V

*VBAT below 1.0 V leads to degraded performance of the internally regulated power rails.

Table 4. 5 V SOURCE SELECTION

REG−IN	5 V Source
Short pin 1 to 2	The selected source is USB−C
Short pin 2 to 3	The selected source is the J−Link connector

DIO Power Supply

The Ezairo 8310 exposes 15 DIOs split among 3 different power domains: VBAT, VDDO2 and VDDO3. On the Ezairo 8310 HDB VDDO2 and VDDO3 domains are connected to selection headers that allows the domains to be powered by VBAT or VDDIF. The "VDDOx Power Supply Options and Configuration" table (Table 5) details the configuration options.

Table 5. VDDOx POWER SUPPLY OPTIONS AND CONFIGURATION

VDDOx Source	Header Configuration
VDDIF	Short pins 1 & 2
VBAT	Short pins 3 & 4

Renesas Microcontroller Power Supply

The Renesas MCU core is powered by a 3.3 V LDO regulator, which is in turn powered by a 5 V rail supplied by a USB connection. The rest of the voltage supplied to the MCU, for digital inputs/outputs, analog references, etc., are provided by the 3.3 V regulator.

Communication

There are three ways of achieving communication between the Ezairo 8310 Hardware Demo Board and the Ezairo 8300 Evaluation and Development Board.

The USB−C connection (J10) is a J−Link onboard solution that provides a SWJ−DP interface for debugging the Ezairo 8310 at up to 2MHz. The TC2030−IDC connector (J11 header) is used to program the Arm® Cortex®−M3 processor with J−Link firmware. This is pre−programmed onto the HBD as a factory standard.

It is also possible to connect and debug the Ezairo 8310 via standard JTAG. The JTAG (JLINK header) connector is compatible with SEGGER® J−Link debugging devices.

Additionally, communication and debugging of Ezairo 8310 can be achieved through the Promira Serial Platform from Total Phase™, through an I²C interface. The Communication Accelerator Adapter (CAA) is also supported but is considered obsolete. The serial interface can be connected to the CAA or Promira through the 6−pin DIN connector. The “DIN Connector Pinout” table (Table 6) shows details of the DIN connector.

Table 6. DIN CONNECTOR PINOUT

Pin Number	Serial Interface Pin Description
1	Supply Voltage from the Serial Interface
2	System Ground
3	SCL (I²C Clock)
4	SDA (I²C data)
5	VBAT (Sense Voltage)
6	No Connect

For troubleshooting purposes, the I²C signals can be probed on a standard 0.1−inch header, labelled IC, that allows connection to the SDA (pin 2) and SCL (pin 1).

A block diagram of the communication connections is shown in the “Hardware Demo Board Communication Connections” figure (Figure 2), and an overview in tabular form is presented in the “Communication Configuration” table (Table 7).

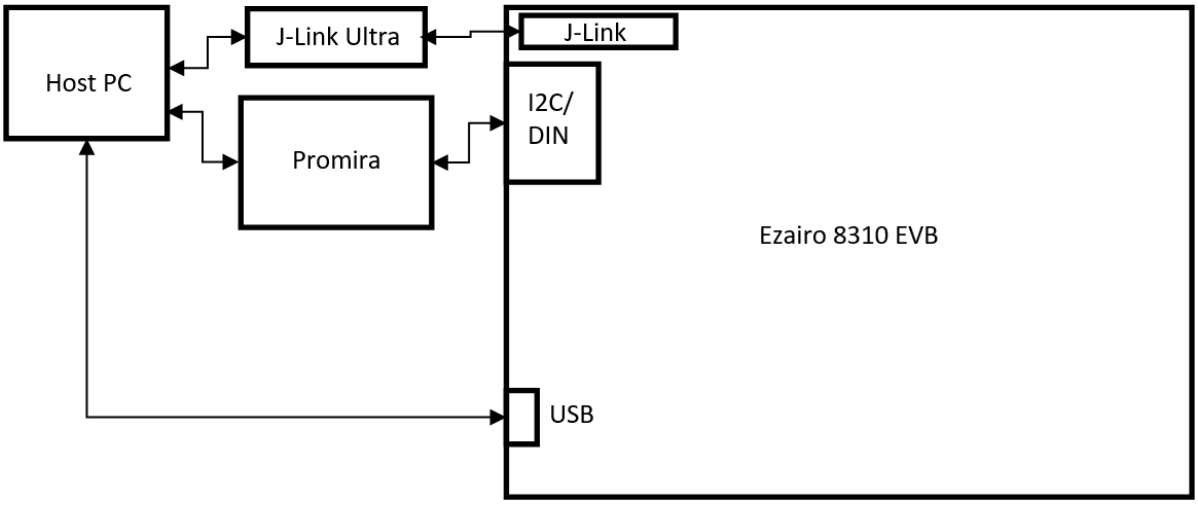

Figure 2. Hardware Demo Board Communication Connections

Table 7. COMMUNICATION CONFIGURATION

Designator	Configuration Description
SENSE	Connects VBAT to the SENSE pin on the 6−pin DIN connector, if shorted
COMM−GND	Connects the ground from the Promira /CAA to the HBD ground, if shorted
EXT−CLK	Pin used to connect an external clock source to drive the Ezairo 8310
I2C	Can be used to connect an I²C device, instead of using the 6−pin DIN connector

Input Stage

A new feature of Ezairo 8300, and therefore of Ezairo 8310, is a very high impedance input stage (~GΩ). This necessitates some consideration when connecting devices to the inputs. The most important factor is the need to add a DC bias for devices that do not inherently produce a DC bias of their own. Since microphones produce their own DC bias, they do not cause an issue. However, many audio measurement instruments do not introduce DC bias, and for these, the bias needs to be added. To connect a device that does not generate a DC bias, see the "Header Configuration Required to Enable DC Bias" table (Table 8). To connect a device that generates its own DC bias, such as a microphone, see the "Header Configuration for Disabling DC Bias" table (Table 9).

Table 8. HEADER CONFIGURATION REQUIRED TO ENABLE DC BIAS

Designator	Configuration for DC Bias
VDC−BIAS	Short pins 2 & 3
BIAS	Short pins 1 & 2 for channel AI0 Short pins 3 & 4 for channel AI1 Short pins 5 & 6 for channel AI2 Short pins 7 & 8 for channel AI3
C−BYPx	Leave open pins 1 & 2
AIx/MICx	Connect audio source to Aix or MICx, leave other connector open

Table 9. HEADER CONFIGURATION FOR DISABLING DC BIAS

Designator	Configuration for DC Bias
VDC−BIAS	Leave open
BIASx	Leave open
C−BYPx	Leave open
AIx/MICx	Leave open
AIxH	Connect audio source

Output Stage

There are two digital outputs (RCVR0, RCVR1) available on the HDB through standard 0.1−inch header. The direct digital outputs are available on headers FILTEN0, FILTEN1, RCVR0, and RCVR1. Separate RC filter networks are provided to attenuate out−of−band noise from the direct digital outputs when connected to high impedance audio measurement equipment (OD0, OD1). The onboard RC filters are enabled by the FILTEN0/FILTEN1 headers as described in the "Output Stage Enable Configuration" table (Table 10). The user can choose to use VBAT as the output driver supply voltage, or supply a separate voltage on the VBATOD header.

To enable these options, follow the "Onboard RC Filter Configuration" table (Table 11).

Table 10. OUTPUT STAGE ENABLE CONFIGURATION

Designator	Configuration Description
OD−SEL	Short pins 1 & 2 to power the output drivers with VBAT. Leave pins 1 & 2 open and connect a voltage source to the VBATOD header to power the output drivers from an external source.

Table 11. ONBOARD RC FILTER CONFIGURATION

Function	FILTEN0/FILTEN1
Disabled	Open pins 1 to 3 Open pins 2 to 4
Enabled	Short pins 1 to 3 Short pins 2 to 4

NOTE: To connect receivers or loudspeakers (without the RC filter), use headers RCVR0/RCVR1 or FILTEN0/FILTEN1.

Digital Input/Output (DIO)

The Ezairo 8310 HDB contains 15 DIO signals available on three headers DIO1, DIO2 and DIO3. The headers provide access to all DIO signals, which in turn provide access to a wide variety of interfaces (GPIO, SPI, PCM, I²C, UART, LSAD, clocks). See the "DIO/RFIO Reference Domains" table (Table 12) for pinout and reference domains. The three available sources for the VDDO domains (VDDIF, VDDO2 and VDDO3) are available at each end of the row of DIO headers.

Table 12. DIO/RFIO REFERENCE DOMAINS

DIOs	DIO Header Pin	Header	Reference Domain	Alternate Function on Board
5	3	DIO1	VDDIF	SPI_CS (`externalmemory`)
8	5	DIO1	VDDIF	DIO8−SW
9	7	DIO1	VDDIF	DIO9−SW
10	2	DIO1	VDDIF	
11	4	DIO1	VDDIF	
18	3	DIO2	VDDO2	
19	5	DIO2	VDDO2	

Table 12. DIO/RFIO REFERENCE DOMAINS (continued)

DIOs	DIO Header Pin	Header	Reference Domain	Alternate Function on Board
20	7	DIO2	VDDO2	
21	2	DIO2	VDDO2	
22	4	DIO2	VDDO2	
23	6	DIO2	VDDO2	
24	3	DIO3	VDDO3	
25	5	DIO3	VDDO3	
26	7	DIO3	VDDO3	
28	2	DIO3	VDDO3	

The Ezairo 8310 HDB has two momentary switches that can be used as momentary hard pull−downs on DIO8 and DIO9 (SW3). DIO35 is also connected to the EXT−CLK header for connecting an external clock source to the Ezairo 8310.

The RESET switch can be used to reset the Ezairo 8310.

For more information on the DIOs, refer to the *Ezairo 8300 Hardware Reference*.

Test Point Headers

The “Measurement Test Points” table (Table 13) shows a list of 0.1−inch headers on the HDB that are provided as measurement test points. There are also several ground hooks available on the HDB as an easy way to provide a reference. These hooks provide easy access to DGND, GND−BAT, AGND and GNDOD.

Table 13. MEASUREMENT TEST POINTS

Designator	Measurement
VREG	Output of the band−gap reference regulator in the Ezairo 8300
VBAT	Output voltage of the connected battery/chosen voltage source
VDDIF	Output of the interface charge pump
VDDO2, VDDO3	Voltage reference of the DIO2,3 domains
VBATOD	Voltage for the audio output driver
1V25	Output of 1.25V LDO
SPI	Enables probing of the SPI lines while communicating with non−volatile memories
VMIC	Output of the microphone voltage regulator
VBAT−I	Current measurement pin. Place a DMM across these two pins in current mode to measure the current consumption of the whole Ezairo 8310 device. Keep shorted otherwise. Can be used as an enable pin.

Indicator LEDs

The on−board J−Link debugger has a green LED indicator connected on P111 of the Renesas MCU.

APPENDIX A

HEADERS, CONNECTORS AND SCHEMATICS

This topic contains useful tables describing the headers on the Ezairo 8310 HDB, the connectors present on the Ezairo 8300 EVB, and schematic drawings of the Ezairo 8310 HDB for your reference.

Headers on the Ezairo 8310 HDB

This section contains a list and description of all headers present on the HDB, shown in the “List of Headers on the Ezairo 8310 HDB” table (Table 14).

Table 14. LIST OF HEADERS ON THE EZAIRO 8310 HDB

Designator	Description
SENSE	Used for connecting the sense voltage to the Promira
COMM−GND	Used for connecting the Promira ground to the HDB ground
EXT−PSU	Used for connecting an external power supply
PSU−SEL	Used to select power source for VBAT, to power Ezairo 8310
I2C	Used for connecting an I^2C device to communicate with Ezairo 8310
VBAT−I	Current measurement header. Keep shorted in normal operation.
VDC−BIAS	Connects VREG to the analog audio inputs to provide DC bias. BIAS0/1/2/3 need to be connected as well.
BIAS	Part of the DC biasing circuit used for the analog audio inputs. Short the header that corresponds to the input being biased.
C−BYP0/1/2/3	Used to bypass the DC blocking capacitor on the analog inputs from the RCA jacks/MICx headers
MIC0/1/2/3	Used to connect a 3 pin microphone input, typically a microphone
RESET	Can be shorted to reset the Ezairo 8300 module
MIC−GND	Determines the ground reference used by the audio inputs. Connect pins 2 & 3 to use GMIC; recommended when using a microphone. Connect pins 1 & 2 to use AGND; recommended for use with audio measurement instruments.
EXT−CLK	External clock source
RCVR0	Direct digital audio output 0. Allows connection via 0.1 inch headers to audio measurement devices when the output filters are enabled.
RCRV1	Direct digital audio output 1. Allows connection via 0.1 inch headers to audio measurement devices when the output filters are enabled.
FILTEN0	Enables the analog output filter for analog output 0
FILTEN1	Enables the analog output filter for analog output 1
OD0	Used to connect to the filtered analog output 0
OD1	Used to connect to the filtered analog output 1
VREG	Measurement header for VREG internal regulator
VMIC	Measurement header for VMIC internal regulator
VBATOD	Used for connecting an external power source to power the output drivers
VDDIF	Measurement header for VDDIF internal regulator/charge pump
VBAT	Measurement header for VBAT internal regulator
1V25	Measurement header for 1V25 voltage rail
REG−IN	Header for selecting the 5 V source for the 1.25V switching regulator. Short pins 2 & 3 to select J−Link 5V as the source, and short pins 1 & 2 to select USB 5V as the source.
SPI	Allows probing of the SPI signals
VDDO2,3	Measurement header for VDDOx internal regulator
VDD02/3−S	Used for selecting source for VDDO reference for each VDDO domain. Short pins 1 & 2 to select VDDIF as the source. Short pins 3 & 4 to select VBAT as the source.
DIO1/2/3	Each of these headers contains all of the DIO pins associated with the corresponding VDDOx domain.
DEBUG−EN	Enables debug of the Ezairo 8300 via the Renesas MCU and USB−C connection

Ezairo 8300 EVB Connectors

The “List of Connectors on the Ezairo 8300 EVB” table (Table 15) lists all connectors present on the EVB, and the purpose of each.

Table 15. LIST OF CONNECTORS ON THE EZAIRO 8300 EVB

Connector	Description
J2	6−pin mini−DIN connector used for communicating with serial I^2C devices, such as the Promira
J1	16mm battery holder
OD0	RCVR0 audio output via header
OD1	RCVR1 audio output via header
J10	USB−C connector used to communicate with the Ezairo 8310 via onboard J−link
J11	TC2030−IDC connector for programming firmware into the Atmel MCU. Intended for manufacturing use.
RCVR0	Header for unfiltered RCVR0 output
RCVR1	Header for unfiltered RCVR1 output
MIC0/1/2/3	Analog input headers, corresponding to the appropriate input on the Ezairo 8310
JLINK	20−pin header used to connect the J−Link debugging device

Schematics

This section contains the schematic diagrams for the Ezairo 8310 HDB, shown in the “Power Supply and Communications Schematics” figure (Figure 3), the “DUT Schematics” figure (Figure 4), and the “Debug Interface Schematics” figure (Figure 5).

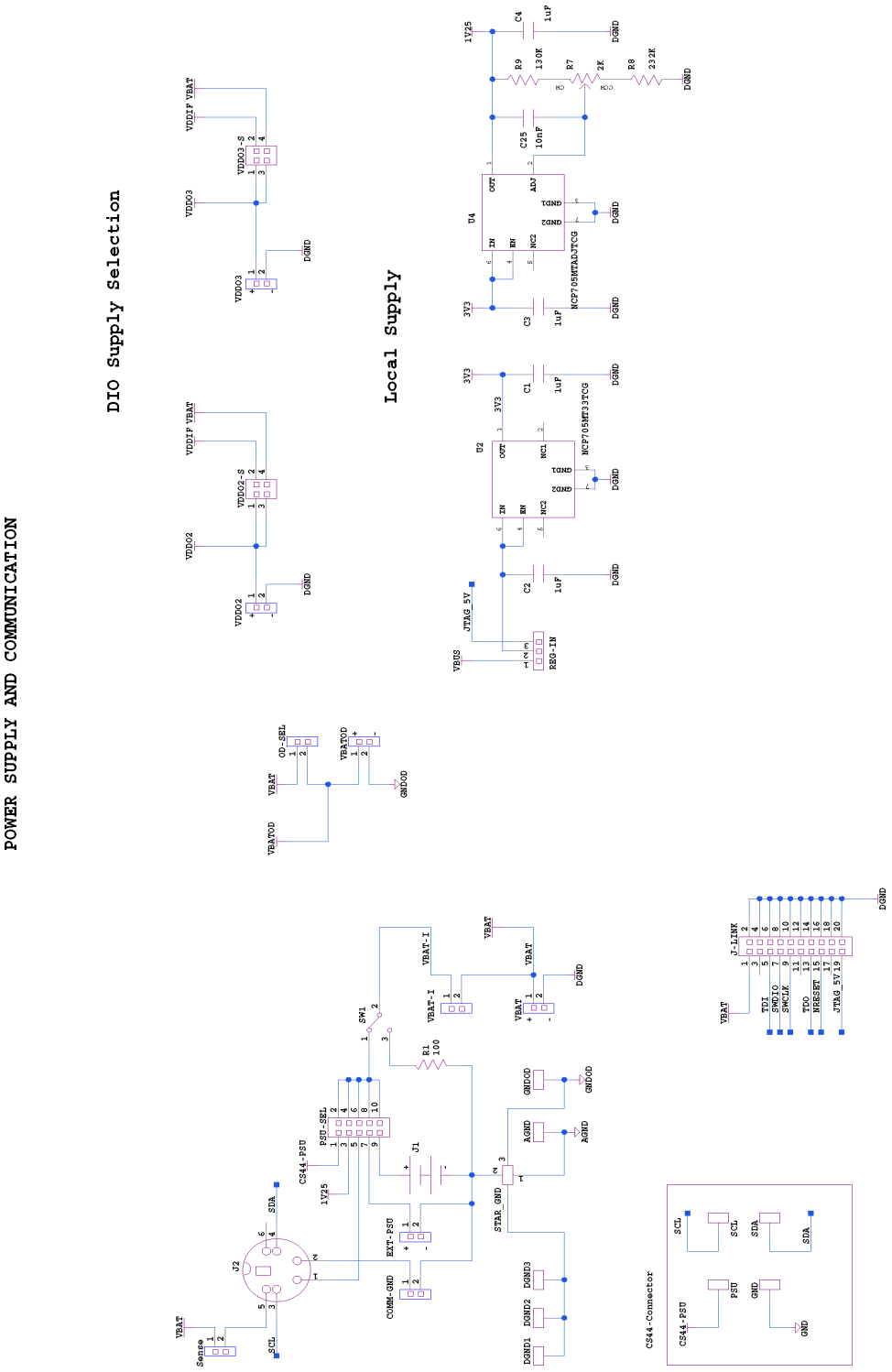

Figure 3. Power Supply and Communications Schematics

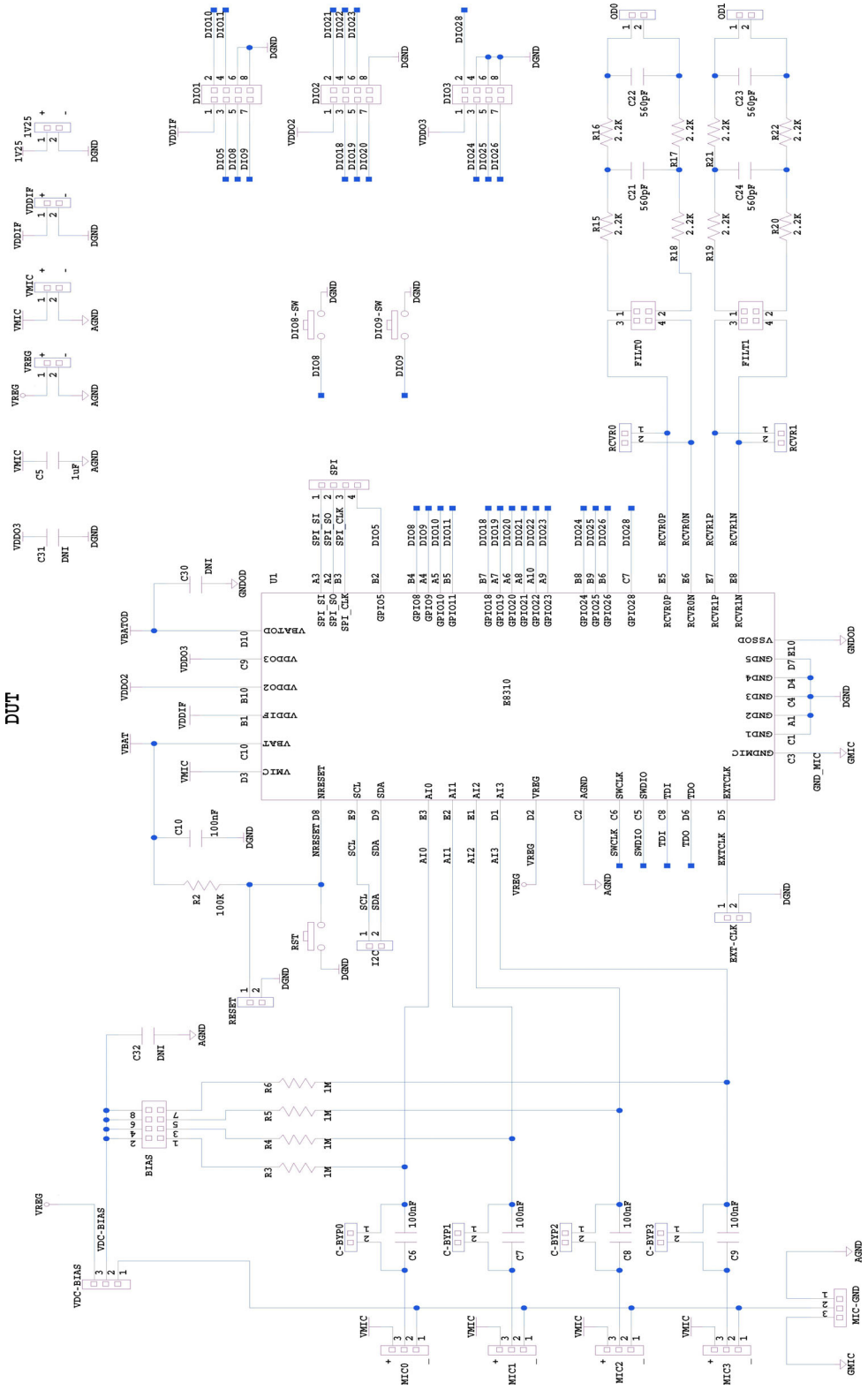

Figure 4. DUT Schematics

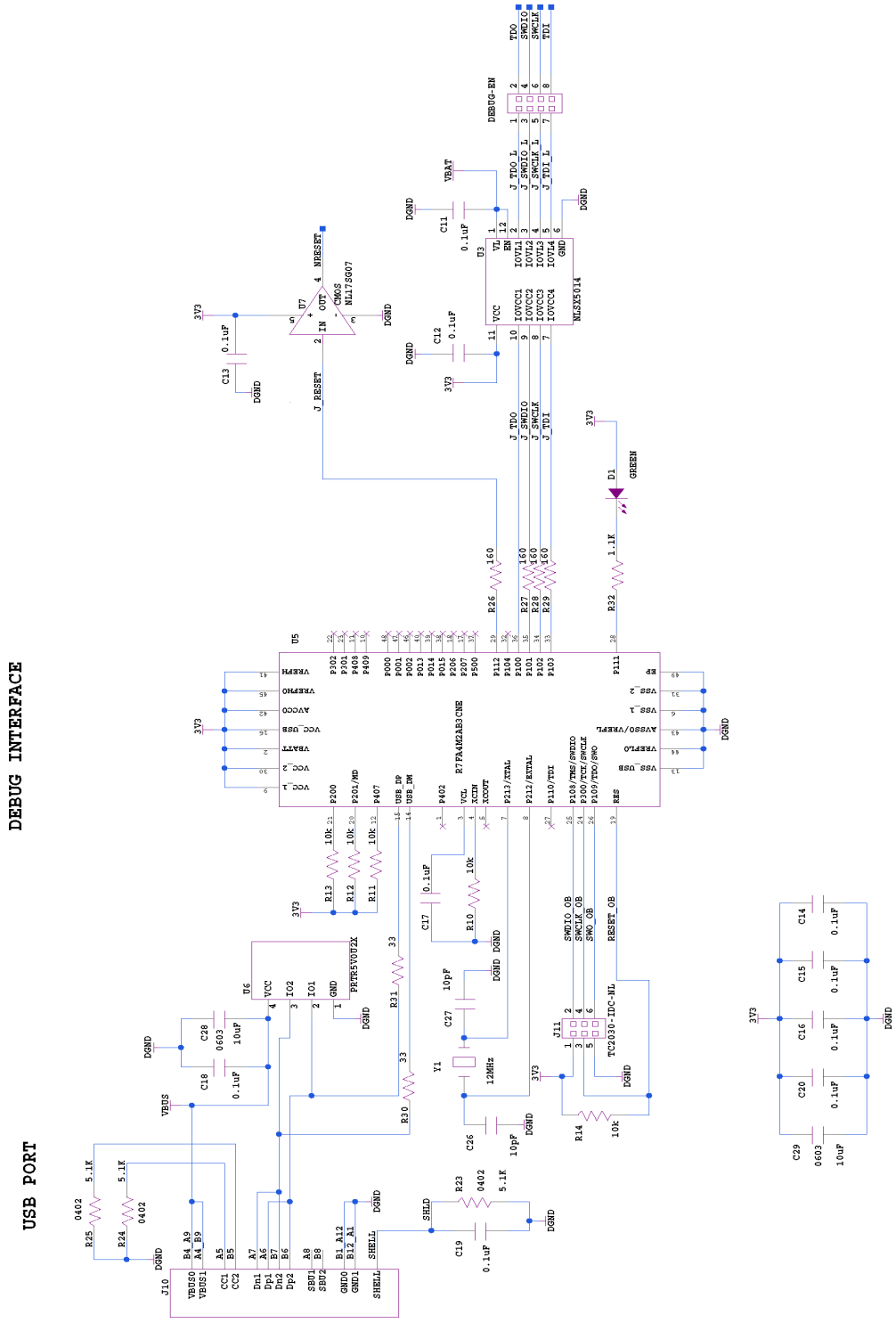

Figure 5. Debug Interface Schematics

ADDITIONAL INFORMATION

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