NCS35011 Evaluation Board User's Manual

NCS35011EVK

Introduction

This user's manual provides information regarding the configuration and method to test the NCS35011 IC. The evaluation board serves as a demonstration of NCS35011 general functionality. NCS35011 manages lithium−ion batteries from 3 to 5 cells in series with accurate battery indication through 3 to 5 LED outputs. Each cell in the battery pack is monitored for an over−voltage (OV) and under−voltage (UV) condition. Upon detecting an over−voltage, the ODI pin will assert indicating a fault condition and stay asserted until the fault is cleared. During an under voltage condition, the UDI pin will also assert indicating the fault but will have a pulse width that is pre−set in the protector. Both OV and UV detections have a hard coded pre−set delay time before fault indication.

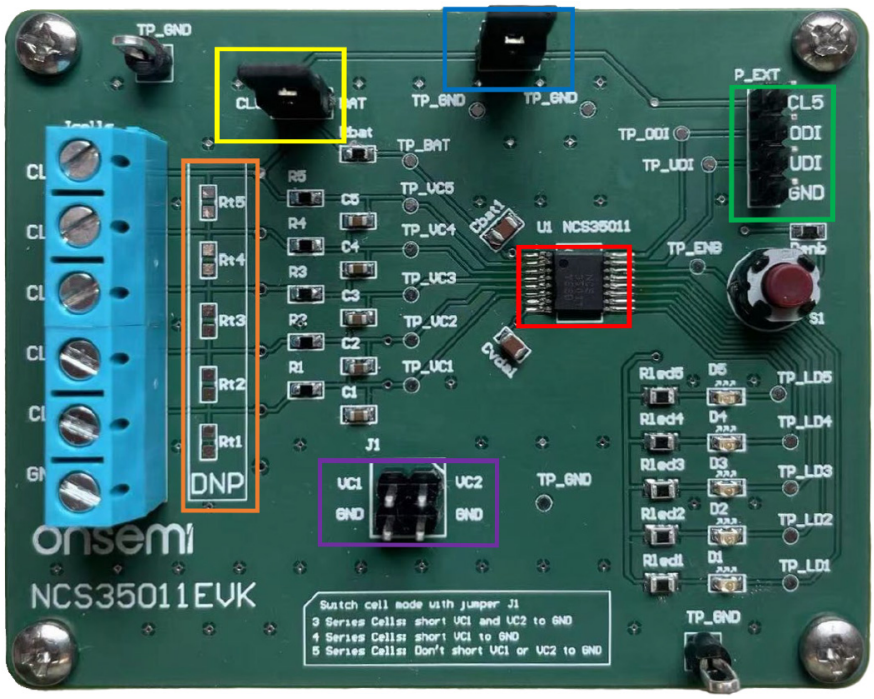

Figure 1. NCS35011 Evaluation Board

Features

- Over−Voltage (OV) and Under−Voltage (UV) Detection
- Protection for 3, 4 and 5 Series Cells
- State of Charge (SoC) Indication with High Voltage Tolerant LEDs for 3, 4, and 5 LED Options
- Configurable Fault Outputs (Push−Pull or Open Drain Active High or Low)
- High−Accuracy Voltage Measurement ±5 mV
- Low Power Consumption I_{CC} = 4 μA
- Input BAT Voltage Range 4 V to 25 V, Tolerant to 65 V for Increased Immunity to Surge
- Extended Junction Temperature Range to 125°C

Quick Start

Recommended Setup

Before beginning, the following setup is needed:

- DC power supplies to generate the battery cell voltages.
- A single DC power supply and five SMD (Rt1−Rt5) or external test resistors to generate the voltage divided cell voltages.
- Two external Pull−up resistors for UDI and ODI pin open−drain configuration test.
- Function generator to generate the cell level over voltage or under voltage.
- Oscilloscope.
- Digital Multi−meter.

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Board Setup

Step 1:

Identify the NCS35011 configurations. Depending on the IC trim, a different **J1** (see Purple boxed area in Figure 1) configuration may be required to short the corresponding VC pins to GND to create the 3, 4, or 5 series cells test mode.

Step 2:

Identify the NCS35011 ODI and UDI pin configurations. If IC is configured as Open−drain, external pull−up resistors are needed to connect between CL5 and ODI/UDI (see Green boxed area in Figure 1). It is recommended to limit the UDI and ODI current less than 5 mA.

Step 3:

Jcells jumper is the connector for external power or battery connection. Battery cell voltages can be generated through multiplier DC power supplies or SMD 0603 resistors Rt1 – Rt5 (see Orange boxed area in Figure 1) to create the voltage divided cell voltages.

Step 4:

JBAT jumper (see Yellow boxed area in Figure 1 allow user to measure the quiescent current into the IC BAT pin; J0 jumper (Blue boxed area) allow user to measurement current through all the LEDs.

Step 5:

SMD test points (TP_BAT, TP_VC5, TP_VC4, TP_VC3, TP_VC2, TP_VC1, TP_GND, TP_LD1, TP_LD2, TP_LD3, TP_LD4, TP_LD5, TP_ENB, TP_UDI, and TP_ODI) allow user to probe and measure each IC pins voltage. Refer to the schematic and layout diagrams found in Figure 2 and Figure 3 respectively as needed.

SCHEMATIC & LAYOUT DIAGRAMS

Schematic Diagram

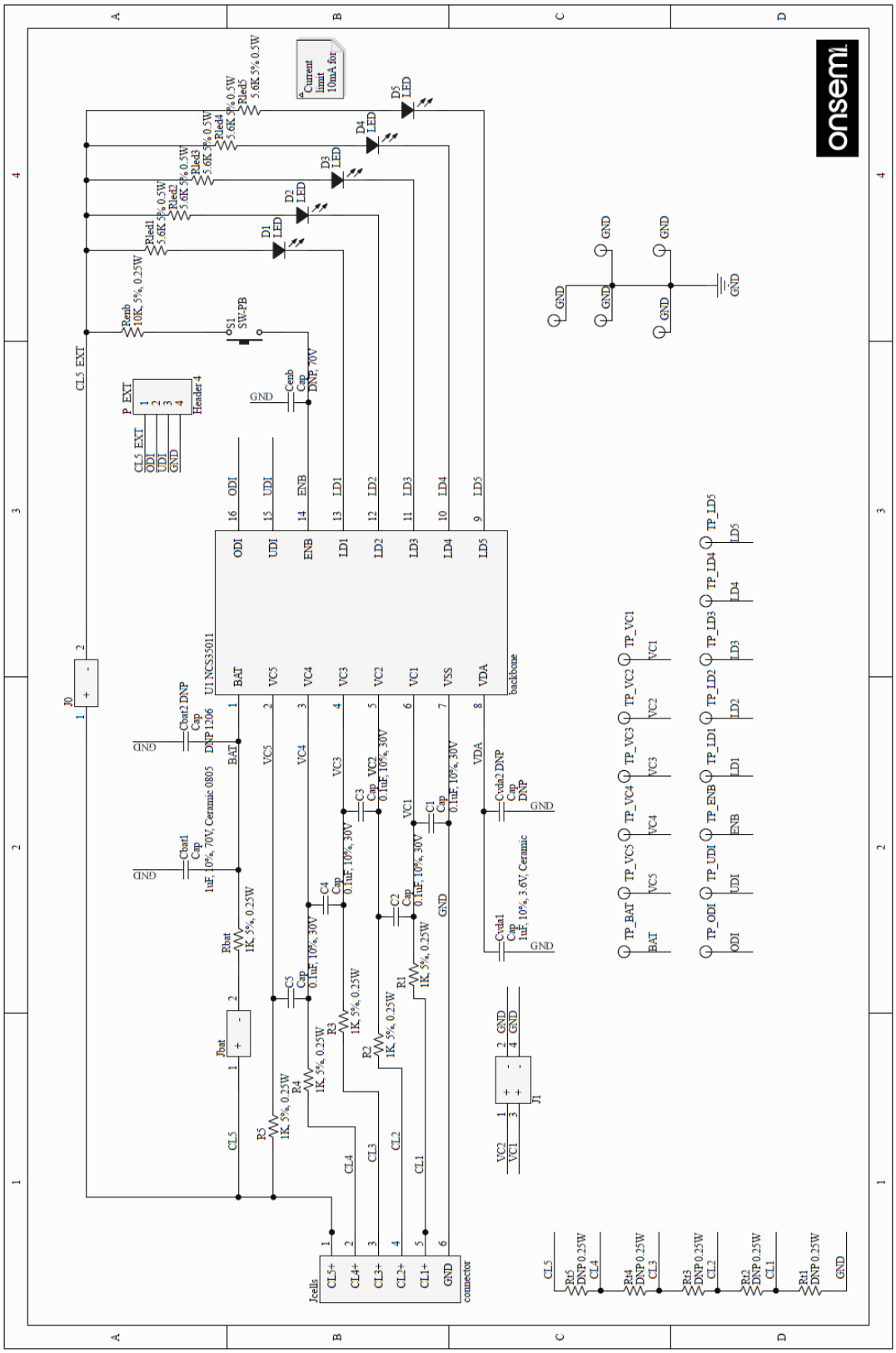

Figure 2. NCS35011 Evaluation Board Schematic

Layout Diagram

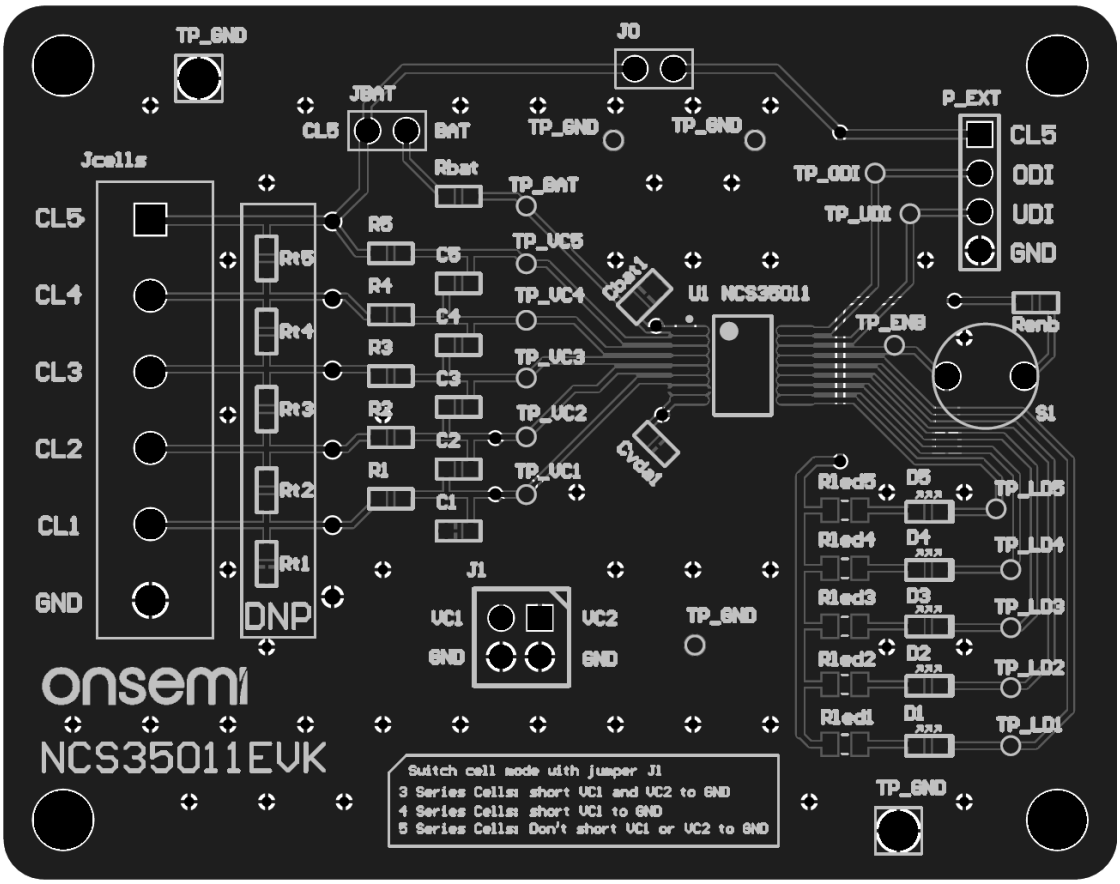

Figure 3. NCS35011 Evaluation Board Layout

Table 1. BILL OF MATERIALS

Quantity	Designator	Part Number	Value	Footprint
1	U1	NCS35011		TSSOP16
1	S1	MCR08MT1G	Switch	SW−PB
5	D1−5	APTD1608LZGCK	Green LED	0603
5	C1−5	Capacitor	0.1 μF 35 V	0603
1	Cbat1	Capacitor	0805 70/100 V	0805 / 1206
1	Cvda1	Capacitor	1 μF 6 V	0603
6	R1−5, Rbat	Resistor	1 k	0603
1	Renb	Resistor	10 k	0603
5	Rled1−5	Resistor	12 k	0805
1	Jcells	TB002−500−06BE	Terminal block	
1	JBAT, J0	Header Connector	1 x 2	
1	J1	Header Connector	2 x 2	
1	P_EXT	Header Connector	1 x 4	
2	TP_GND	Test Loop		Through Hole

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