150 W PFC Solution with Drain ZCD Sense Evaluation Board User's Manual

EVBUM2843/D

SPECIFICATION

onsemi's Device	Application	Input Voltage	Output Power	Topology	I/O Isolation
NCP1623ADR2G NCP58920	Above 75 W power supply, Smart phone super charger, PD3.1 adapter	90 Vac to 264 Vac	150 W	Boost	Non−Isolated

	Output Specification
Output Voltage	250 V @ low line (LL), 390 V @ high line (HL)
Nominal Current	0.6 A @ LL, 0.384 A @ HL
Max Current	0.6 A @ LL, 0.384 A @ HL
Min Current	zero

Efficiency	95.7% @ 90 Vac & full load
Protection	UVP, OVP, OCP, OVS, OTP
PCBA Size	51 mm x 47 mm x 21 mm

CIRCUIT DESCRIPTION

This evaluation board user's manual describes a 150 W PFC using NCP1623A without aux. winding, universal AC input, two stage follower boost output for smart phone super charger, NB adaptor and general power supply supporting 140 W PD3.1, and low cost, high efficiency, and low standby power are essential.

The featured PFC solution uses VSFF PFC controller with boost topology, the PN is NCP1623ADR2G, also uses **onsemi**'s iGaN, NCP58920 with internal gate drive. This evaluation board user's manual provides the complete circuit schematic details, PCB layout, inductor specification and BOM for 150 W PFC solution, and also some key waveforms for reference. In additional, this design also provides some design tips for feedback, ZCD network, PFC inductor design, bulk capacitance evaluation and some layout guideline.

Two stage follower boost mode can increase the efficiency at low line, the AC line transition voltage can be easily designed through ZCD network and two stage output can also be designed through feedback network.

There is no auxiliary winding for ZCD detection in this design, ZCD and valley detection is done by resistor divider from drain voltage, it also provides valley switching on at different load.

PFC ON/OFF can be controlled via DIS pin in SOIC8 version or Vcc on/off on TSOP6 and SOIC8 version both.

KEY FEATURES & PERFORMANCES

- Universal AC Input Range (90 − 264 Vac)
- Valley Synchronized Frequency Fold−back (VSFF)
- CRM/DCM Operation with Valley Switching
- Skip Mode for Light Load Regulation
- Sleep Mode with Low Current Consumption (SOIC8 Only)
- DIS Pin for On/Off Control (SOIC8 Only)
- Two Stage Follower Boost Output
- w/o Auxiliary Winding ZCD Sense
- High Operation Frequency up to 300 kHz
- iGaN Used
- OVP, UVP, OCP, OVS, OTP Protection
- PCBA Size: 51 mm x 47 mm x 21 mm

BOARD PHOTOS

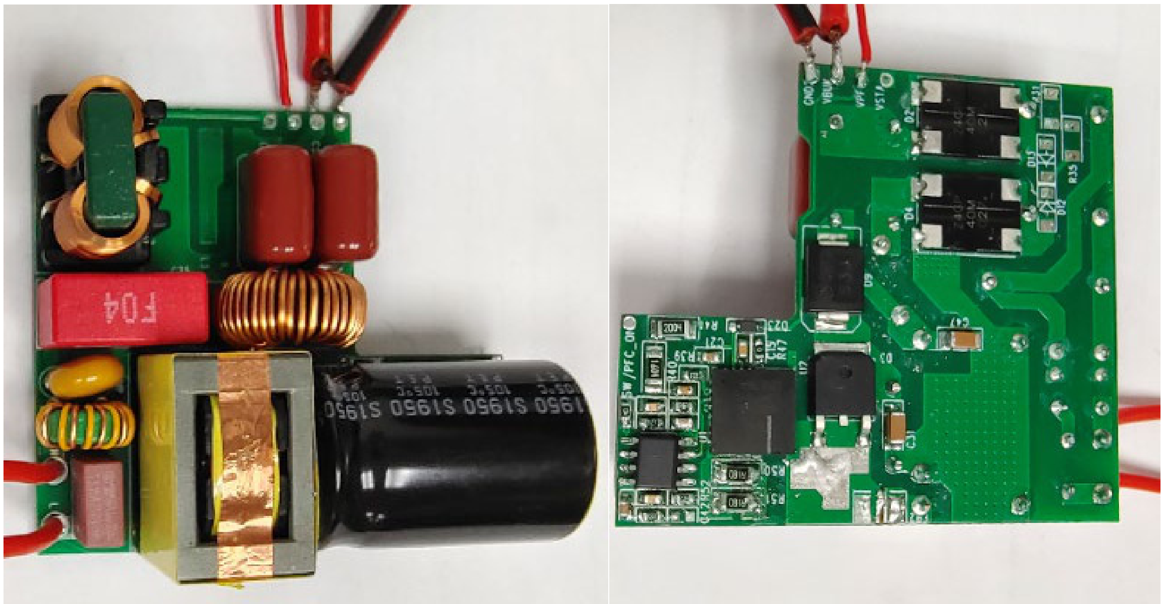

Figure 1. 150 W EVB with SO8 controller

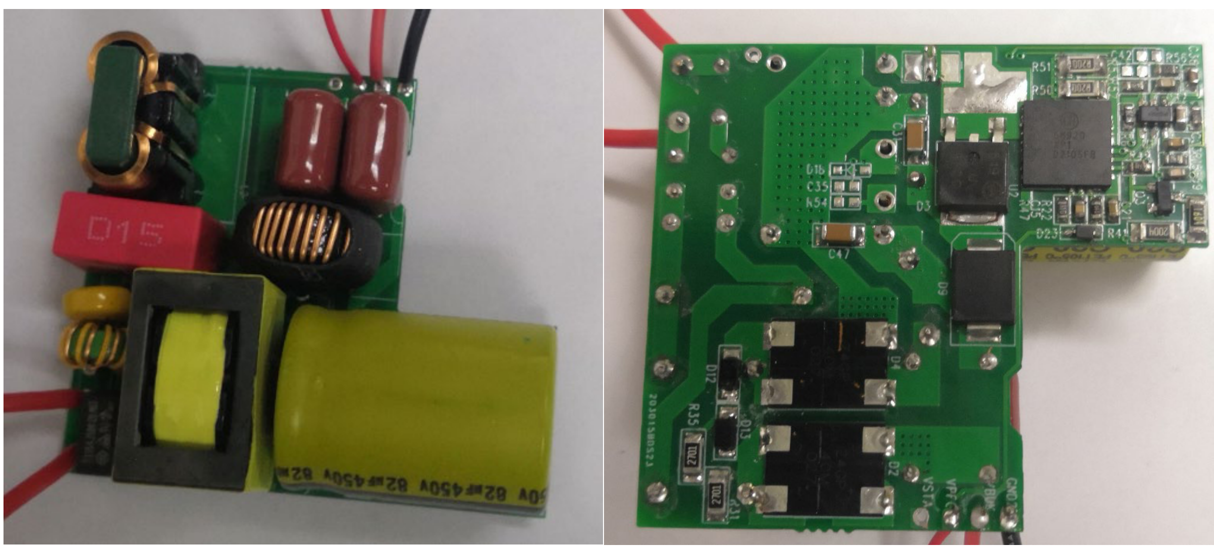

Figure 2. 150 W Reference Design Example with TSOP6 Controller

EVB DESIGN (SOIC8) CIRCUIT SCHEMATIC

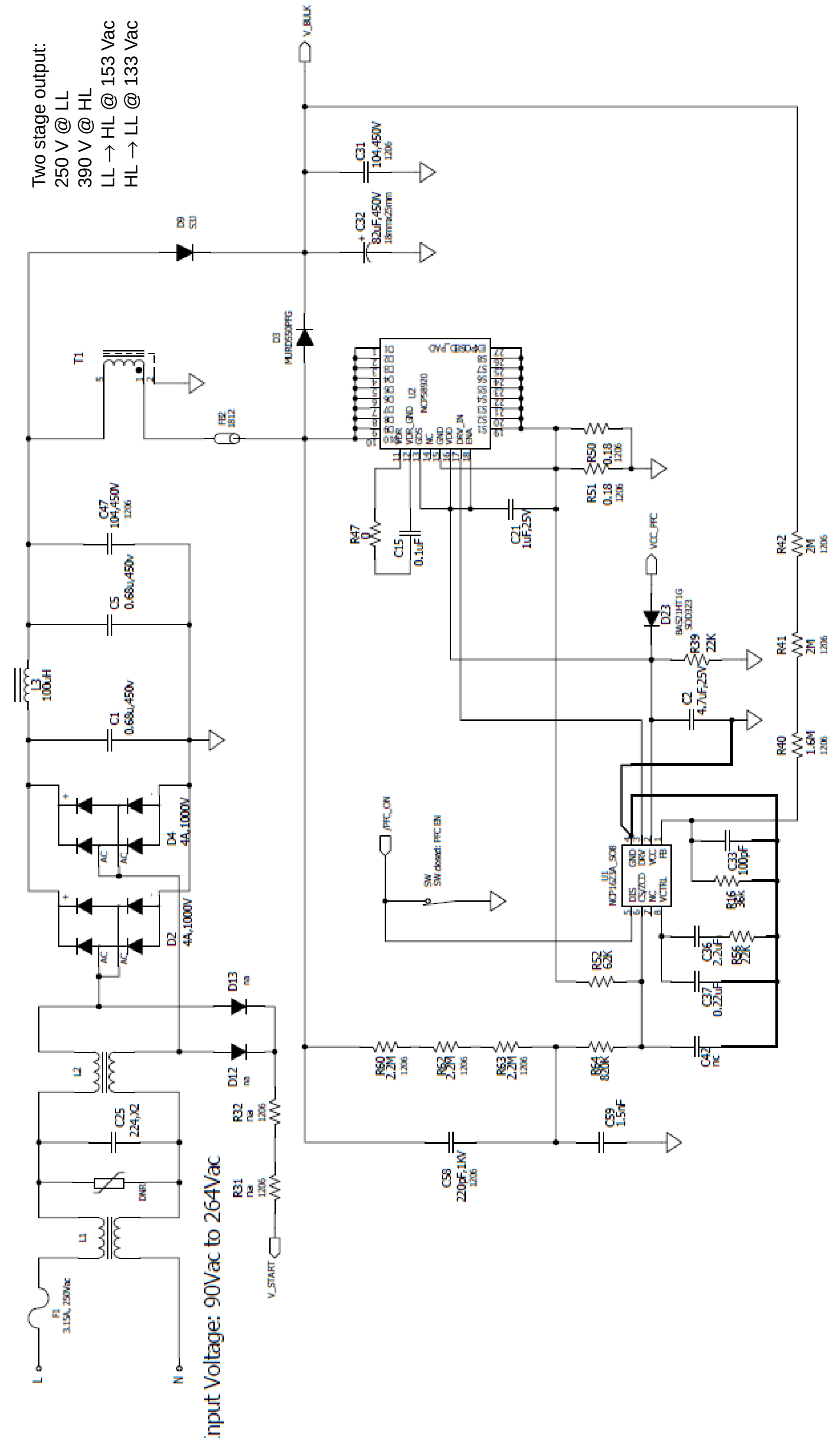

Figure 3. 150 W EVB Schematic with SOIC8 Controller

REFERENCE DESIGN (TSOP6) CIRCUIT SCHEMATIC

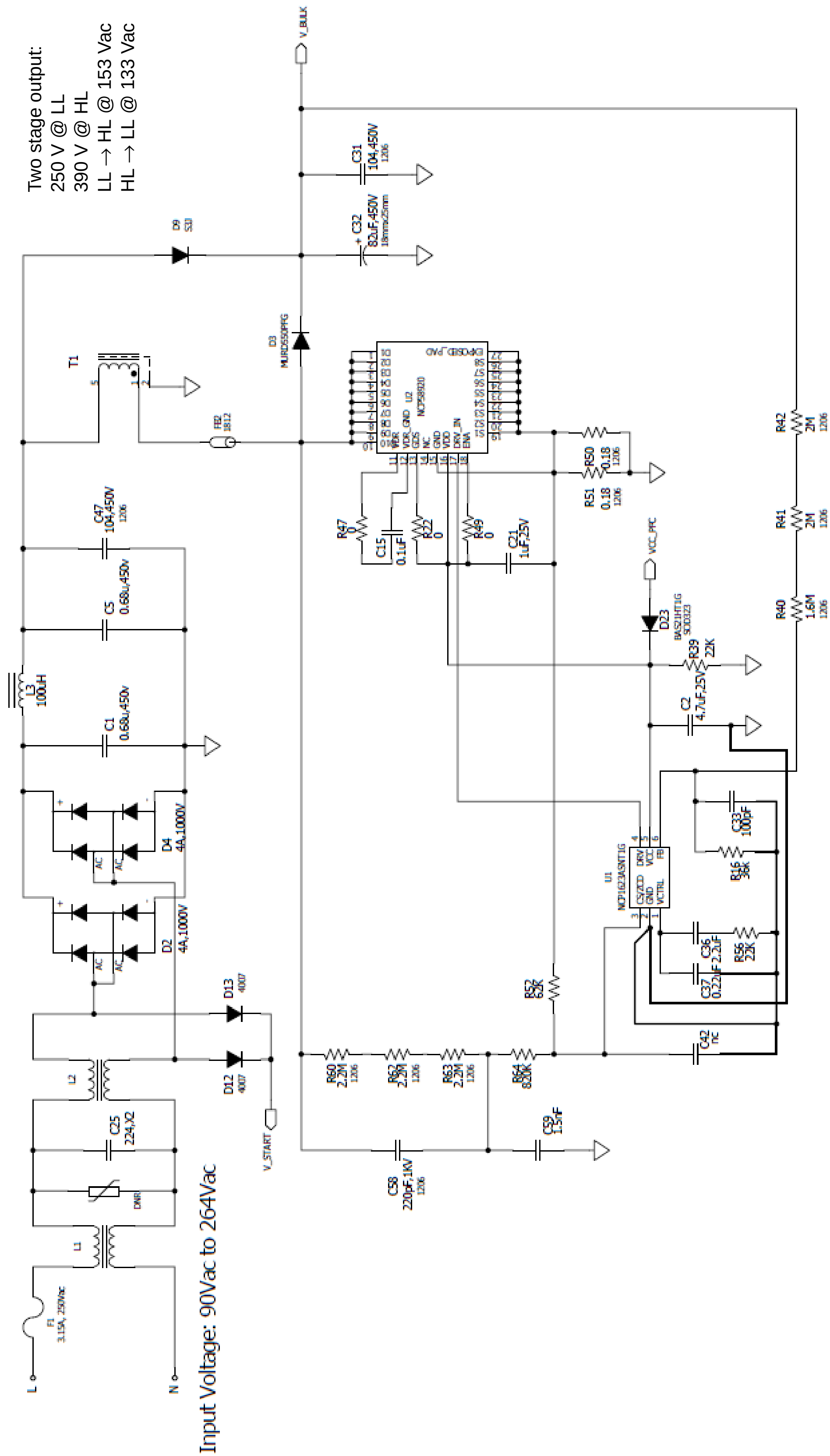

Figure 4. 150 W Reference Design Schematic with TSOP6 Controller

PCB

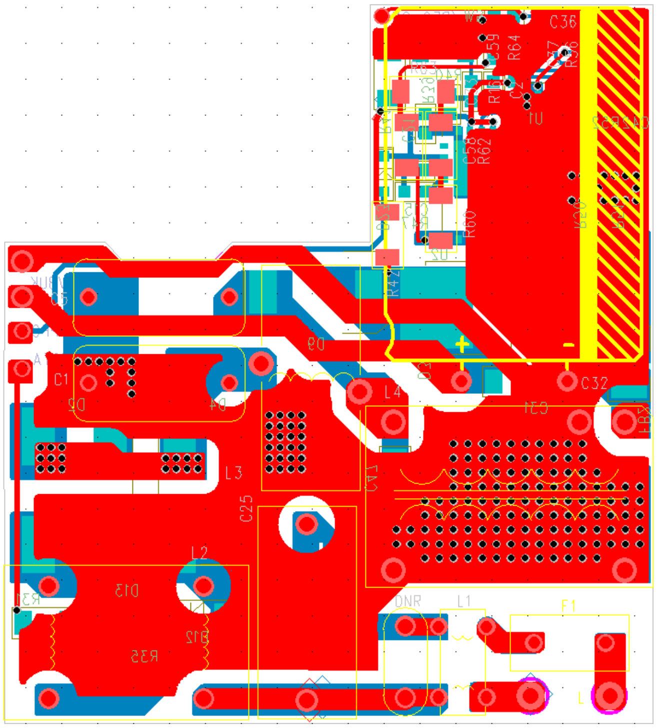

Figure 5. (Top), Top View of PCB, SOIC8

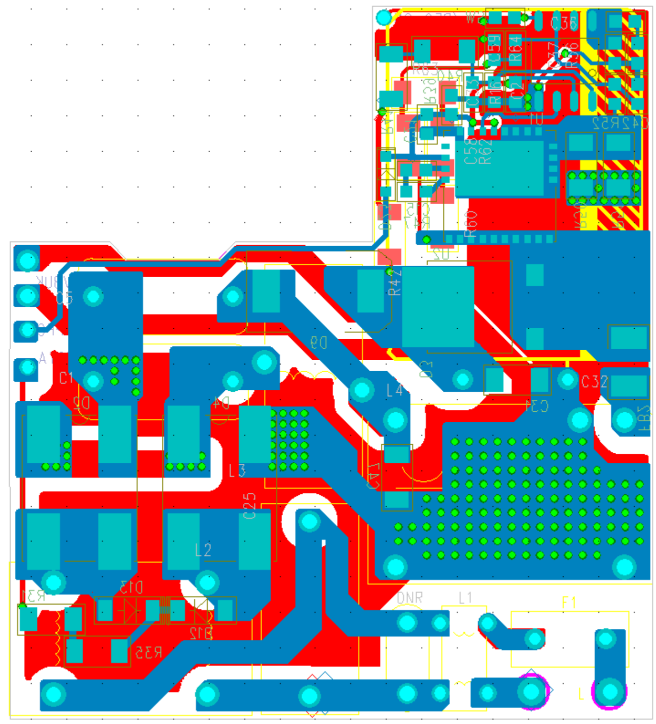

Figure 6. (Bottom), Bottom View of PCB, SOIC8

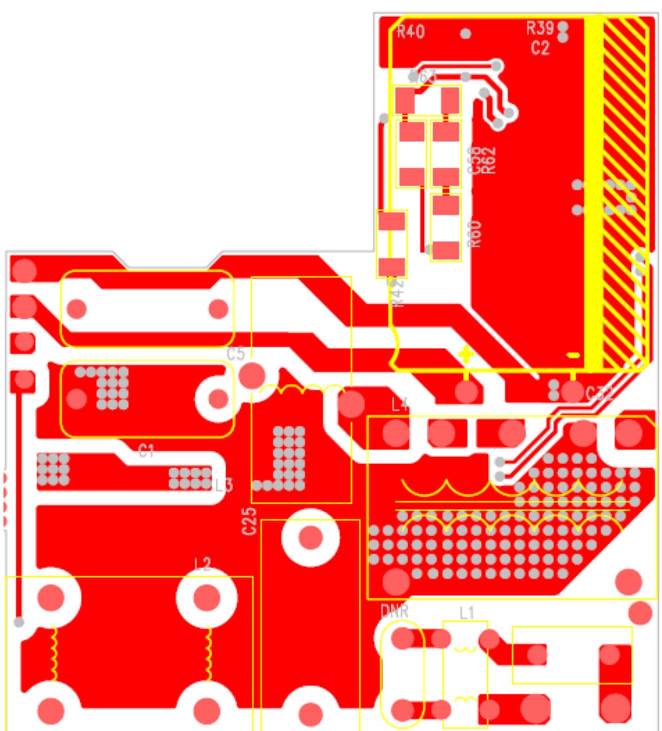

Figure 7. (Top), Top View of PCB, TSOP6

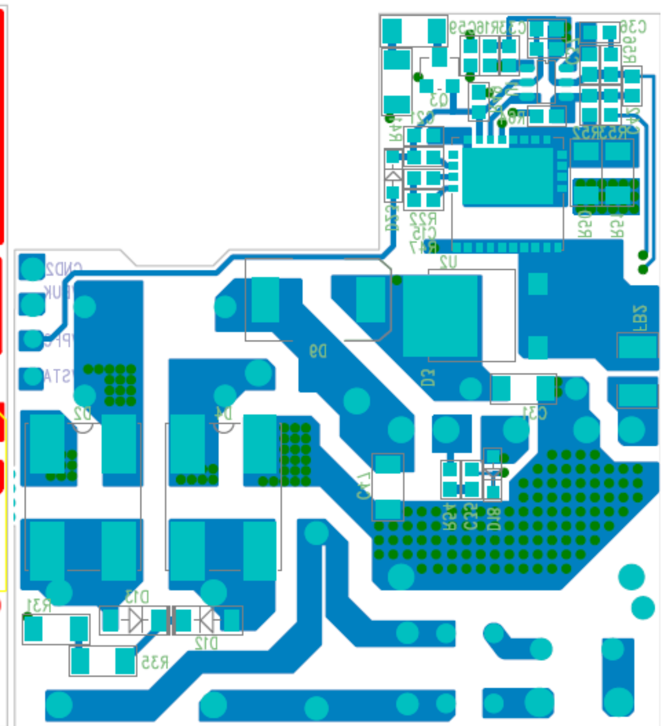

Figure 8. (Bottom), Bottom View of PCB, TSOP6

PFC INDUCTOR SPECIFICATION

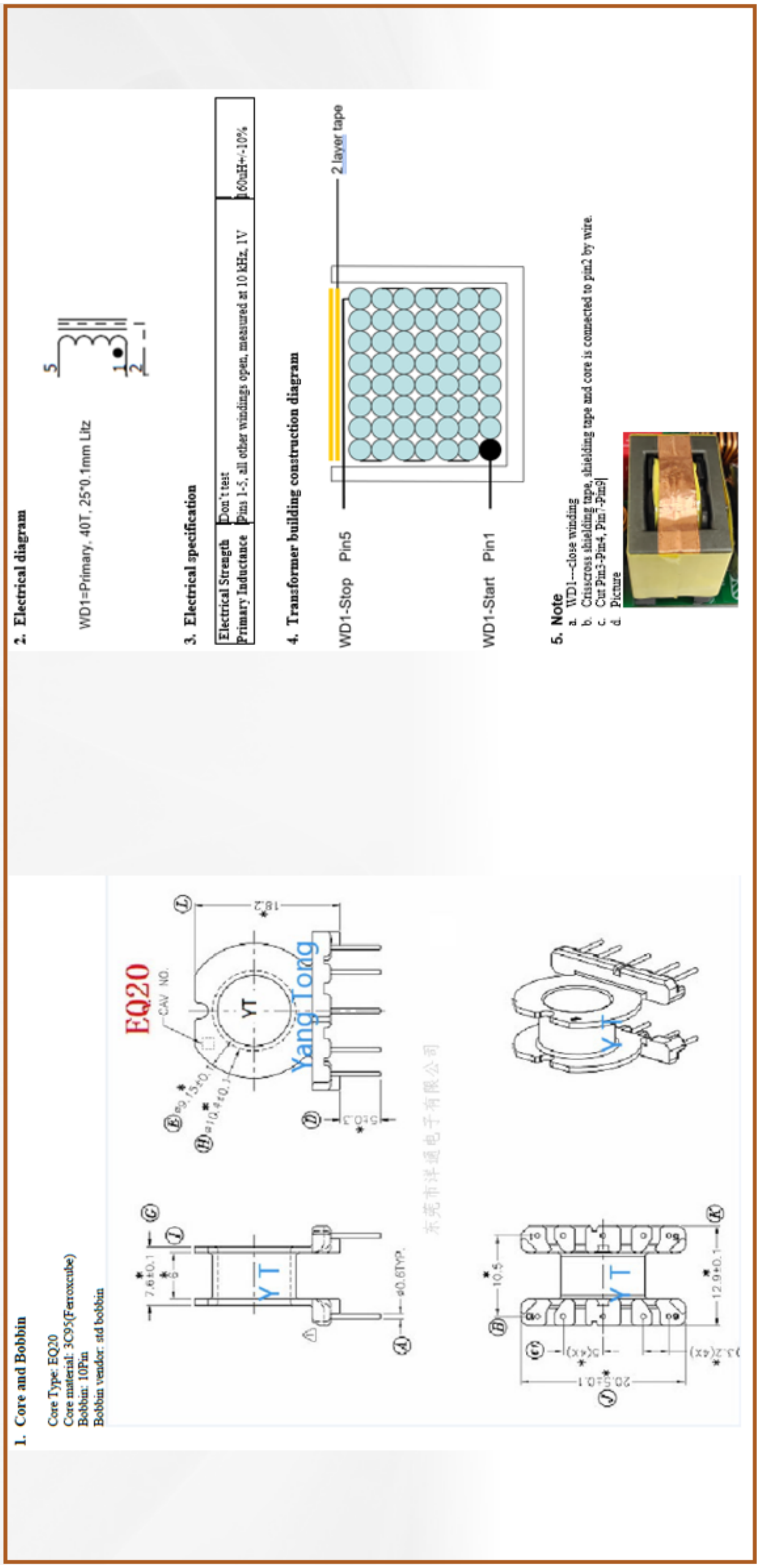

Figure 9. PFC Inductor Specification

Efficiency and PF Curve

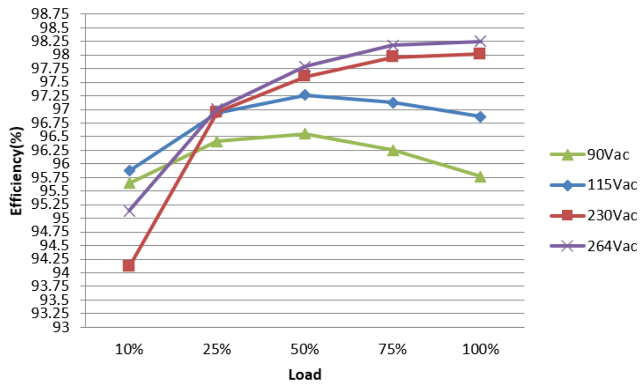

Figure 10. Efficiency Curve by Load

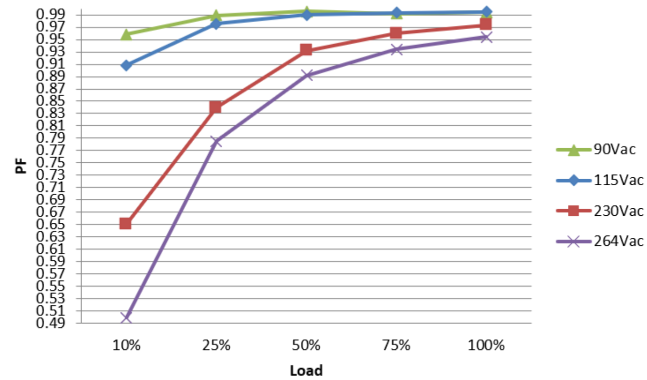

Figure 11. PF Curve by Load

Normal Operation Waveforms

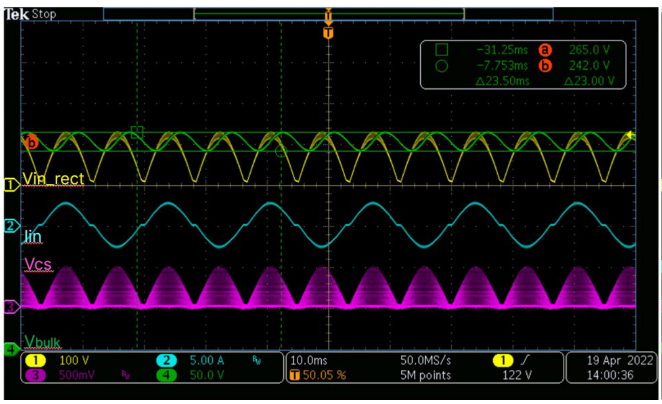

Figure 12. Full Load (0.6 A) @ 90 V_{AC}

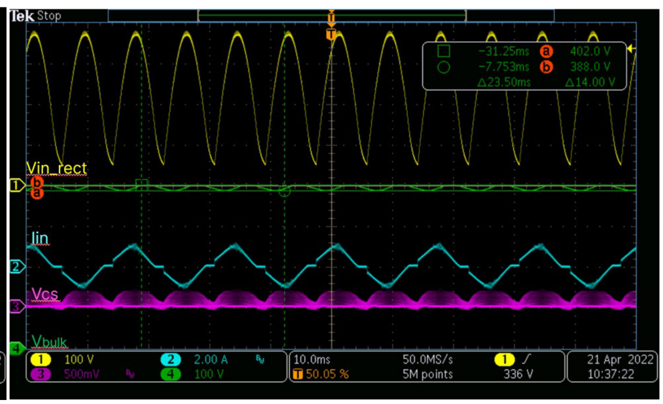

Figure 13. Full Load (0.6 A) @ 264 V_{AC}

Line Transition

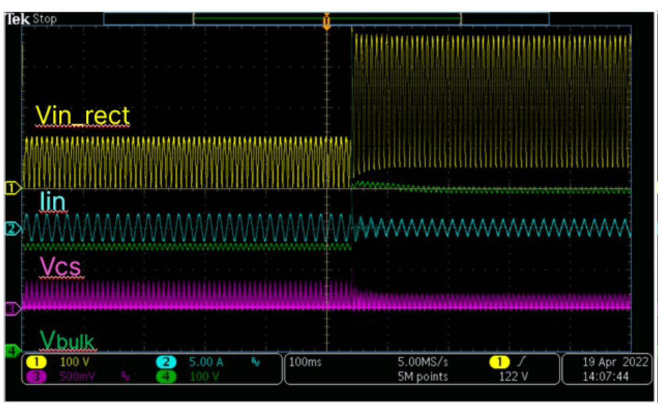

Figure 14. 90 V_{AC} → 264 V_{AC} @ 0.384 A

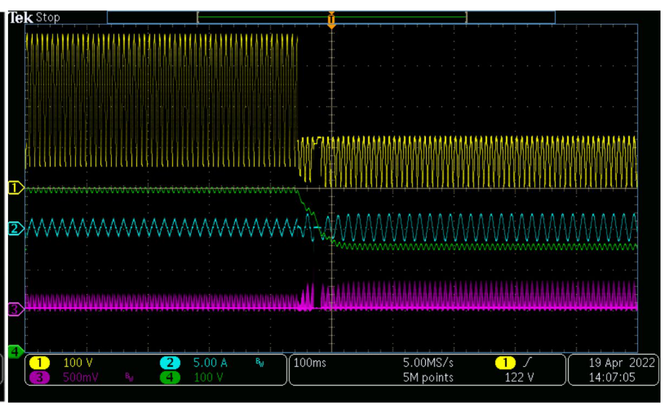

Figure 15. 264 V_{AC} → 90 V_{AC} → 264 V_{AC} @ 0.384 A

Load Transition

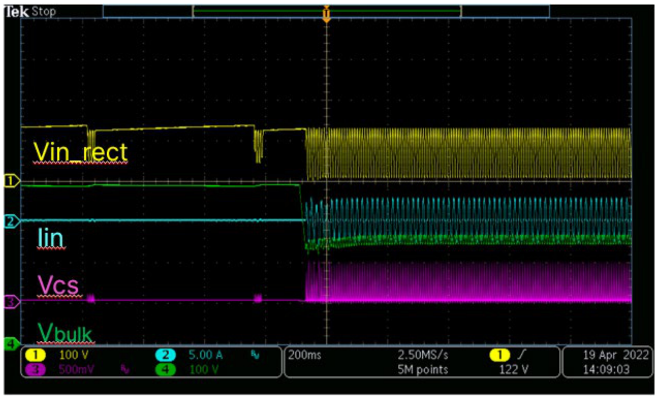

Figure 16. 0 A → 0.6 A @ 264 V_{AC}

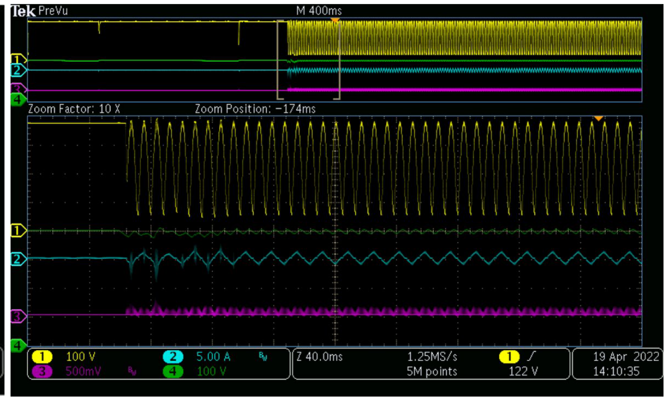

Figure 17. 0 A → 0.384 A @ 264 V_{AC}

Valley Switching

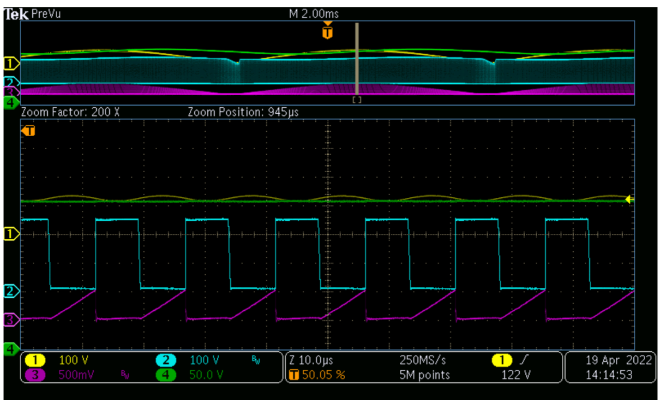

Figure 18. Full Load @ 90 V_{AC}

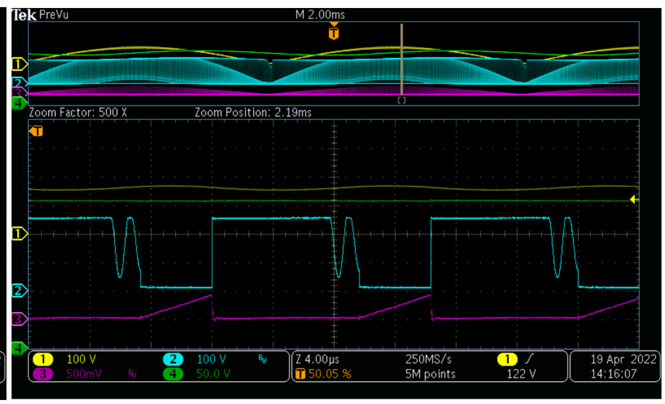

Figure 19. Full Load @ 115 V_{AC}

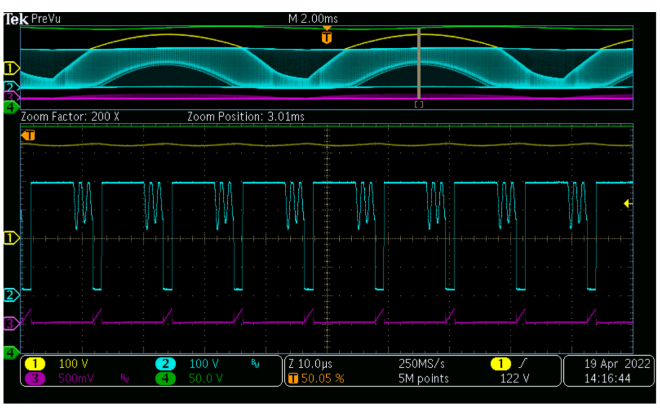

Figure 20. Full Load @ 230 V_{AC}

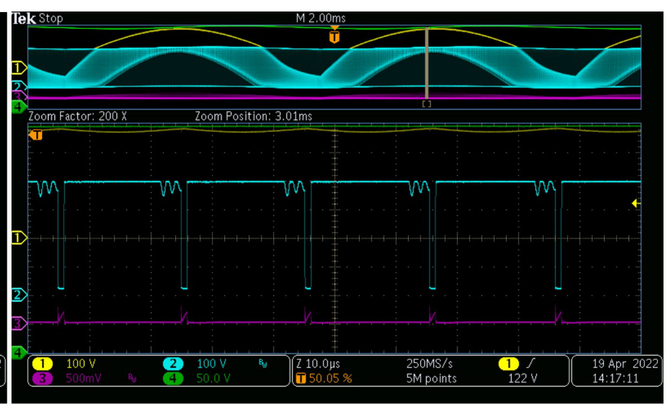

Figure 21. Full Load @ 264 V_{AC}

BOM

Table 1. BOM

Item	Qty	Reference	Type	Part Name	Package	MFR	Value	Description
1	1	T1	PFC Inductor	EQ20	TH type	Custom	EQ20, 160 μH	EQ20, 10Pin bobbin
2	1	C15	Ceramic Capacitor	/885012206095	603	Wurth	0.1 μF	Capacitor, Ceramic, 50 V, 10%
3	1	C37	Ceramic Capacitor	/885012206073	603	Wurth	0.22 μF	Capacitor, Ceramic, 25 V, 10%
4	2	C1 C5	Film Capacitor	ECWFD2W684Q	THT, 10mm, 13 mm x 6 mm x 12 mm	Panasonic	0.68 μ,450 V	Film capacitor
5	1	C59	Ceramic Capacitor	/885012206084	603	Wurth	1.5 nF	Capacitor, Ceramic, 50 V, 10%
6	1	C33	Ceramic Capacitor	/885012206077	603	Wurth	100 pF	Capacitor, Ceramic, 50 V, 10%
7	2	C31 C47	Ceramic Capacitor	C3216X7T2W104K	1206	TDK	104, 450 V	Capacitor, Ceramic, SMD, 5%
8	1	C21	Ceramic Capacitor	/885012206076	603	Wurth	1 μF, 25 V	Capacitor, Ceramic, 25 V, 10%
9	1	C36	Ceramic Capacitor	/885012106018	603	Wurth	2.2 μF	Capacitor, Ceramic, 16 V, 10%
10	1	C58	Ceramic Capacitor	C3216C0G2J221J	1206	TDK	220 pF, 630 V	Capacitor, Ceramic, SMD, 5%
11	1	C25	X2 Capacitor	/890324024002	THT, 12.5 mm, 15 mm x 7 mm x 12 mm	Wurth	224, X2	X2 capacitor, Safety standard approved, 10%
12	1	C2	Ceramic Capacitor	C1608X5R1E475K080AC	603	TDK	4.7 μF, 25 V	Capacitor, Ceramic, 25 V, 10%
13	1	C42	Ceramic Capacitor	Std	603	Wurth	nc	Capacitor, Ceramic, 50 V, 10%
14	2	D2 D4	Bridge Rectifier	Z4GP40MH	Z4PAK	ZOWIE	4 A, 1000 V	Bridge Rectifier, 1000 V, 4 A
15	1	D9	Rectifier	S3J	SMC	**onsemi**	3 A, 600 V	General Rectifier
16	1	DNR	Varistor	820573011	TH	Wurth	10D471K	Varistor, 10D471K
17	2	D12−13	Standard Rectifier	na	SOD123FL	std	0.8 A, 600 V	General Rectifier, 0.8 A, 600 V
18	1	D23	Switching Diode	BAS21HT1G	SOD323	**onsemi**	0.2 A, 250 V	Switching diode, SMD
19	1	FB2	Ferrite Bead	742792511	1812	Wurth	120 ohm @ 100 M, 3 A	120 ohm @ 100 MHz
20	1	L1	Common filter	Custom	TH	Custom	30 μH	T type, 8*4*3 NiZn core
21	1	L2	Common filter	SQ1212	TH type	Std	10 mH	CM Filter, SQ1212, 8*11 pin instance
22	1	F1	Fuse	std	Axial lead	std	3.15 A, 250 Vac	Micro Fuse, 3.15 A/250 V
23	1	D3	Ultrafast Rectifier	MURD550PFG	DPAK	**onsemi**	5 A, 520 V	Ultrafast Rectifier, 5 A, 520 V
24	1	U2	Driver GaN	NCP58920	QFN26	**onsemi**	650 V	Driver GaN, 150 mohm
25	1	U1	PFC Controller	NCP1623ADR2G	SO8	**onsemi**		PFC controller, SO8

Table 1. BOM (continued)

Item	Qty	Reference	Type	Part Name	Package	MFR	Value	Description
26	1	L3	Toroidal Line Choke	T050125−100Uh−070−L	TH type	Yiruisen	100 μH	KoolMu Toroidal, Die13 mm, DCR 30 mohm
27	1	R47	Resistor	Std	603	Std	0 Ω	Resistor, Chip, 1/10 W, 1%
28	2	R39 R56	Resistor	Std	603	Std	22 kΩ	Resistor, Chip, 1/10 W, 1%
29	1	R16	Resistor	Std	603	Std	36 kΩ	Resistor, Chip, 1/10 W, 1%
30	1	R52	Resistor	Std	603	Std	62 kΩ	Resistor, Chip, 1/10 W, 1%
31	1	R64	Resistor	Std	603	Std	820 kΩ	Resistor, Chip, 1/10 W, 1%
32	2	R50−51	Resistor	ERJ8BSFR18V	1206	Panasonic	0.18 Ω	Resistor, Chip, 1/2 W, 1%
33	1	R40	Resistor	Std	1206	Std	1.6 MΩ	Resistor, Chip, 1/4 W, 1%
34	3	R60 R62−63	Resistor	std	1206	std	2.2 MΩ	Resistor, Chip, 1/4 W, 1%
35	1	R41	Resistor	Std	1206	Std	2 MΩ	Resistor, Chip, 1/4 W, 1%
36	1	R42	Resistor	std	1206	std	2 MΩ	Resistor, Chip, 1/4 W, 1%
37	2	R31−32	Resistor	std	1206	std	na	Resistor, Chip, 1/4 W, 1%
38	1	C32	Electrolytic electrolytic capacitor	420BXW82MEFR18X25	18 mm x 25 mm	Rubycon	82 μF, 420 V	size:18 mm x 25 mm
39	1	SW	Resistor	std	603	std	0	switching, replaced by 0 ohm

DESIGN DESCRIPTION

PFC ON/Off Control

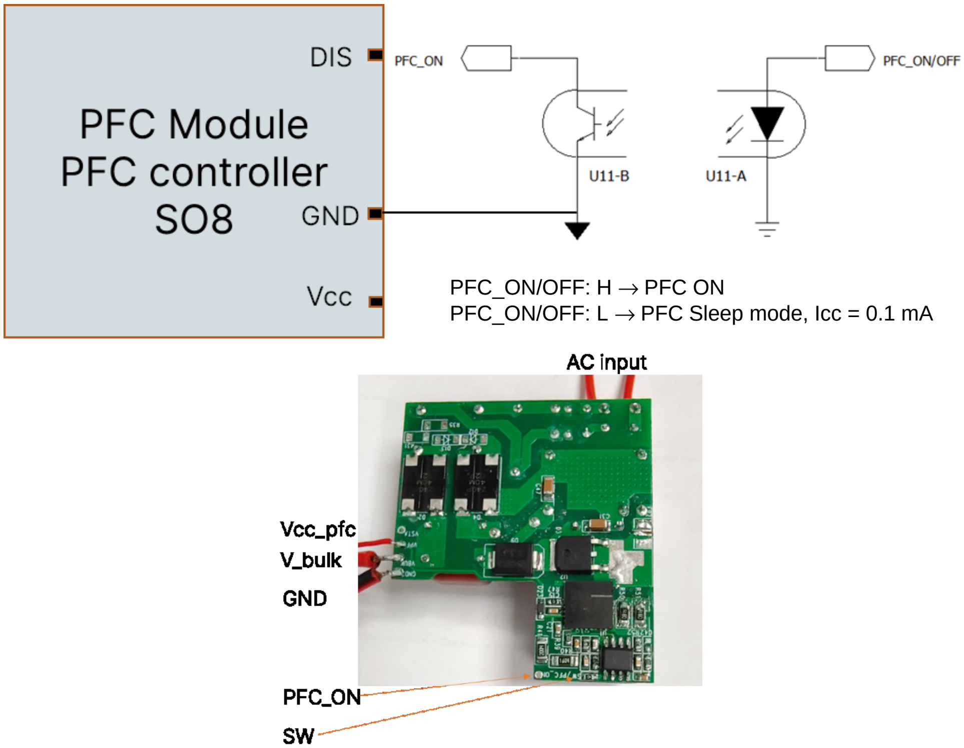

Figure 22. EVB (SOIC8) DIS Pin Control

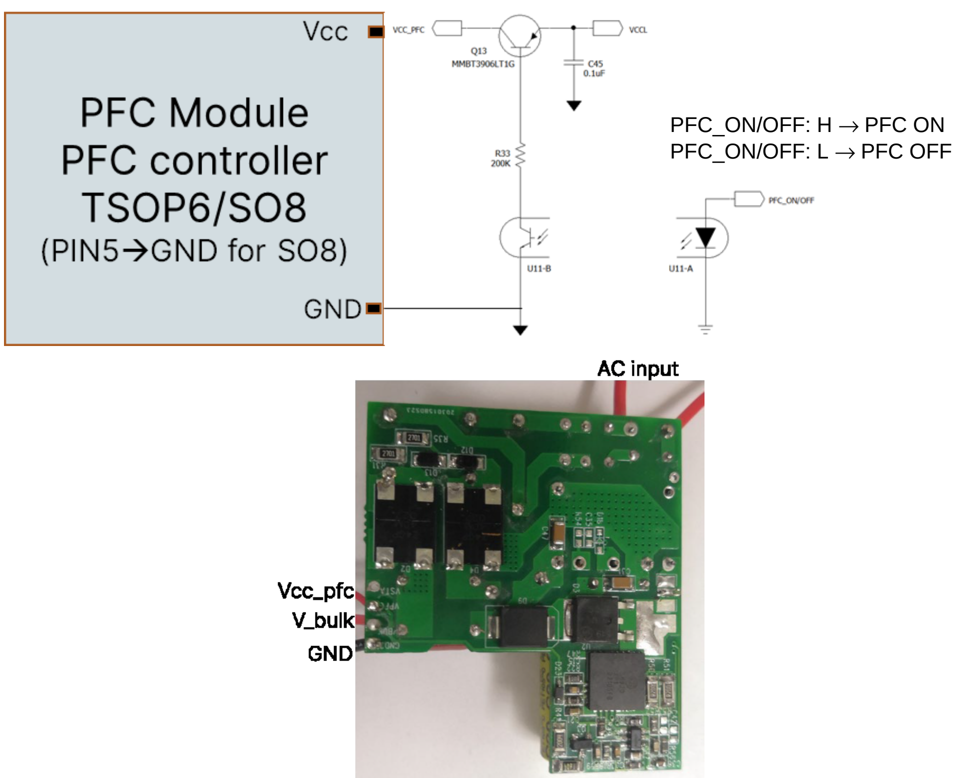

Figure 23. Reference Design Vcc ON/OFF

Feedback Network Design

NCP1623A provides two stage boost follower at low line (LL) and high line (HL), one a internal 25 μA current source is inserted to FB pin and follow through Rlow resistor to reduce output voltage, so the following two equations can be got:

Assume: Vo = 250 V @ LL, Vo = 390 V @ HL
Rup − up divider resistor
Rlow − low divider resistor

$$(2.5 / Rlow - 0.025) \times Rup = 250\ V - 2.5\ V \quad \text{(eq. 1)}$$

$$(2.5 / Rlow) \times Rup = 390\ V - 2.5\ V \quad \text{(eq. 2)}$$

Calculate equation (1), (2), get Rup = 5.6 M, Rlow = 36 k

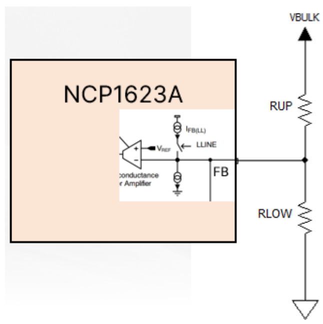

Figure 24.

ZCD Network Design

Assume Vbulk = 250 V @ LL

Set line transition point is 154 Vac, 154 x 1.414 = 217 V, so there is enough margin to work very well at Top of sin wave

LL to HL transition detection threshold is 1.8 V

Rcs1 + Rcs1d + Rcs2 < 10 M

(large power loss on this resistor while too small resistance, but there is too small bias current it will impact the precise of line transition point if too larger resistance)

According to selecting line transition voltage and detecting threshold to get the following equation:

$$\frac{R_{CS1} + R_{cs1d}}{R_{cs2}} = \frac{154 \times 1.4141 - 1.8}{1.8} = 119.98$$

So R_{cs1d} = 119.98 x $R_{cs2} - R_{cs1}$

Set R_{cs1} = 6.6 M (three 2.2 M resistor in series), R_{cs2} = 62 k

Get R_{cs1d} = 119.98 x $R_{cs2} - R_{cs1}$ = 839 k, so take R_{cs1d} = 820 k

verity Rcs1 + Rcs1d + Rcs2 = 7.482 M < 10 M

verity (Rcs1 + Rcs1d + Rcs2) / Rcs2 = 120.7, about 138 − 12.5%, no issue in actual test

Calculate C1, C2

Because external ZCD resistor divider uses high resistance, than parasitic capacitance on PCB will results in phase shift of ZCD voltage and ZCD detecting tolerance, so it must be compensated by external capacitor divider, the current through C1 and C2 must be equal, impedance divided ratio must be equal to capacitance divided ratio.

Get the following equation:

According to experience to select C1 = 220 pF, calculate C2 = C1 x (Rcs1 / (Rcs1d + Rcs2)) = 1646 pF, take 1500 pF

So final ZCD external component parameters:

Rcs1 = Rcs1a + Rcs1b + Rcs1c = 6.6 M

Rcs1d = 820 k

Rcs2 = 62 k

C1 = 220 pF (voltage rating: 400 V − 630 V)

C2 = 1500 pF (voltage rating: 50 V)

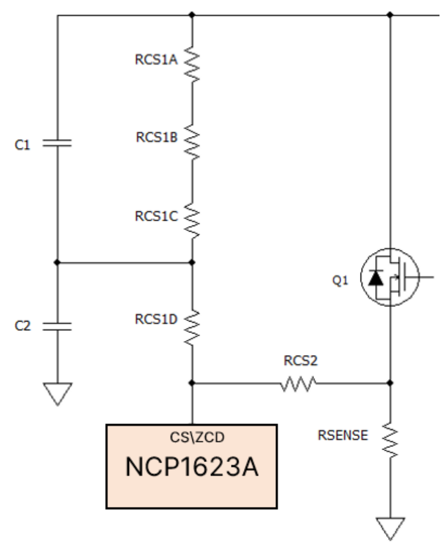

Figure 25.

PFC Inductor Design

Set Vbulk = 250 V @ LL

1. Dmax calculation
   Dmax = (Vo − Vin) / Vo = (90 x 1.414 − 250) / 250 = 0.491
2. Max Ton calculation (set min Fsw = 77 kHz @ 90 Vac and full load)
   Ton = (1000 / 77) x Dmax = 6.38 μS
3. Inductance calculation
   $$L = \frac{V^2_{ac\_min} \times T_{on}}{2 \times P_{in}} = \frac{90^2 \times 6.38}{2 \times 160} = 160\ (\mu H)$$
4. Max primary peak current and sense resistor calculation
   Ip = (Vdc_min x Ton) / L = 127 x 6.38 / 160 = 5.06 A, Rsense = 0.5 / 5.06 = 0.099 ohm, take 0.09 ohm
5. Inductor turns calculation (EQ20 core, Ae = 59 mm^2)
   Np = L x Ip / (ΔB x Ae) = 160 x 5.06 / (0.34 x 59) = 40 (Turns) (Delta Bmax = 0.34 T)

Bulk Capacitance Selection

Table 2.

FB SOVP Enter Voltage Ratio at Low Line, Ver. A	$K_{FB(SOVP-EN-LL)}$	$V_{FB(SOVP-EN-LL)} / V_{REF}$	108.5	110.0	111.5	%
FB SOVP Exit Voltage Ratio at Low Line, Ver. A	$K_{FB(SOVP-Ex-LL)}$	$V_{FB(SOVP-Ex-LL)} / V_{REF}$	106.5	108.0	109.5	%

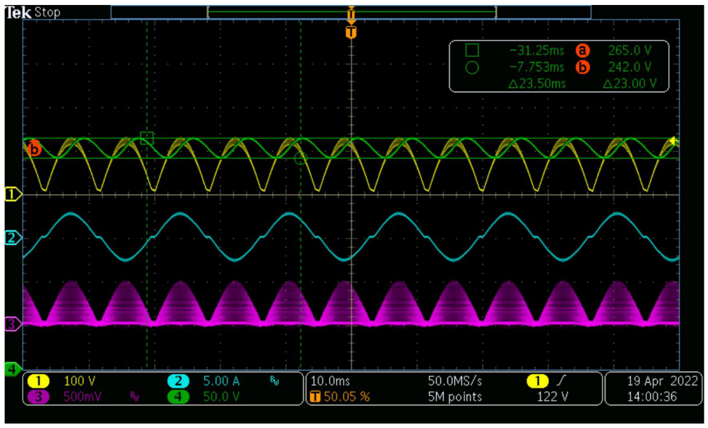

Figure 26.

1. The ripple voltage on FB pin is filtered by error amp and equal to reference voltage, so it will trigger SOVP while highest point of ripple is larger than 11.5% of this reference voltage
2. While output ripple peak−peak is large than 30 V − 31 V then it will trigger SOVP at low line
3. Because of lowest line frequency and enough margin, actual bulk capacitance and delivery power ratio is about 1:2, means that 200 W delivery power needs min 100 μF bulk capacitance at least

PCB LAYOUT GUIDANCE

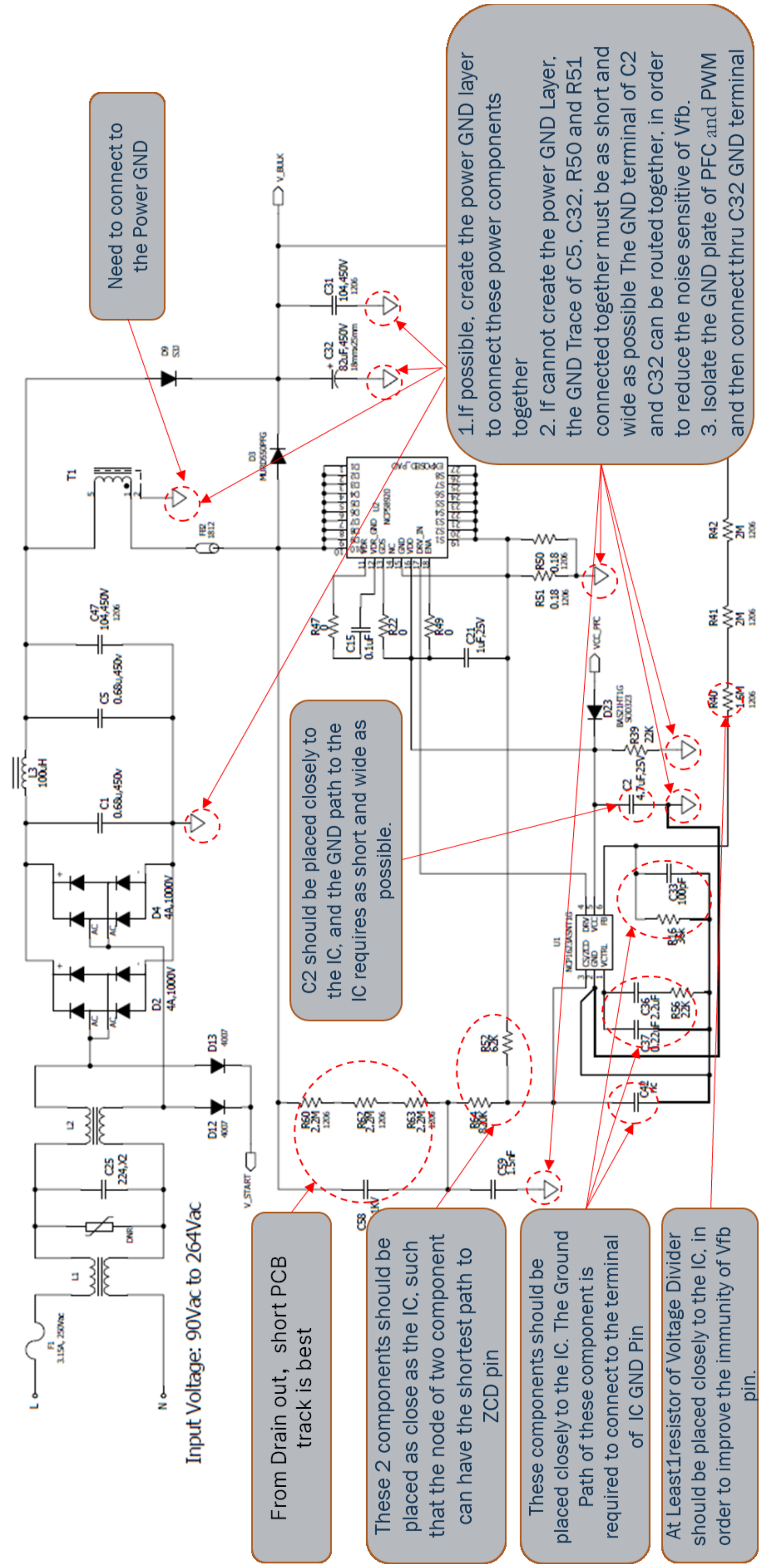

Figure 27.

REFERENCE

onsemi datasheet for NCP1623 and NCP58920
onsemi Design Notes DN05043

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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