NCN26010XMNEVB 10BASE-T1S MACPHY Evaluation Board User's Manual

EVBUM2832/D

Figure 1. Evaluation Board Photo

Introduction

The NCN26010XMNEVB is a PCB designed to allow customers access to **onsemi**'s NCN26010 SPI enabled 10BASE−T1S MACPHY. Its main purpose is to demonstrate the MACPHY's basic functionality and doubles as a lab tool to allow customers to develop their own embedded software drivers for the NCN26010 device.

Features

The NCN26010XMNEVB Eval board includes all circuitry to allow the board to act as a 10BASE−T1S MACPHY node, when connected to a host computer / MCU via SPI.

The eval board NCN26010XMNEVB, carrying the NCN26010 has two RJ45 connectors that allow attaching a twisted single pair data cable. For ease of use, standard cat 5 Ethernet cables can be connected to the RJ45 connectors. Note that only one pair (connected to pin 1 and 2) of the RJ45 connector is used.

The SPI connection can be done through a PMOD connector on the NCN26010 eval board, allowing the connection to MCU demo− and eval boards of various vendors. One example of such a Eval board is **onsemi**'s RSL10 BDK−GEVK.

When pairing the NCN26010XMNEVB with the NCN26010BMNEVB, users can connect the eval board to a Raspberry Pi single board computer (SBC).

For details on how this is done, please refer to the NCN26010XMNEVK eval kit users guide.

To allow monitoring of the SPI traffic, the EVB features a 0.1" pitched pin header that is easily accessible. This header could also be used to connect a logic analyzer, allowing tracing of the SPI signals while in full operation together with a (not supplied) Raspberry Pi or any other suitable host MCU or SBC. Users can also use this connector for connecting to host PCBs (3rd party MCU eval boards) that do not offer a PMOD connector.

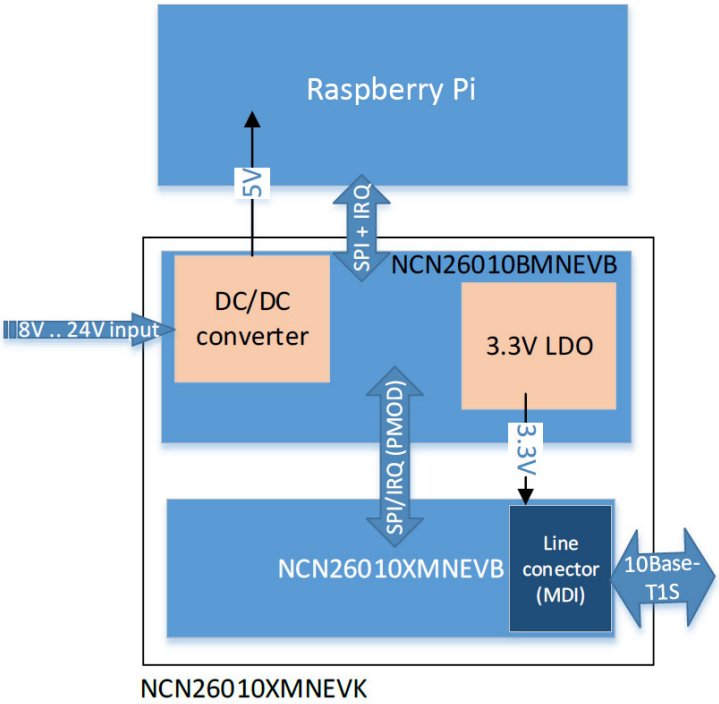

Figure 2. Evaluation Kit Simplified Block Diagram

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APPLICATIONS INFORMATION

To act as a communication node, the evaluation board needs a host computer to perform any network communication. The NCN26010XMNEVB performs the functions of a MAC (media access controller) and a PHY (physical layer) device.

The upper layer protocols need to be provided by software running on the host. The host will also have to handle the SPI communication between the MACPHY and the host, since the MACPHY operates as an SPI slave device.

In addition, the MACPHY provides an IRQn signal that signals new RX data and other events that need to be handled by the host.

Connectors and Jumper locations

The following picture shows the top view of the EVB:

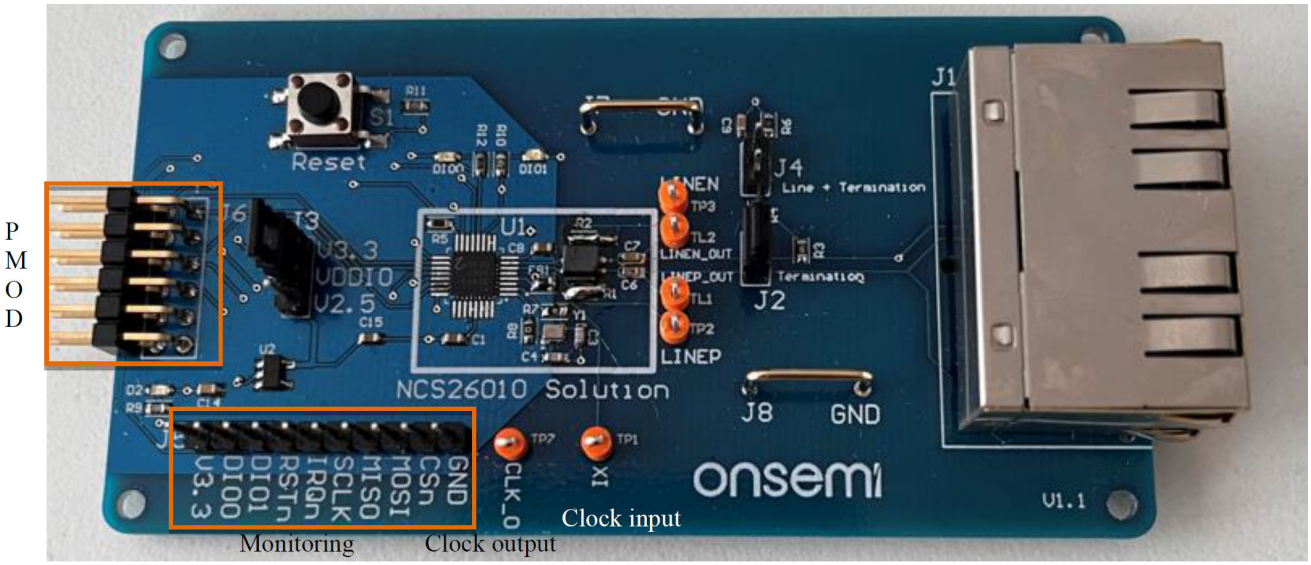


Figure 3. Evaluation Board – Top View

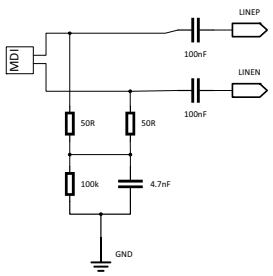
Power Supply, Test Points and Connectors

NCN26010XMNEVB needs a single 3.3 V power supply that can provide a peak current of at least 100 mA. Note that at full operation the board draws approx. 45 mA of current but has an inrush current of up to 100 mA at power on.

Power can be fed through the PMOD connector J6 or the edge connector J5.

Following is a list of all connectors and test points on the NCN26010XMNEVB evaluation board.

Table 1. CONNECTORS AND JUMPERS

Name on Board	Function	Comment
J1	Dual RJ45 SPE	These two connectors are used to connect standard Cat5 ethernet cables. Note that only the twisted pair connecting to pins 1 and 2 of the RJ45 connectors are used. Users can crimp their own cables by utilizing pins 1 and 2 of the RJ45 connectors. The two sockets are electrically connected to connecting multiple NCN26010 boards to build a larger network.
J2	Jumper to set termination	When closed, the board provides a 100 Ω termination resistor across the MDI terminal. Note that only the boards at both ends of the multidrop segment should have the termination resistor enabled
J3	Digital IO voltage selection	Use this jumper to select between a 3.3 V and 2.5 V VDDIO voltage. The eval board has a 2.5 V Voltage regulator to allow interfacing with MCUs that use 2.5 V IOs; set the jumper accordingly. Note that in any case, the Eval boards power supply will have to be 3.3 V
J4	Jumper to set Opt−BIN Termination  	When closed, adds a capacitor and a 100 kΩ resistor to ground. This jumper should only be set when J2 is set.
J5	SPI and IRQ debug/Monitoring	This port can be used to connect a logic analyzer, allowing to monitor the OA−Protocol on the SPI interface. It can also be used to interface to MCU boards that do not have a PMOD connector. The board can also be powered though this port. **When connecting the board via the PMOD (J6) connector, do not use J5 to power the board.** The pinout of J5 is detailed on the eval board.
J6	PMOD connector	This is the primary connector allowing to power the Eval board and bring the SPI, DIO and IRQ signals to a host MCU. The pinout mostly follows the Digilent PMOD interface Type 2A
J7, J8	GND	Ground connection bar. Allows easy ground connection for oscilloscope probes or similar.

In addition to connectors and jumpers, the board features several test points that allow monitoring of various signals. See Table 2.

Table 2. TEST POINTS

Name on Board	Function	Comments
TP1	Clock input.	In case the board should be clocked by an external clock, TP1 can be used to inject a 25 MHz LVCMOS external clock signal. For this to work, the on−board crystal circuit needs to be disconnected from the NCN26010 device. This is done by removing the 0 Ω resistor R7.
TP2, TP3	LineP and LineN Test Points	TP2 and TP3 can be used to monitor the 10BASE−T1S signal at the NCN26010 pins (behind the decoupling network). onsemi recommends the use of a differential probe with low capacitance, when monitoring the LINEN/P differential 10BASE−T1S signals
TL1, TL2	MDI L+ and L− Test Point (LINEP/N_OUT)	Same as TP2 and T3, these test points can be used to monitor the activity on the SPE Ethernet line (or cable). In contrast to TP2 and TP3, TL1 and TL2 are test points that allow monitoring the SPE signal before the AC coupling capacitors and the common mode choke (at the MDI)
TP7	Clock output	This test pin can be used to monitor the 25MHz system clock of the device. See datasheet for details on how to enable or disable this output.

Connector Pinouts

PMOD connector J6

The PMOD connector J6 is used to connect the eval board to the host CPU. Its pinout mainly follows the Digilent recommendations for SPI PMOD 2A connector pinout. The numbering follows the PMOD recommendation. The Table 3 shows the numbering scheme when looking directly at the connector from the left edge of the board.

Table 3. PMOD PIN NUMBERING

1	2	3	4	5	6
7	8	9	10	11	12

See table below for the pin out and pin description of the J6 PMOD connector.

Table 4. J6 PMOD CONNECTOR PINOUT

Pin	Signal	Comment
1	CSn	SPI active low chip select. Driven by the host, input to the eval board. This pin is used to select the device for SPI transaction. When low the NCN26010 will accept SPI data from the host.
2	MOSI	Master Out Slave In Output from Host, input to NCN26010 MOSI is part of the SPI interface.
3	MISO	Master In Slave Out Input to Host, output from NCN26010 MISO is part of the SPI interface
4	SCK	SPI clock driven by Host The SPI clock needs to be in the range between 15 and 25 MHz to comply with the requirements of the Open Alliance specification
5	GND	Ground connection
6	VDD	3.3 V power supply. Used to power the Evaluation Board
7	IRQn	Interrupt request signal, driven by NCN26010. Output from NCN26010, input to the host computer / MCU. Used by NCN26010 to signal RX data and other events.
8	RSTn	To reset the device, this pin needs to be driven low by the host. As this pin is an open drain bidirectional pin on NCN26010, it should never be driven to VDD (to prevent damage to both, the host and the NCN26010). The board provides a 3.3 kΩ pull−up resistor on this pin.
9	DIO1	Digital GPIO from NCN26010, see datasheet for details
10	DIO0	Digital GPIO from NCN26010, see datasheet for details
11	GND	Ground connection
12	VDD	3.3 V power supply. Used to power the Evaluation Board

Side connector J5

The side connector J5 can be used to monitor the SPI traffic as well as the DIO0/1 and IRQn pins of NCN26010.

As it provides all necessary pins to connect the NCN26010XMNEVB to a host MCU, it can also be used instead of the PMOD (J6) connector for 3rd party SBC or MCU boards that do not offer a PMOD port.

The pinout of the J5 connector is shown in the Table 5. For a brief functional description please consult Table 4.

Table 5. J5 Side Connector Pinout

Pin number	Function
1	GND
2	CSn
3	MOSI
4	MISO
5	SCK
6	IRQn
7	RSTn
8	DIO1
9	DIO0
10	3.3V VDD

Using an External Clock

If the user of the NCN26010 desires to not use the on−board crystal oscillator but rather use an external 25 MHz clock instead, such clock can be fed into the board via the XI (TP1) test point after removing the R7 resistor.

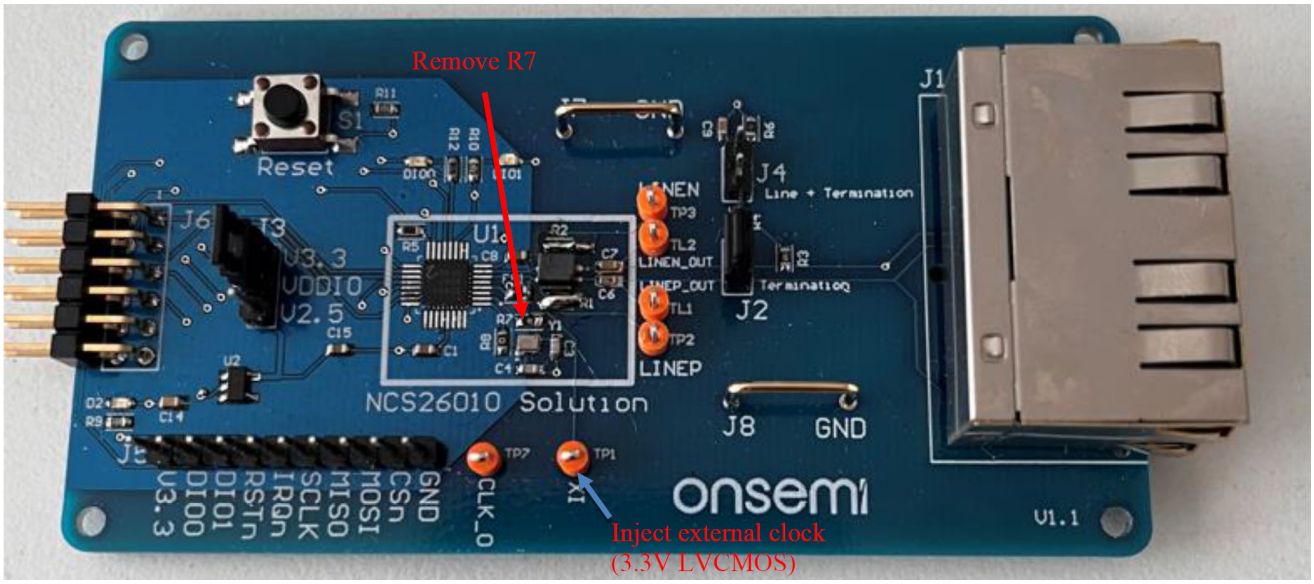


Figure 4.

Bypassing the Common Mode Choke

In some cases, users may wish to test the performance without a common mode choke.

To bypass the common mode choke, two 0 Ω resistors R2 and R1 need to be populated by the user.

In addition, users can also remove the common mode choke from the boards when R1 and R2 are populated.

NCN26010XMNEBV Schematic

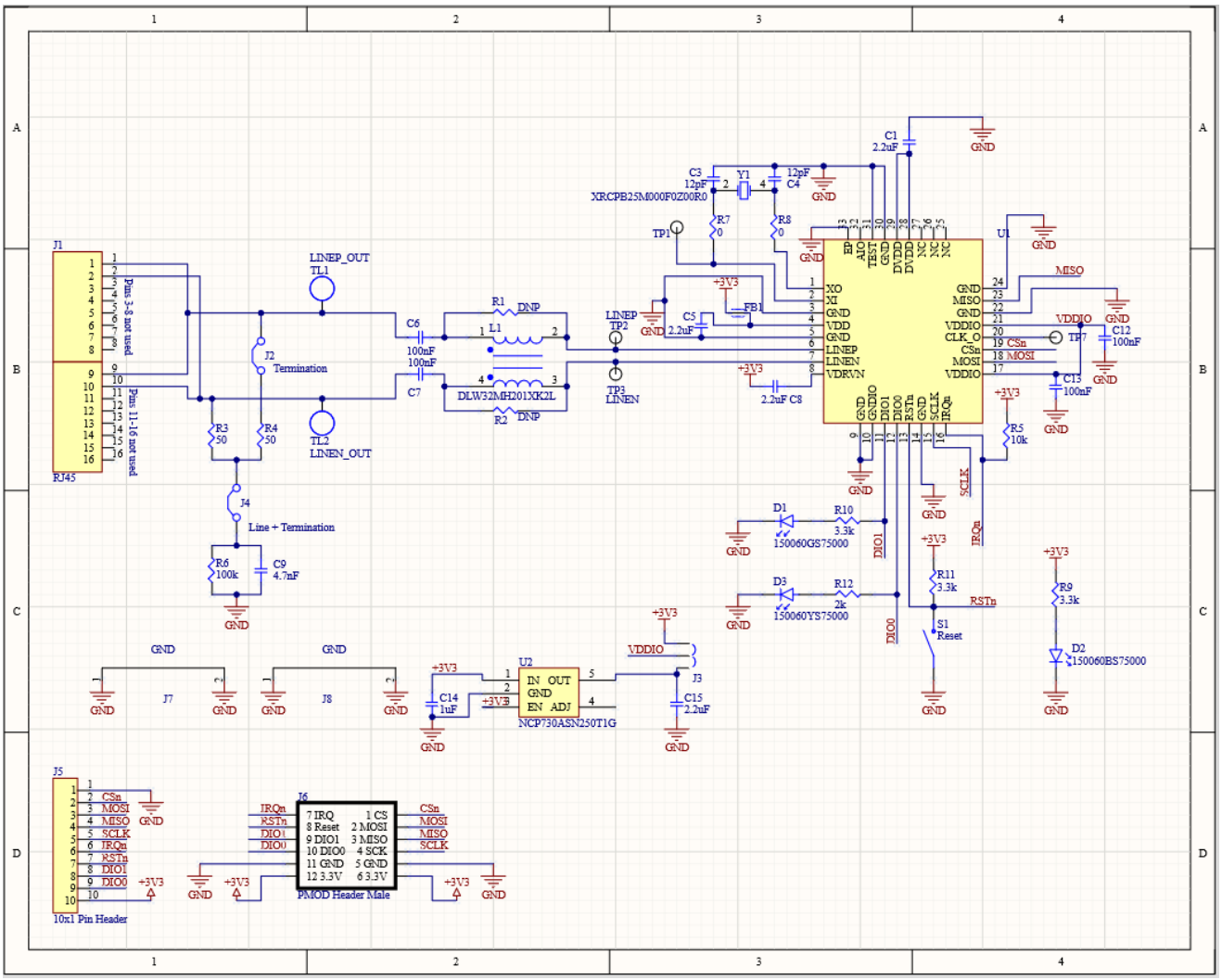


Figure 5. NCN26010XMNEBV Schematic

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