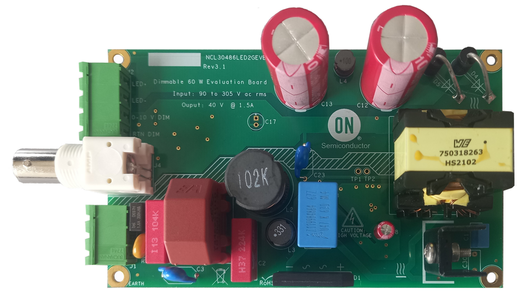
NCL30486LED2 60 W High Power Factor Dimmable LED Driver Evaluation Board User's Manual

NCL30486LED2GEVB



Evaluation Board Overview

This manual covers the specification, construction, and testing of the NCL30486B evaluation board. This board is configured as a 60 W high PF flyback LED driver for LED lighting.

The Key Features of this Evaluation Board

- PSR (Primary Side Regulation)
- Low THDi
- High Power Factor
- CC/CV Modes
- Quasi-Resonant Operation
- Valley Count Frequency Foldback
- High Line Valley Skip
- 0 – 10 V Fully Isolated Dimming Control
- Brown Out/In
- Line Feedforward Compensation
- Current Limit Protection
- Output Over Voltage Protection
- Open/Short Pin Protection

SPECIFICATIONS

Parameter	Value	Unit
Input Voltage	100 – 277	V ac
Line Frequency	50/60	Hz
THDi (>50% Load)	20%	Max.
Power Factor (>75% Load)	0.9	Min.
Output Voltage	40	V dc
Output Current	1.5	A dc
Efficiency	90%	Max
Ripple	< 50%	Pk – Pk
Startup Time	< 250	ms
Dimming Isolation	500	V dc

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CONTROLLER PIN DESCRIPTIONS

ADIM Pin

Analog dimming control voltage is applied to this pin. Voltage between $V_{DIM(MIN)}$ and V_{DIM100} will dim the output current from a minimum value [dimming clamp of 0, 1, 5, or 8%] to 100%. The dimming level corresponds to a minimum of 0.7 volts up to a maximum of 3.0 volts. When ADIM pin is lower than $V_{ADIM(EN)}$ (0.5 V), DRV pulses are disabled or dimCV mode is entered according to the options.

This analog dimming control can be used together with PDIM to achieve higher resolution for low dim levels. Leave this pin open if no analog dimming control is required. Connect a 100 pF capacitor to this pin in all cases. Do not exceed 5.5 V input from external control devices.

COMP Pin

The OTA error amplifier output is available on this pin. A Type 2 compensation network connected between this pin and ground controls loop bandwidth for constant voltage (CV) control. Voltage on the COMP pin is discharged to zero when Vcc is below reset level.

ZCD Pin

Demagnetization Function

The power magnetic is monitored through an auxiliary winding connected to this pin. Core demagnetization is detected and processed by the valley count control before issuing a DRV pulse starting the next switching cycle. This processing insures quasi-resonant operation which minimizes losses by initiating the next switching cycle near a minimum drain voltage.

Shorted Output Detection

Should the ZCD voltage remain at or below 0.65 volts for 90 ms, it is assumed the converter output is shorted. The controller will cease drive pulses for 4 seconds allowing a cooling period before automatically restarting.

Voltage Monitoring

Auxiliary winding voltage is monitored as part of CV regulation control. Voltage is sensed after a blanking time and processed for CV regulation. Voltage regulation threshold is 3.50 volts. Actual output voltage is determined by the transformer turns ratio and the resistor divider network between the ZCD pin and auxiliary winding.

It can be seen that the ZCD voltage is limited to a range of 0.65 volts (shorted output) to 3.50 volts (regulation threshold) resulting in an output voltage control range of 5.38:1. Thresholds should be carefully matched to LED voltage to avoid unintentionally limiting constant current (CC) output level by entering CV mode, especially at low temperatures. However, the CV mode can be used to limit output power if needed.

Over Voltage Protection

If the aux winding voltage exceeds the Slow OVP threshold (115% nominal) for 4 consecutive cycles, DRV pulses are suspended for 1.5 ms. After this delay, a DRV pulse is issued to check output voltage. The cycle repeats until the aux winding voltage is below Slow OVP threshold. Note that at very light loads, the test pulse can cause the output voltage to increase.

If the aux winding voltage exceeds the Fast OVP threshold (130% nominal) for 4 consecutive cycles, or 2 cycles if Slow OVP is already active, DRV pulses are suspended for 4 seconds. After this time, DRV pulses resume.

CS Pin

Current Mode Control

MOSFET current information enters through this pin. The control algorithm uses this current information to compute output current. The overcurrent protection threshold is 1.4 volts with a 350 ns blanking period. When the threshold is reached, the switching cycle is terminated. The next cycle will start when ZCD conditions are met. In case of extreme faults a higher threshold of 1.96 volts with 170 ns blanking will initiate a 4 second shutdown after 4 consecutive pulses. Recovery is automatic.

CS Short Detection

When Vcc bias power is first applied, the controller delivers 500 μA out the pin and monitors the voltage on the CS Pin. If the voltage is below 60 mV, the controller assumes a shorted pin and will not issue DRV pulses. With tolerance, the minimum resistance in series with the CS pin is 225 Ω.

Line Feedforward

The control algorithm accounts for many errors, such as leakage inductance, when computing the output current. Some error sources are variable with line voltage, such as the effect of delays in the power stage. As the input voltage increases, the power stage delays cause the peak current to slightly overshoot. While this is not usually a large increase in output current, the control can compensate for this by sourcing a current out of CS Pin which is proportional to the input voltage. This introduces a voltage drop across the series resistor between CS Pin and MOSFET current sense resistor. The voltage drop reduces the target peak current slightly such that the effect of the delay is cancelled and regulation is improved. The optimal value for the series resistance is a trial and error process, bearing in mind the previously described minimum value. Note that any impedance between DRV pin and the gate of the switching MOSFET will affect regulation.

GND

This is the ground or return reference pin for the controller. Use good PCB layout practices to ensure switching currents do not degrade control signals.

DRV Pin

The DRV pin connects to the gate of the MOSFET. A direct connection to the gate is recommended for optimal primary side regulation. If necessary, switching times can be modified via a collection of resistors and diodes for EMI considerations.

Vcc Pin

This pin receives the bias power for the controller. The internal HV Startup provides initial charge to the Vcc capacitor. After the converter is operational, an external source provides bias power. Typically, the ZCD winding is dimensioned to also supply bias power.

Proper bypassing is required for the Vcc Pin. Place sufficient capacitance to maintain operating voltage during DRV Pin sourcing. A good quality electrolytic capacitor is typically sufficient, however some applications may require a 100 nF ceramic capacitor as well. 10 μF is a good first choice. Excessive capacitance or external loads will increase stress on the HV startup current source.

Over Voltage Protection is included on Vcc Pin. Typical OVP threshold is 26.5 Vdc. Ensure the external bias does not exceed the minimum OVP threshold of 25 Vdc to avoid activating the protection feature. A voltage regulator can be used for applications requiring wide output voltage range since aux winding voltage follows output voltage and may exceed the OVP threshold.

PDIM Pin

This pin is used for Pulse Width Modulation dimming control. An opto-coupler can be connected directly to this pin thanks to an innovative current controlled interface. Opto-coupler collector voltage is held constant while duty factor information is interpreted via collector current. This provides more symmetric response for rise and fall times allowing higher dimming accuracy. Typical current thresholds are 70 μA rising and 153 μA falling. Current should not exceed 1080 μA or the interface will be out of operating range. Care should be taken in selecting the opto-coupler and drive current of the opto-LED. Generally speaking, select a low CTR opto-coupler with a narrow gain range.

As previously mentioned, this PWM dimming control can be used together with ADIM to achieve higher resolution for low dim levels. Leave this pin open if no PWM dimming control is required. The control will default to 100%. Connect a 100 pF capacitor to this pin in all cases.

If PDIM Pin is continuously pulled low, the controller is disabled.

HV Pin

The High Voltage Pin provides three essential functions: start up current, input line reference, and line range selection. It is recommended that a resistance is place in series with the rectified ac bus, and a capacitor is connected to return. The corner frequency of this RC filter is between 12 kHz and 20 kHz to limit high frequency noise. Recommended resistance is 1 kΩ to 3.3 kΩ.

HV Start

An internal HV current source charges the Vcc capacitor when ac input is first applied. Initial current is limited to 300 μA until Vcc exceeds 1 V. This prevents excessive dissipation in the event Vcc is shorted. Nominal charge current is 5.1 mA which is applied until $V_{CC(on)}$ is reached, typically 18 V.

After reaching $V_{CC(on)}$, the HV current source is turned off, the controller is activated, and DRV pulses are issued. Bias power is derived from the Vcc capacitor until alternate bias power is available. Typically, the ZCD winding is configured as an Auxiliary source to supply bias power. If alternate power is not available, the controller will cease DRV pulses when Vcc falls below 10.2 V. At this point, the HV current source resumes charging the Vcc capacitor as another start up attempt is made.

Rectified Line Sensing

The rectified ac input supplies a reference for the Power Factor control loop. The signal is internally scaled and used to match input current to the input voltage thereby providing High Power factor and low Total Harmonic Distortion. Care should be taken in the design of the EMI input filter to not introduce excessive distortion or phase delay which could cause poor performance. It is essential the HV Pin voltage be a good representation of the rectified ac input voltage. In particular, the voltage must reduce to a low level at zero crossings.

The rectified ac input is also used for brown out detection. When the applied voltage exceeds a threshold, DRV pulses are enabled. Conversely, when the applied voltage falls below another lower threshold, DRV pulses are terminated. A 25 ms blanking time is used with brown out. Two ranges of brown out protection are available.

The controller has an optional input over voltage protection feature. If the rectified ac input exceeds 469 V dc nominal, DRV pulses are terminated. When voltage drops below 443 V dc for 25 ms, operation resumes.

Line Range Selection

The gain of the feedback loop is dynamically changed to provide optimum PF, THDi, and output regulation over a wide range of ac input voltage. An internal comparator monitors ac input voltage present on the HV Pin and changes the gain at a voltage which is not internationally used for commercial power. Transitioning through this input voltage band will appear as a disturbance in output power as a one-time event. It is not indicative of a problem within the controller.

As previously mentioned in the CS Pin section, a current proportional to the ac input voltage is sourced out the CS Pin. This current compensates for delays which are related to ac input voltage. The basis for this current is the voltage monitored on the HV Pin.

SETTING UP THE LED DRIVER

Constant Current Control

The Primary Side Regulation control loop monitors the voltage presented on the CS Pin to maintain proper Constant Current output. This PSR control function eliminates the need for an opto-coupler and yet maintains tight load current regulation.

The parallel combination of R11 and R12 is Rsense. The term Nsp is the secondary to primary winding turns ratio of the transformer. V_{REF} is 334.2 mV. The formula below establishes the full output current regulation point in CC mode.

$$I_{out} = \frac{V_{REF}}{2\,N_{SP}\,R_{sense}}$$

Note that this calculation is independent of transformer inductance. In addition, leakage inductance is compensated via the control algorithm. Best performance is obtained if capacitor C11 of the primary winding clamp is connected to the source of Q2.

Constant Voltage Control

The Primary Side Regulation also includes a Constant Voltage mode. The Auxiliary winding voltage is scaled by resistor divider R6 & R7 and present to the ZCD pin. The voltage is sampled during the switch off-time after a blanking delay and used for CV feedback. The internal reference voltage is 3.50 V nominal. In other words, CV regulation point is determined by the output winding to Aux winding turns ratio and the resistor divider.

Care must be taken when setting the CV regulation point. LEDs have a negative temperature coefficient, which means the voltage drop will be higher at low temperature. Ensure the CV regulation voltage is higher than the maximum LED string voltage in order to maintain Constant Current operation. Note that it is possible to limit output power at low temperature by adjusting the CV regulation point within the expected LED string voltage at low temperature. Careful tolerance allowance is required in this case.

PWM Dimming

R16 limits the maximum current sourced by the PDIM Pin. This pin maintains a fixed 3 V, and therefore the ‘low state’ current will be 3 V / 16k = 188 μA. The digital isolator has an open collector output. R17 maintains a small bias current for PDIM Pin when the isolator is in the ‘high state’, 3 V / (16k + 47k) = 48 μA. This satisfies the minimum current requirement. C15 bypasses noise from PDIM Pin.

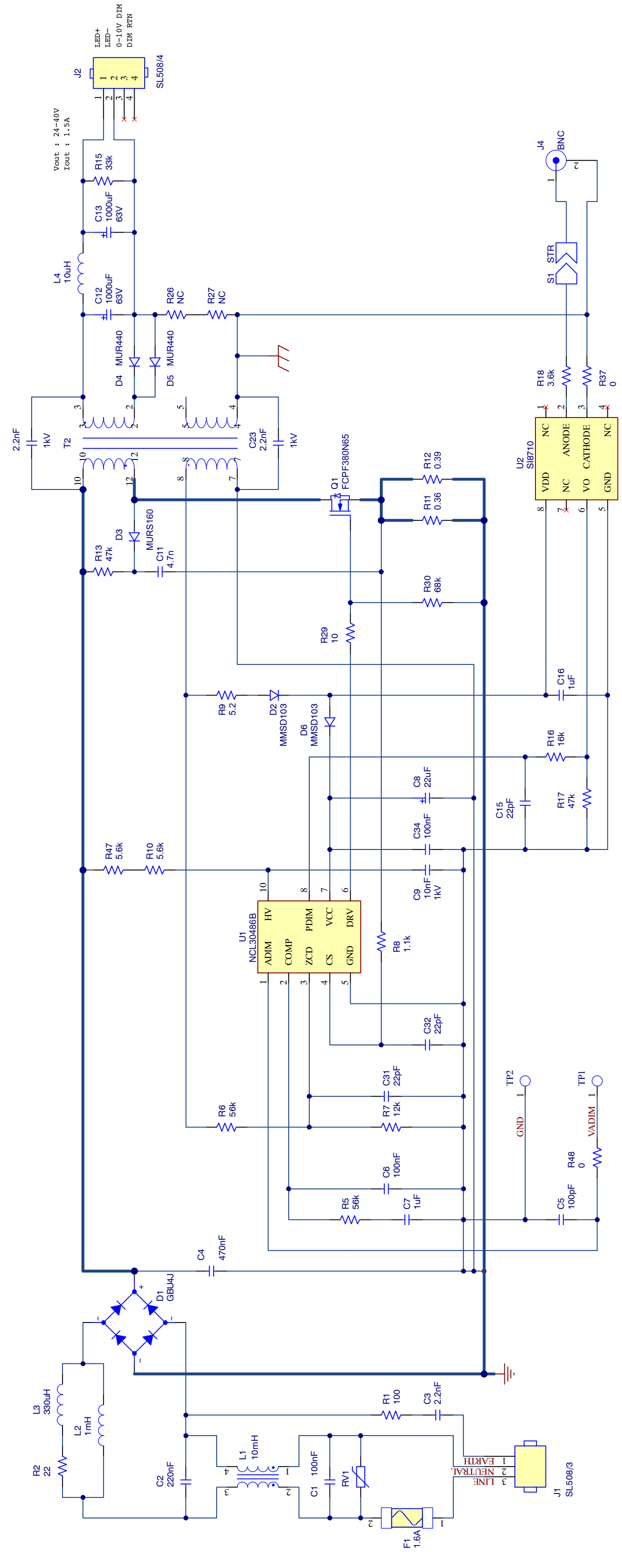

Figure 1. EVB Schematic

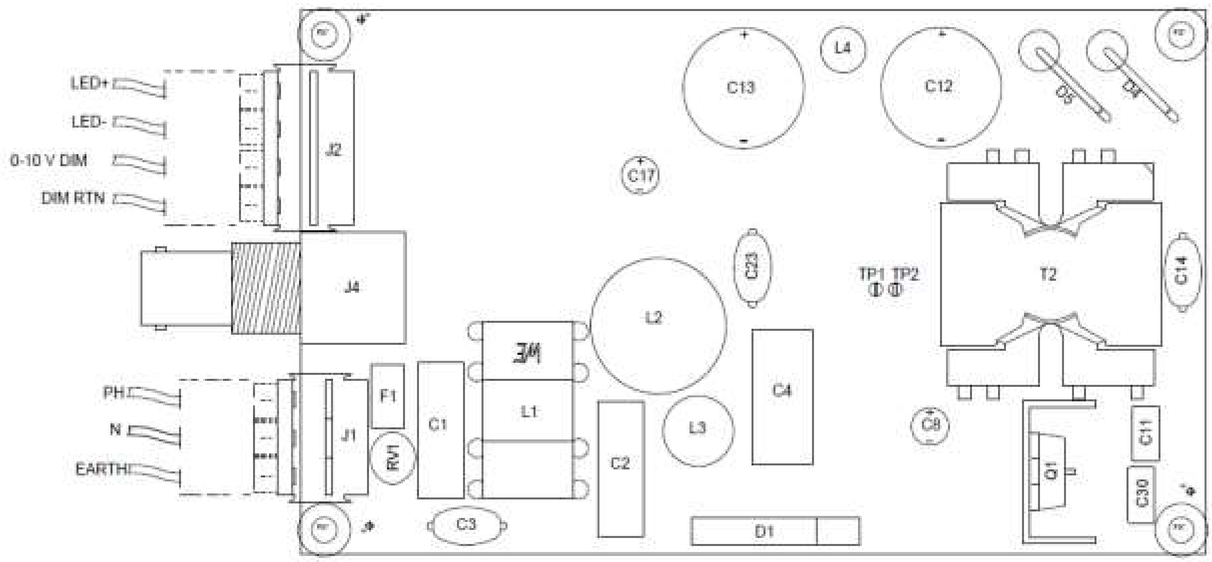

Figure 2. Top Silkscreen

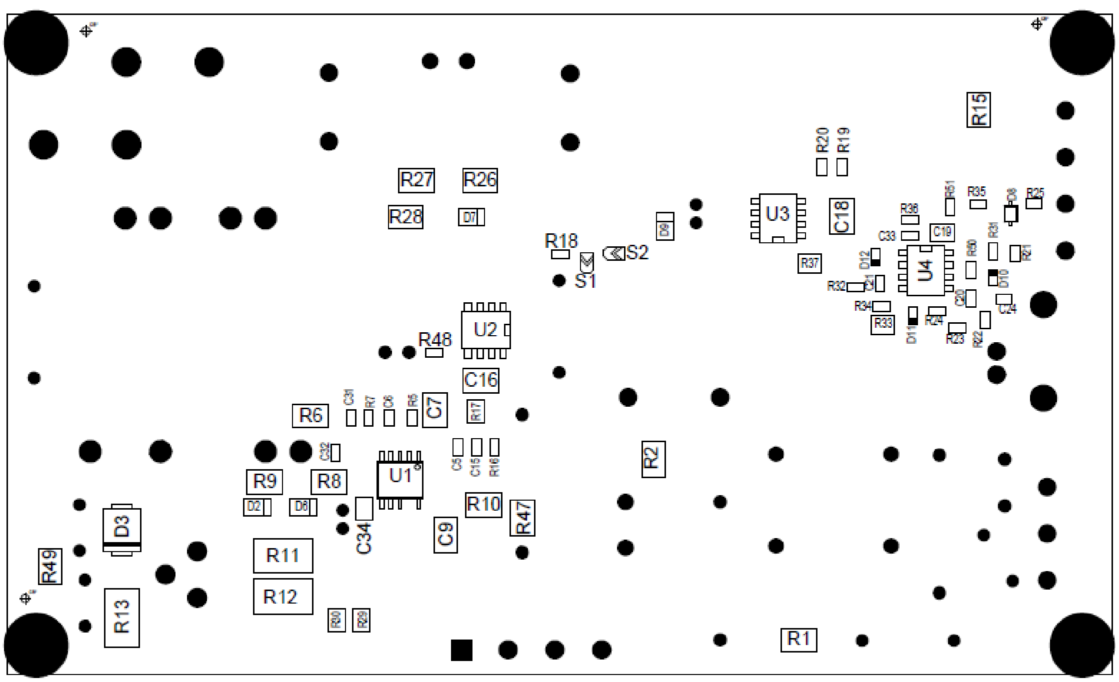

Figure 3. Bottom Silkscreen

TEST PROCEDURE

Required Equipment

- AC Source: 90 to 277 V rms, 50/60 Hz, minimum 100 W capability
- AC Wattmeter: 100 W minimum, with power factor measurement capability
- Signal generator
- DC Voltmeter: 100 V dc minimum, 0.1% accuracy
- DC Ammeter: 2 A dc minimum, 0.1% accuracy
- LED load: 35 V to 40 V dc, rated 1.5 A dc
- Resistor load: 100 Ω, 30 W minimum

Test Connections Per Figure 4

1. Connect AC source to the input of the power meter. Connect the output of the wattmeter to connector J1 of UUT (Unit Under Test). Observe ‘L’ and ‘N’ connections. Connect J1 ‘Earth’ to Ground for safety.
2. Connect UUT output connector J2 ‘LED+’ to DC ammeter. Connect other lead of DC ammeter to ‘+’ of LED Load. Connect UUT output connector J2 ‘LED−’ to ‘−’ terminal of the LED load.
   Caution: Observe correct polarity to avoid potentially damaging the load.
3. Connect DC voltmeter to UUT output connector J2 ‘LED+’ and ‘LED−’.
4. Connect the waveform generator to the UUT connector J4 using a BNC cable. Keep the waveform off for the moment. It will be used for the dimming tests only.

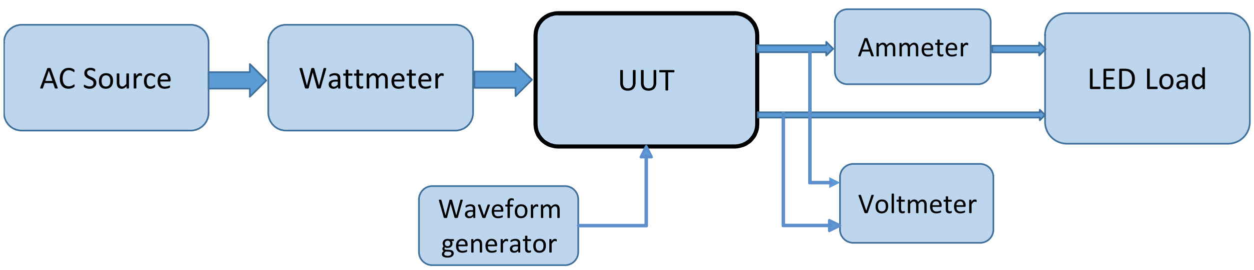

Figure 4. Test Setup

Constant Current Regulation

1. Set the LED Load between 36 and 38 V dc
2. Set the AC Source as indicated in the chart below.
   Caution: Do not touch the UUT once it is energized. Hazardous voltages are present.
3. Enter ‘P’ or ‘F’ in column below depending on test result.
4. When test is completed, set AC Source to zero volts, Set DC Supply to zero volts.

Input Vac	Input Power	Power Factor		Output Current			Output Voltage
		Reading	P/F (>0.9)	Reading	Limits	Pass/Fail	
100					1.33 – 1.47 A dc		
120					1.33 – 1.47 A dc		
230					1.33 – 1.47 A dc		
277					1.33 – 1.47 A dc		

Dimming Test

1. Apply 120 V ac for all tests shown below.
   Caution: Do not touch the UUT once the power is applied. Hazardous voltages are present.
2. Set the waveform generator as follows: square signal waveform with V_{high} = 10 V, V_{low} = 0 V, 4 ms period ($T_{sw(DIM)}$), inverted polarity (see Figure 5). Set duty−ratio as indicated in below table.

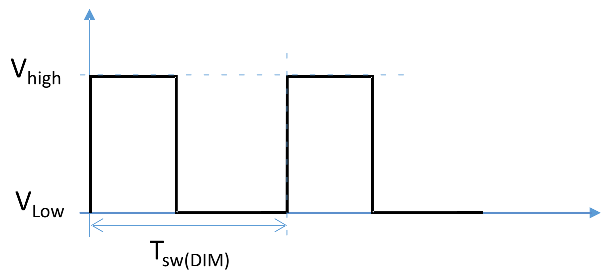

Figure 5. Dimming Signal

3. Enter 'P' or 'F' in column below depending on test results.

Dimming Duty−ratio	Output Current			Output Voltage
	Reading	Limits	Pass / Fail	
50%		0.68 – 0.77 A dc		
10%		0.13 – 0.16 A dc		

4. When test is completed, disconnect AC source and waveform generator.

Constant Voltage Regulation

1. Disconnect the waveform generator from J4.
2. Remove the LED load and replace it with the 100 Ω resistor.
3. Set the AC source as indicated in the table below.
4. Enter 'P' or 'F' in column below depending on test result.
5. When test is completed, turn−off the AC source.

Input Voltage (V rms)	Output Voltage		
	Reading	Limits	Pass / Fail
120		37 – 41 V dc	
277		37 – 41 V dc	

TYPICAL TEST DATA

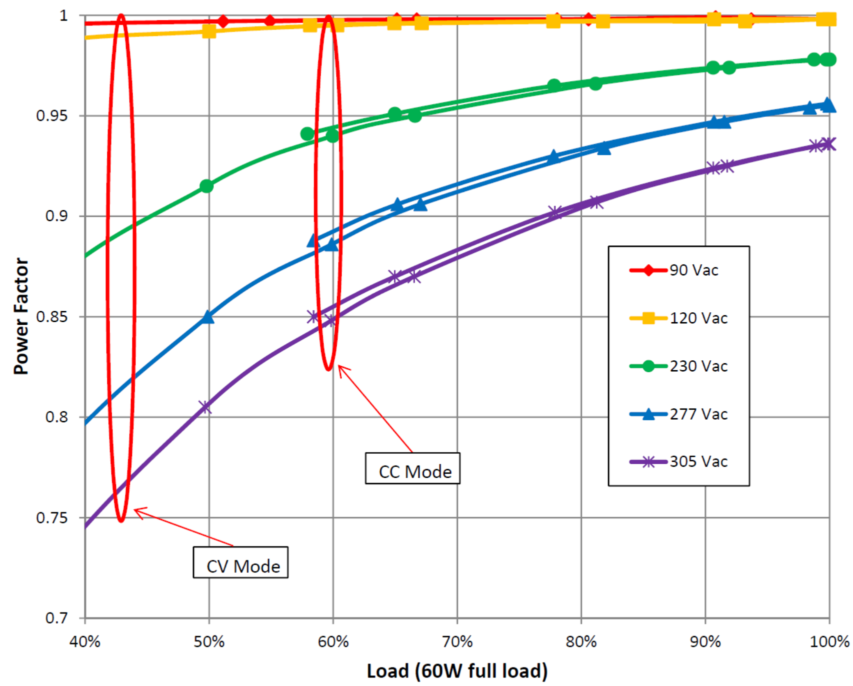

Figure 6. Power Factor Performance

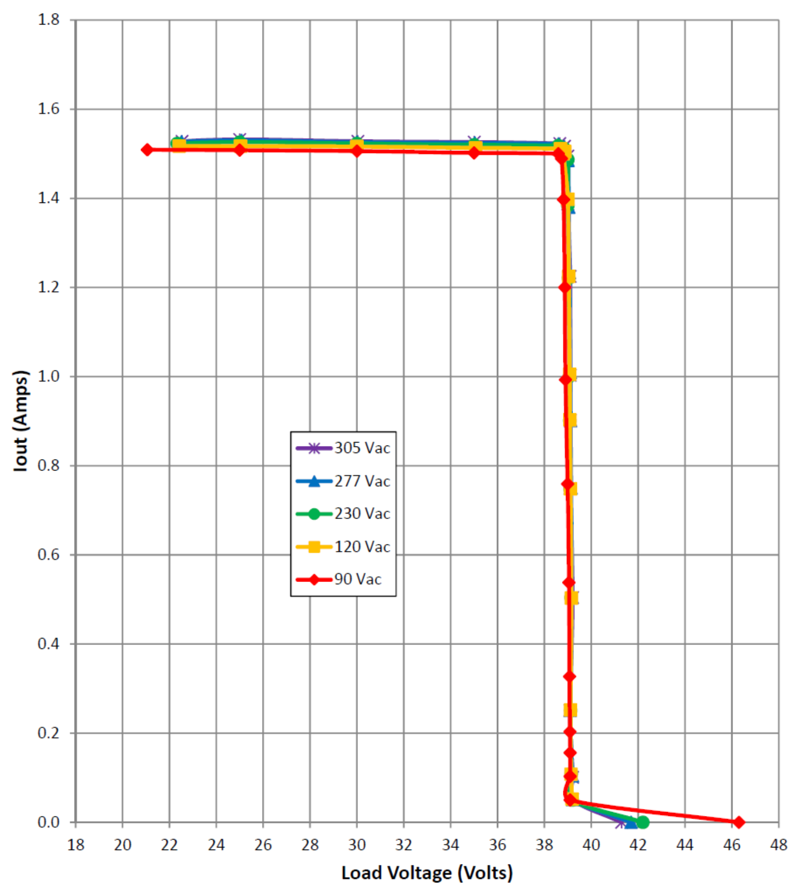

Figure 7. Line and Load Regulation Performance

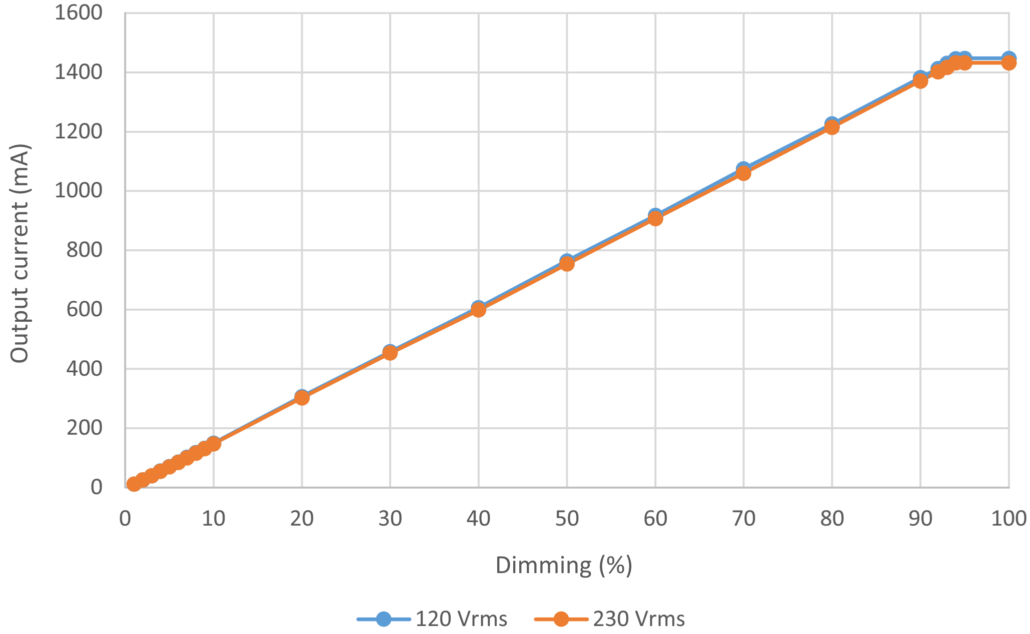

Figure 8. Dimming Performance

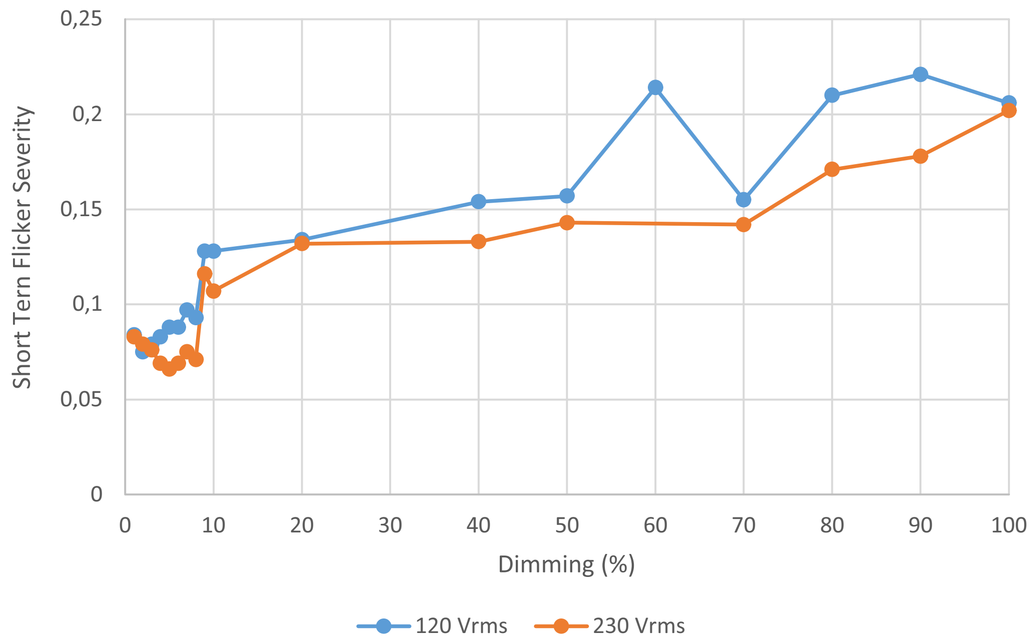

Figure 9. Short Term Flicker Severity Pst

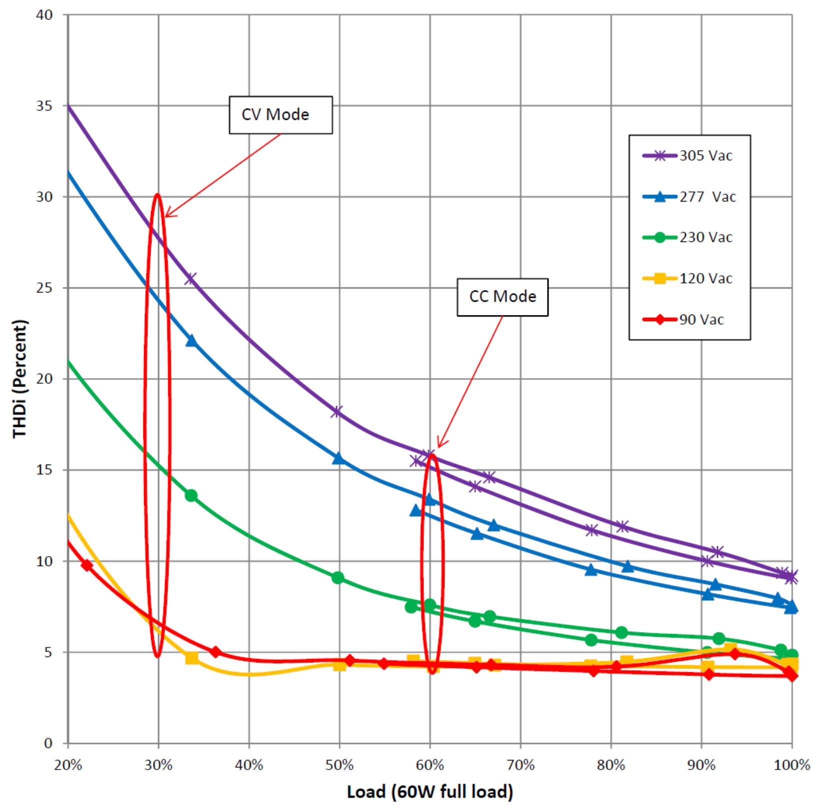

Figure 10. THDi Performance

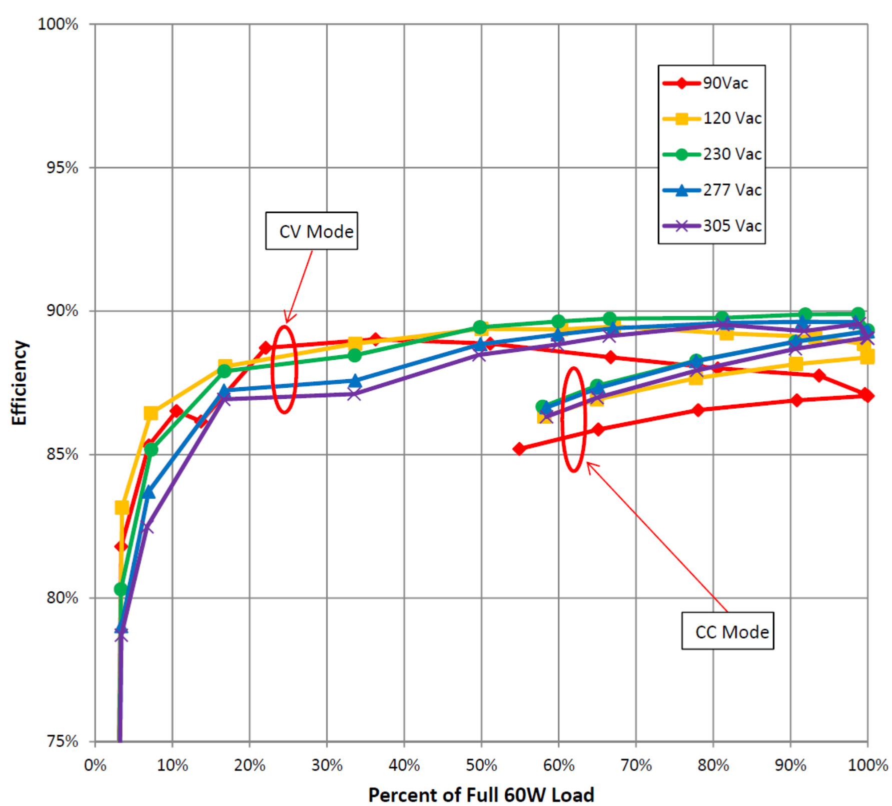

Figure 11. Efficiency

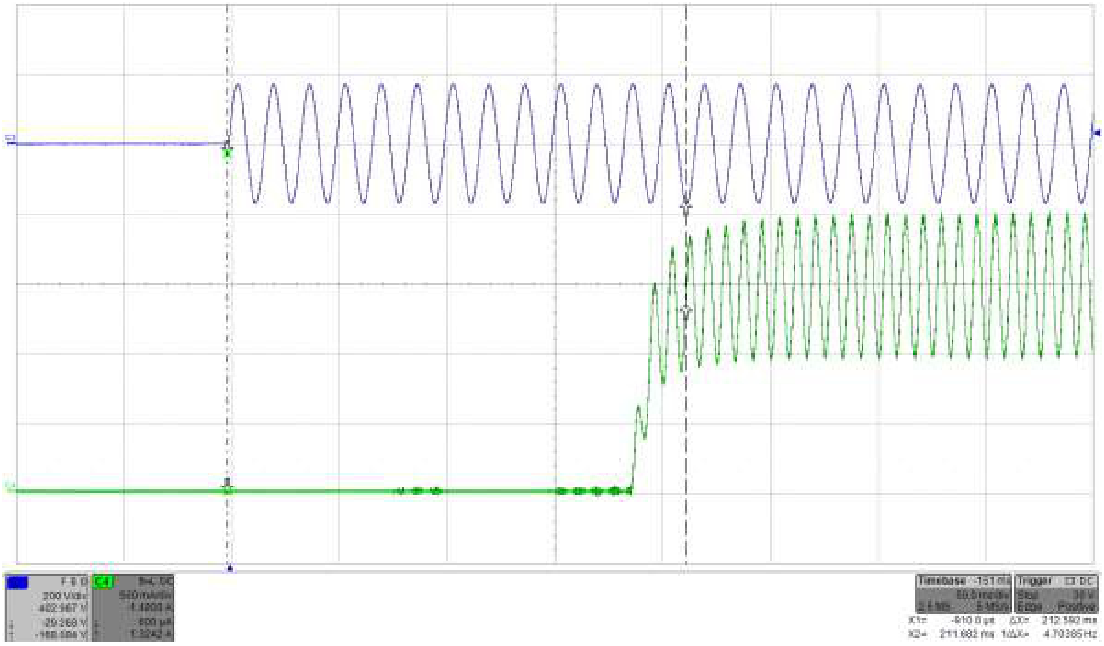

Figure 12. Full Load Startup 120 V rms

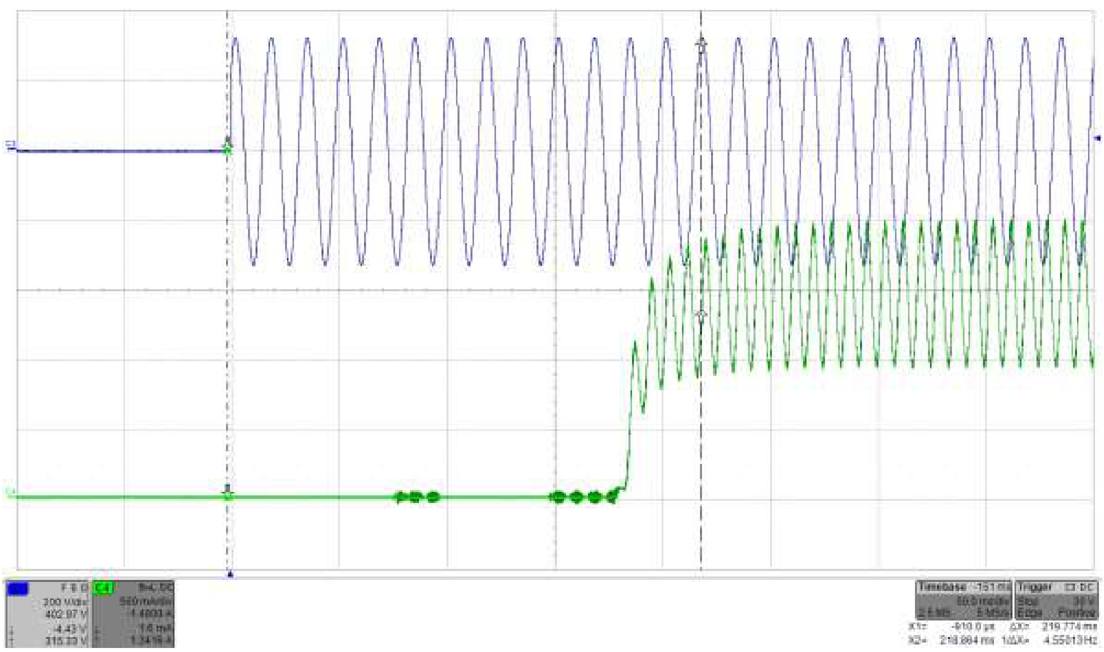

Figure 13. Full Load Startup 230 V rms

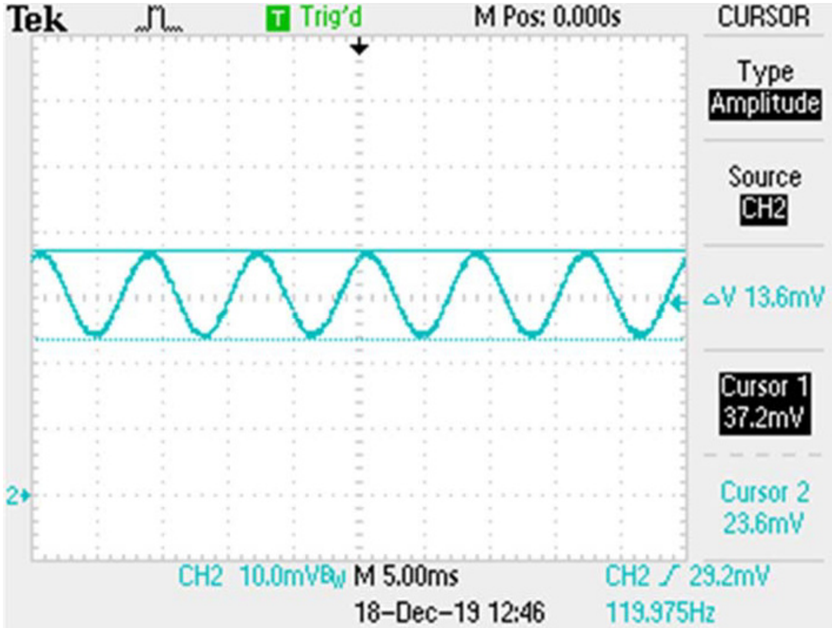

Figure 14. Output Ripple Current with 120 V ac Input

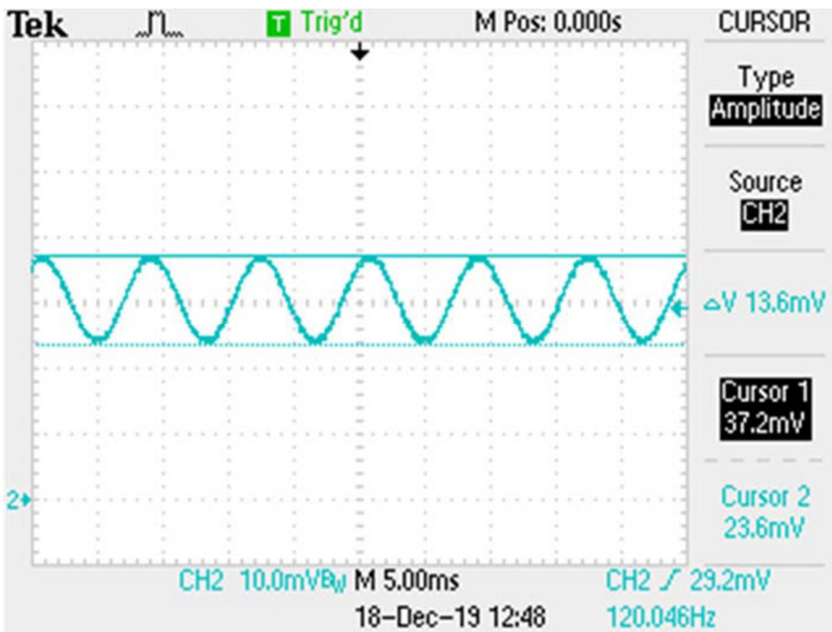

Figure 15. Output Ripple Current with 230 V ac Input

ADDITIONAL INFORMATION

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