NCP51100 EVB

Single 2A Low-Side Gate Driver Evaluation Board User's Manual

ON Semiconductor®

www.onsemi.com

EVAL BOARD USER'S MANUAL

Introduction

This user guide supports the evaluation board for the NCP51100. It should be used in conjunction with the NCP51100 datasheets as well as ON's application notes and technical support team. Please visit ON's website at www.onsemi.com.

This document describes a proposed solution for the high speed dual gate driver using the NCP51100. This user's guide also includes information regarding operating procedures, input/output connections, an electrical schematic, printed circuit board (PCB) layout, and a bill of material (BOM) for the evaluation board.

Description

The NCP51100 2 A gate driver is designed to drive an N−channel enhancement−mode MOSFET in low −side switching applications by providing high peak current pulses during the short switching intervals. The driver is available with TTL input thresholds. Internal circuitry provides an under−voltage lockout function by holding the output LOW until the supply voltage is within the operating range. The NCP51100 delivers fast MOSFET switching performance, which helps maximize efficiency in high frequency power converter designs. NCP51100 drivers incorporate MillerDrive™ architecture for the final output stage. This bipolar−MOSFET combination provides high peak current during the Miller plateau stage of the MOSFET turn−on / turn−off process to minimize switching loss, while providing rail−to−rail voltage swing and reverse current capability. The NCP51100 is available in industry standard, 5−pin, SOT23.

Key Features

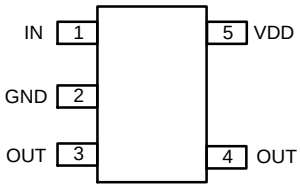
- Industry−Standard Pinouts
- 11 V to 18 V Operating Range
- 3 A Peak Sink/Source at VDD = 12 V
- 2.5 A Sink / 1.8 A Source at VOUT = 6 V
- 14 ns / 7 ns Typical Rise/Fall Times (1 nF Load)
- Under 20 ns Typical Propagation Delay Time
- MillerDrive™ Technology
- 5−Lead SOT23 Package
- Rated from –40°C to +125°C Ambient

Typical Applications

- Switch−Mode Power Supplies
- High−Efficiency MOSFET Switching
- Synchronous Rectifier Circuits
- DC−to−DC Converters
- Motor Control

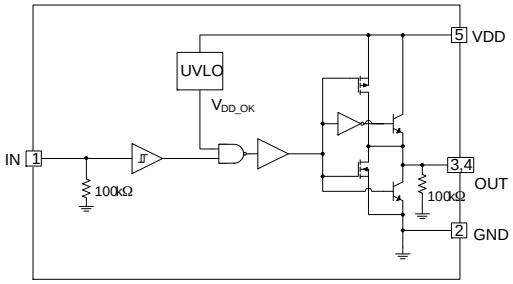
Figure 1. Evaluation Board Picture

PIN CONNECTIONS



(Top View)

FUNCTIONAL BLOCK DIAGRAM



Schematic

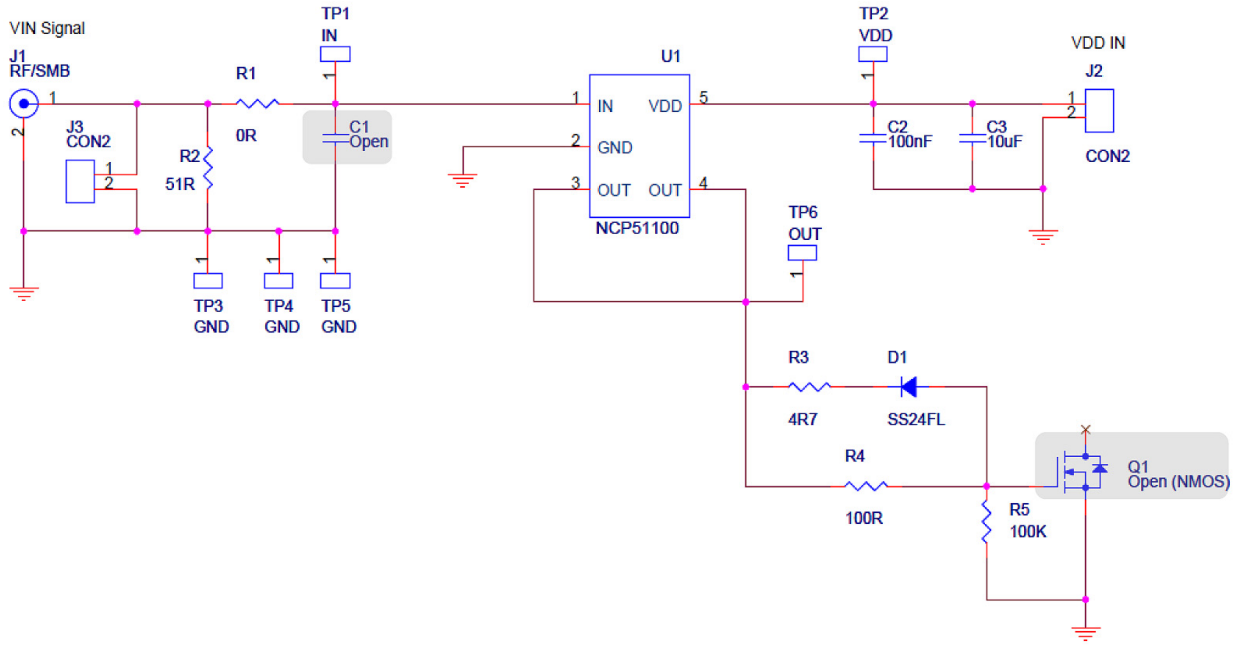


Figure 2. EVB Schematic

Description of Connectors & Test Points

The Table 1 and Table 2 show the description for connectors and test points.

GND is a common ground reference for intput and output circuits.

Table 1. DESCRIPTION OF CONNECTORS

Connector	Pin #	Name	Description	Note
J1	1	VIN	Singal Input (Non−inverting)	
	2	GND	Ground	
J2	1	VDD	Supply Voltage	
	2	GND	Ground	
J3	1	VIN	Singal Input (Non−inverting)	
	2	GND	Ground	

Table 2. DESCRIPTION OF TEST POINTS

TP #	Name	Description	Note
1	IN	Singal Input (Non−inverting)	
2	VDD	Supply Voltage	
3	OUT	Gate Drive Output	
4	GND	Ground	
5	GND	Ground	
6	GND	Ground	

Bench Test Method

The Figure 3 describes the connection for bench test to evaluate NCP51100 EVB

The method for bench test is as the following:

- Connect VDD and GND to 12V power supply
- Connect IN to pulse generator
- Connect TP1 and TP6 to oscilloscope to measure input and output waveform
- Turn on 12 V power supply
- Turn on pulse generator (5V 100khz 50% duty)
- **Measure TP1 and TP6 waveform**: 12 V 100 kHz 50% duty
- Turn off pulse generator
- Turn off power supply

NOTE: The length of wire affects delay time from input to output signal.

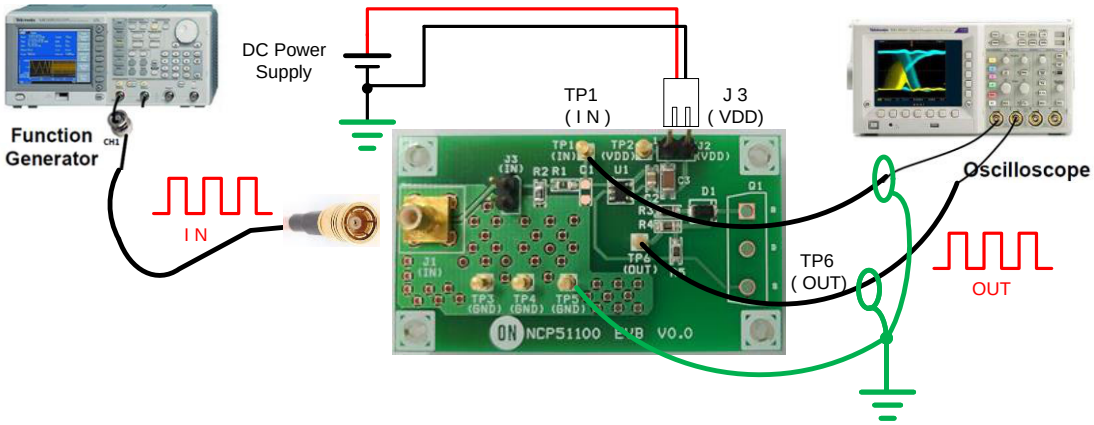


Figure 3. Connection for Bench Test

Waveforms

1. The measured waveforms of inputs and outputs are shown in Figures 6, 7, 8 and 9.
2. The definition for switching waveform timing chart are described in the Figure 4 and Figure 5.

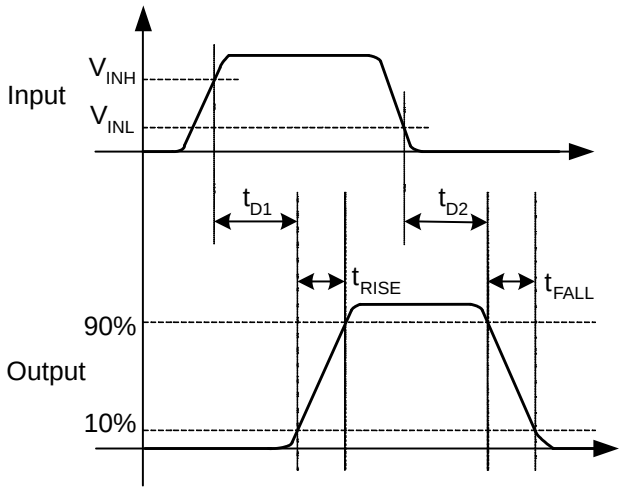


Figure 4. Switching Waveform Definitions

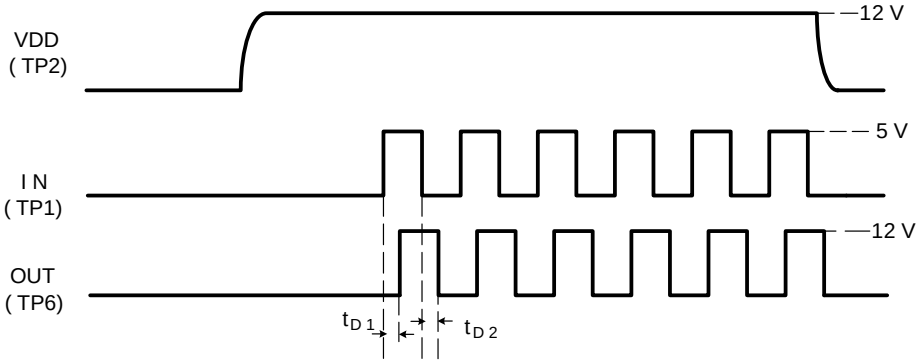


Figure 5. Timing Charts

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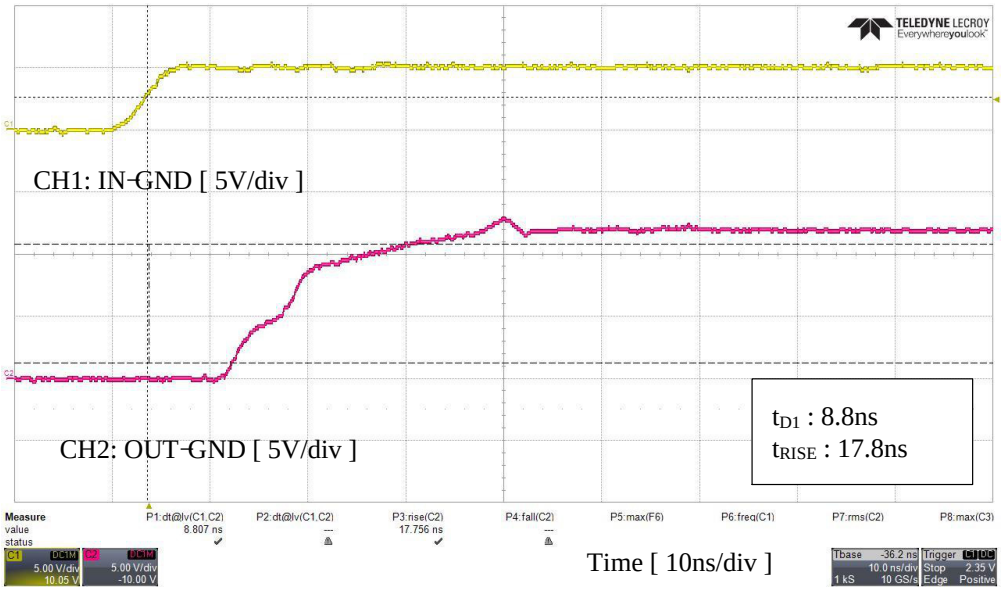

Figure 6. Turn On Waveforms

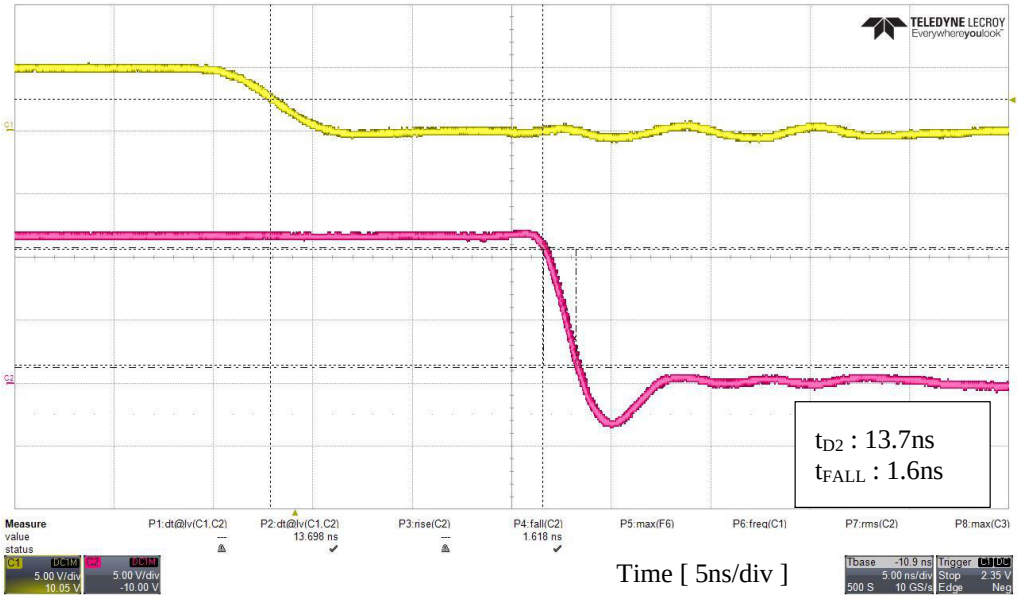

Figure 7. Turn Off Waveforms

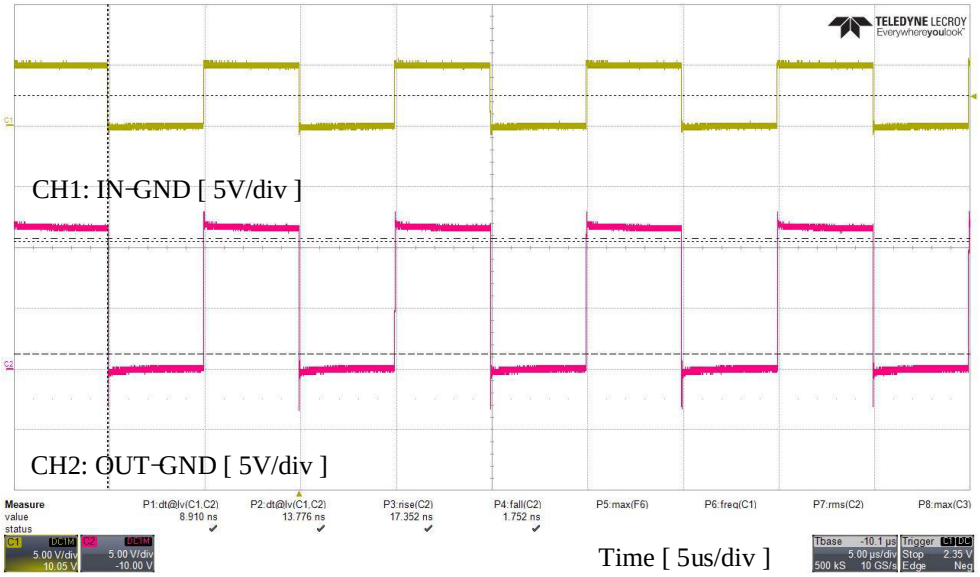

Figure 8. Waveforms @ 100 kHz Switching

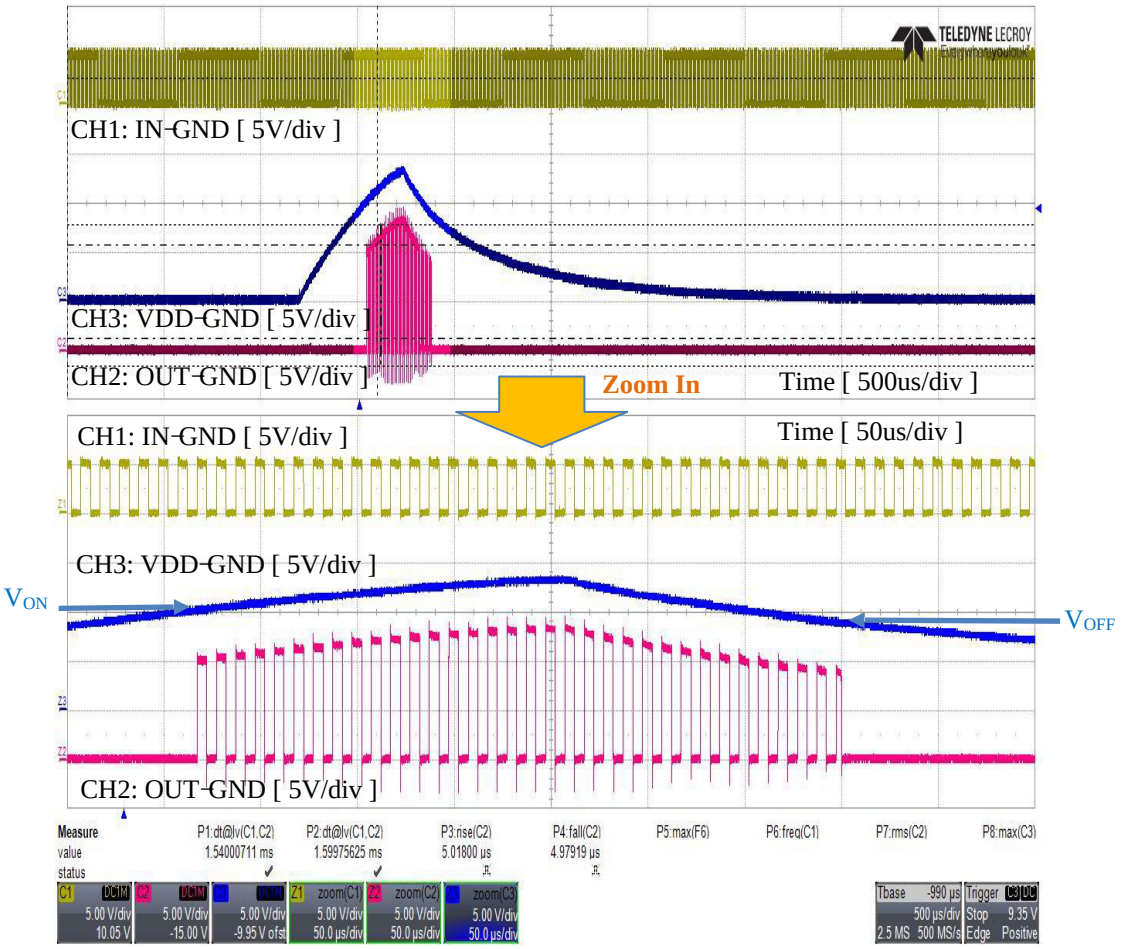

Figure 9. Waveforms while VDD is Varied from 0 V to 12 V

PCB Assembly

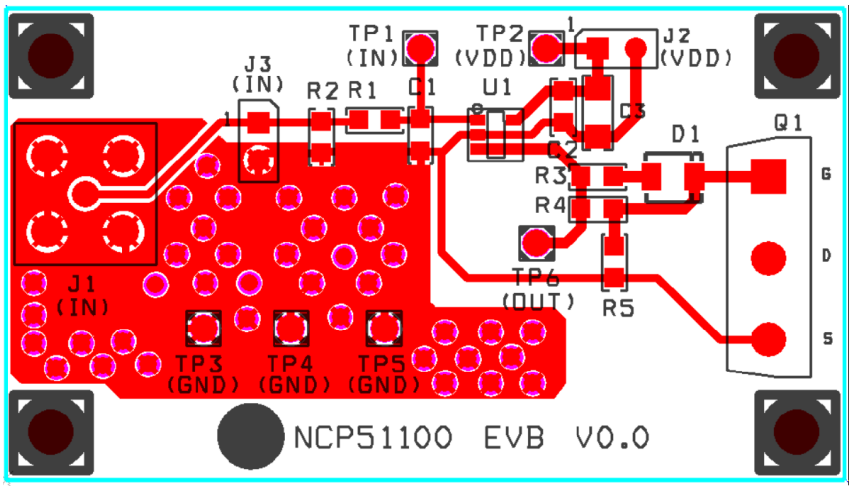

Figure 10. Printed Circuit Board (Top Layer)

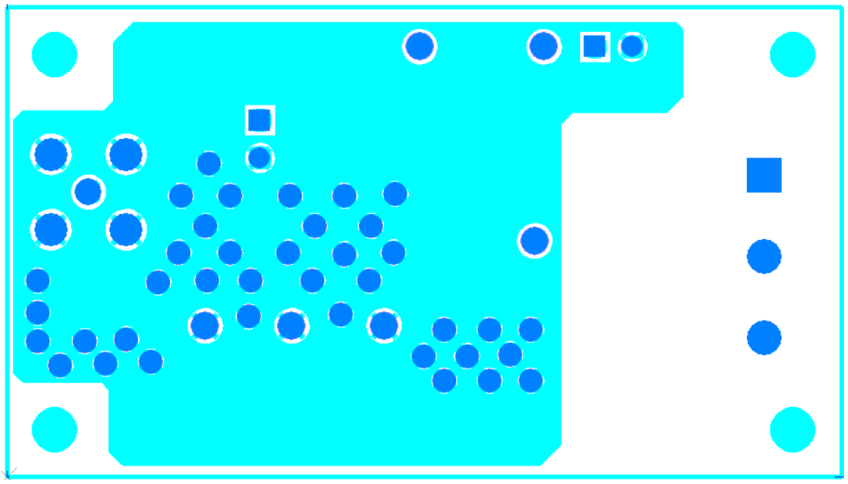

Figure 11. Printed Circuit Board (Bottom Layer)

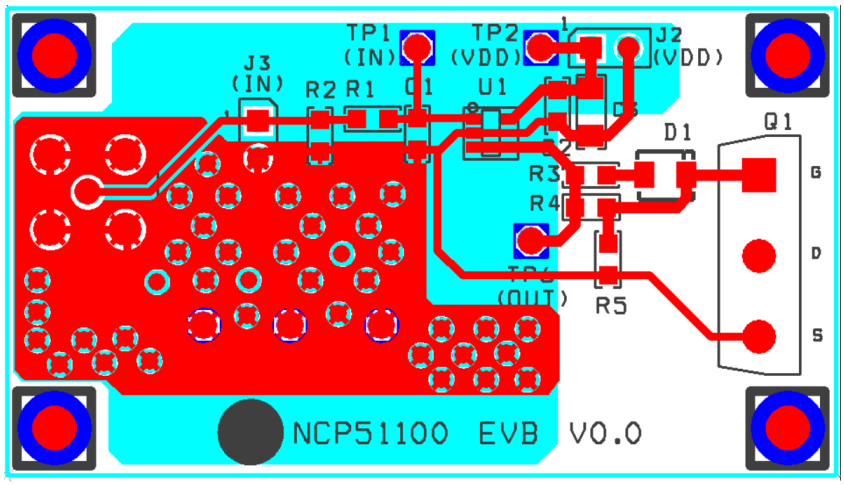

Figure 12. Printed Circuit Board (Top & Bottom Layer)

Table 3. BILL OF MATERIALS

#	Ref.	Part No.	Spec	Q'ty	Manufacturer	Pkg Type
1	C1	X (open)	N/A	1	N/A	
2	C2	CL21B104KBFNNNE	100 nF, 50 V, X7R	1	SAMSUNG ELEC.	0805 (2012)
3	C3	CL31B106KBHNNNE	10 uF, 50 V, X7R	1	SAMSUNG ELEC.	1206 (3216)
4	D1	SS25FA	50 V 2 A (Schottky Barrier)	1	ON SEMI	SOD−123FL
5	J1	731000207	SMB, RF Connector	1	MOLEX	Rhru−Hole
6	J2,J3	A2−2PA−2.54DSA	2 Pin Header	2	Hirose	Rhru−Hole
7	R1	TRR10EZPJ000	0 Ω, 5%, 1/4W	4	ROHM	0805 (2012)
8	R2	ESR10EZPJ510	51 Ω, 5%, 1/4W	1	ROHM	0805 (2012)
9	R3	ESR10EZPJ4R7	4.7 Ω, 5%, 1/4W	1	ROHM	0805 (2012)
10	R4	ESR10EZPJ101	100 Ω, 5%, 1/4W	1	ROHM	0805 (2012)
11	R5	ESR10EZPJ106	100K, 5%, 1/4W	1	ROHM	0805 (2012)
12	*TP1, TP2, TP3, TP4, TP5, TP6	8654	Test Point, 1mm hole	6	Youngjnsa	Rhru−Hole
13	U1	NCP51100	1K ohm, 5%, 1/4W	1	ON SEMI	SOT23−5
14	U2	X (open)	N/A	1	N/A	

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