EVBUM2696/D

QHS952-DS1-GEVK Evaluation Board User's Manual

ON Semiconductor®

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EVAL BOARD USER'S MANUAL

Introduction

QHS952−DS1−GEVK is single RGMII hardware reference module for Quantenna® QT3952BC chipset. This module can be integrated with different Residential GW SoCs to provide up to 1.7 Gbps PHY/Data Link Speed in 80 MHz mode. It consists of one 11ac digital baseband chip and one 2 chain 5 GHz/2.4 GHz RFIC with Skyworks SKY85806 dual−band FEM.

Description

The QT3952BC chipset supports the 802.11ac/n/a standards and 2 streams in 2x2 MU−MIMO configuration. Each FEM can be configured as 5 GHz or 2.4 GHz. QHS952−DS1−GEVK has single RGMII port, which supports 1 Gbps/100 Mbps/10 Mbps.

I/O Interfaces and Features

- Baseband Chip for Cost Effective 2x2 5 GHz or 2.4/5 GHz Dual Band Selectable (DBS) Client Solution
- 2x2 MIMO Configuration: 2 Spatial Streams
- Digital Transmit Beamforming: Explicit and Blind (Implicit)
- Advanced MIMO Features STBC and Channel State Aware Link Management for Sustained Link Robustness
- DSP Engine to Hardware Accelerate Aggregation, De−aggregation, and Packet Re−ordering
- MU−MIMO Client
- LDPC Support
- Supports QT6225B RFIC for Either 2.4 GHz or 5 GHz Applications
  - 802.11ac/n/g/b/a Compliant
- Additional Standards:
  - 802.11e (QoS)
  - 802.11h (DFS & TPC)
  - 802.11i (Security)
  - 802.11k(RRM)
  - 802.11r (Fast Transitions)
  - 802.11v (Network Management)
  - 802.11w (PMF)

Figure 1. QHS952−DS1−GEVK Photo

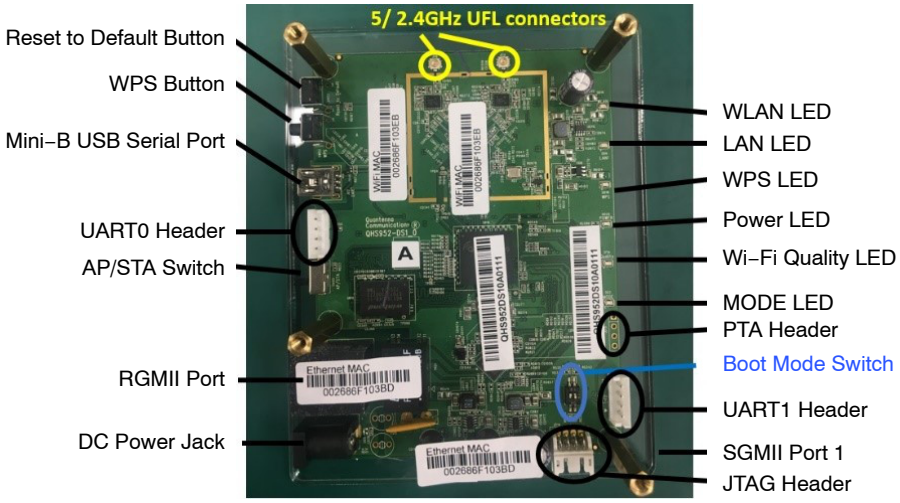


Figure 2. QHS952−DS1−GEVK Description

APPLICATIONS INFORMATION

Power Configuration

QHS952−DS1−GEVK is designed to be powered externally. The external power supply should be 5 V DC. When the board is powered on, the power LED will be steady green.

Reset to Default Button

Reserved (Reset to Default Button).

WPS Button

Reserved (WPS Button).

AP/STA Switch

Reserved (AP/STA Switch)

RGMII Port

RGMII supports 1 Gbps/100 Mbps/10 Mbps UTP speed.

Mini−B USB Serial Port

The Serial port is mainly used for debug purpose.

Table 1. SERIAL PORT SETTING

Baud Rate	115200
Data	8 bit
Parity	None
Stop	1 bit
Flow Control	None

Boot Mode Switch

Boot mode switch controls serial port mode.

Table 2. BOOT MODE SWITCH DEFINITION

State	Definition
00	bootm
10	SPI−0 (Default)

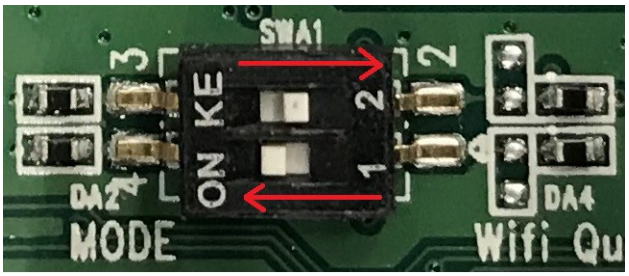


Figure 3. Default Setting (SPI−0)

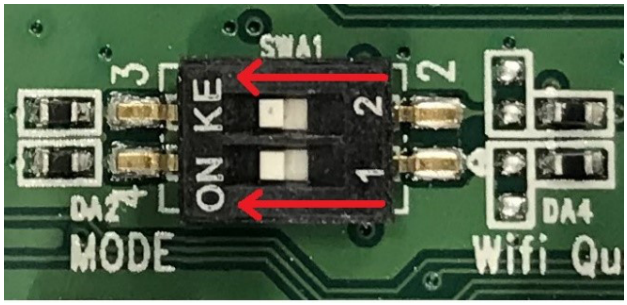


Figure 4. Bootm Setting

BOARD POWER UP

LED Indication When QHS952−DS1−GEVK Powers Up

Figure 5. LED Indication When QHS952−DS1−GEVK Powers Up

Console Display When QHS952−DS1−GEVK Successfully Boots Up

When QHS952−DS1−GEVK successfully boots up, it will show “quantenna #”.

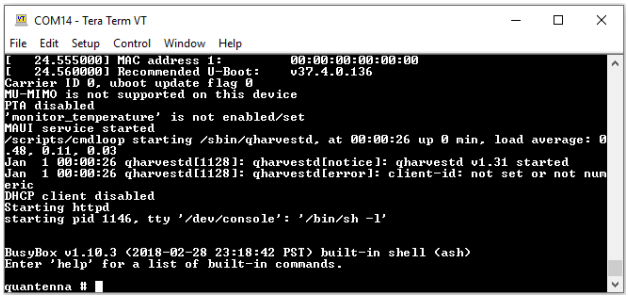


Figure 6. QHS952−DS1−GEVK Successfully Boots Up

Web GUI

QHS952−DS1−GEVK default IP address is 192.168.1.200.

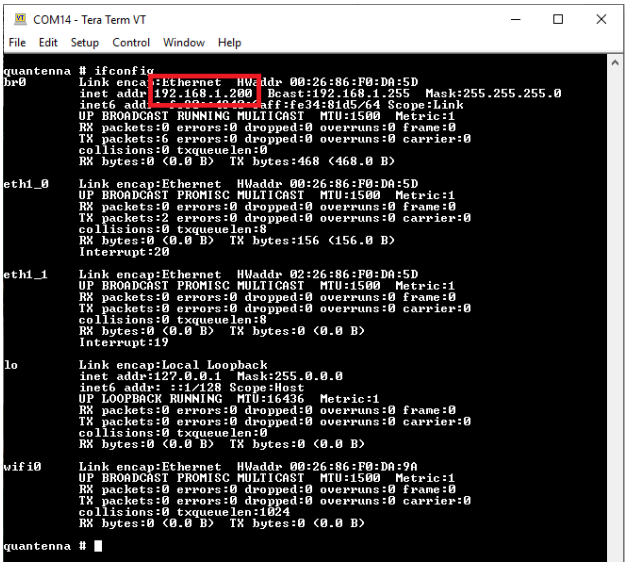
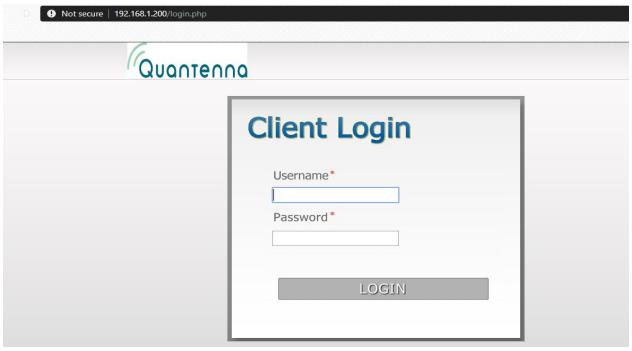


Figure 7. Default IP Address



Web GUI username: super
password: super

Figure 8. Web GUI Username and Password

Telnet

QHS952−DS1−GEVK could also be accessed through telnet. Use board IP address and the login username is “root”.

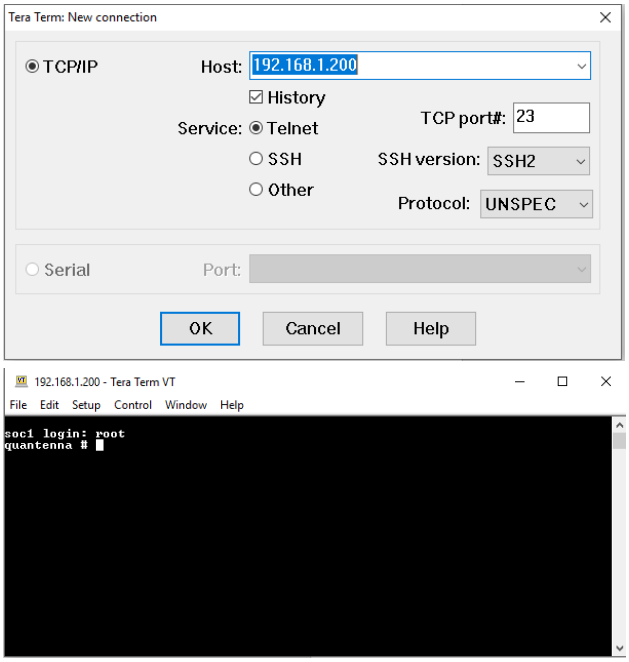


Figure 9. Access Through Telnet

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