Ezairo® 7160 SL Hybrid Demonstrator Board User's Manual

EVBUM2581/D

BOARD DESIGN & OVERVIEW

Purpose

This manual provides information on the configuration and use of the Ezairo 7160 SL Hybrid Demonstrator Board.

The demonstrator board is designed to be used with the Ezairo Preconfigured Suite (Pre Suite), or the Ezairo 7100 Open−Programmable Evaluation and Development Kit (EDK) to develop wireless−enabled hearing aids based on the Ezairo 7160 SL.

Manual Organization

The *Hybrid Demonstrator Board Manual* contains the following chapters and appendices:

- Chapter 1: Introduction describes the purpose of this manual, describes the target reader, explains how the book is organized, and provides a list of suggested reading for more information.
- Chapter 2: Overview provides an overview of the Demonstrator Board described in this manual.
- Chapter 3: Configuration provides the details of the Demonstrator Board. The chapter contains information on the following topics:
  - Demonstrator Board Setup
  - Demonstrator Board Design
  - Power Supply
  - Level Translators
  - LED Circuitry
  - Promira/CAA Debug Port
  - SWJ−DP Debug Port
  - Digital Input/Output (DIO)
  - Test Points

Further Reading

For any technical information not covered in this manual, refer to the following documents:

- Promira™ Serial Platform Quick Start Guide, available at totalphase.com
- Communication Accelerator Adaptor Manual, which is installed with the Communication Accelerator Adaptor (CAA) software
- Integrated Development Environment User's Guide
- Introduction to Ezairo 7100 Programming
- CFX DSP Architecture Manual
- Hardware Reference Manual for Ezairo 7100
- HEAR Configurable Accelerator Reference Manual for Ezairo 7100
- Firmware Reference Manual for Ezairo 7100
- SK4 ELF Toolchain Reference for Ezairo 7100
- Ezairo 7160 SL Datasheet
- Ezairo Sound Designer Software User Manual

BOARD DESIGN & OVERVIEW

Introduction

The Ezairo 7160 SL Hybrid Demonstrator Board is designed to easily develop high−performance hearing aids based on the Ezairo 7160 SL hybrid. The miniature, wireless−enabled hybrid includes an Ezairo 7100 audio processor, RSL10 Bluetooth® Low Energy radio, 2 Mb of EEPROM memory (EA2M) and passive components. The board features many configuration options available via standard 0.1" header pins, and an on−board J−Link debugger based on the Atmel ATSAM3U2CA−AU microcontroller. Using a USB cable, the on−board debugger is used to interface the RSL10 radio within the Ezairo 7160 SL hybrid with a PC for debugging, data collection, or monitoring purposes.

Two versions of the Ezairo 7160 SL demonstrator board are available. The first board is the E7160SL−001GEVB which contains an elastomer socket and is designed for general use. This version of the board is recommended for development, testing and debug purposes since it enables the Ezairo 7160 SL module contained in the socket to be easily swapped out. During development, testing or debug, it may happen that the Ezairo 7160 SL enters a state where it no longer operates as expected – for example, due to improper manipulation of data in the EEPROM. In such a case, the user can take advantage of being able to easily replace the hybrid module on this version of the board. For this reason, **onsemi** recommends using the E7160SL− 001GEVB during development.

The second board is the E7160SL−002GEVB which is optimized for RF testing and characterization. The Ezairo 7160 SL hybrid is directly reflowed on the board, which minimizes the impedance between the onboard matching network and the Ezairo 7160 SL.

Note: The E7160SL−001GEVB doesn't contain an Ezairo 7160 SL module, which are sampled separately. The E7160SL−002GEVB contains one hybrid module soldered on the board.

The Ezairo 7160 SL demonstrator board main functional blocks are shown in Figure 1.

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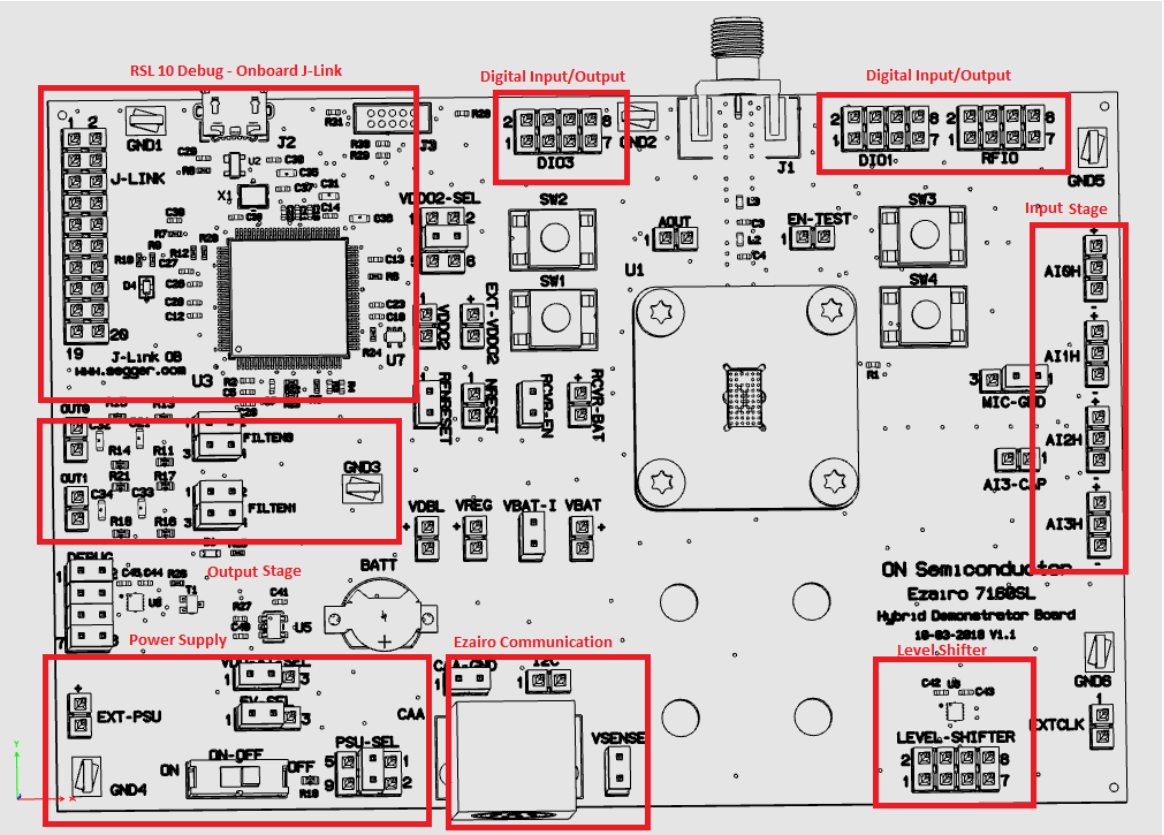

Figure 1. Ezairo 7160 SL Hybrid Demonstrator Board Overview

Ezairo 7160 SL Demonstrator Board Features

- On−board J−Link adaptor for debugging through a USB connection to the PC
- Alternate on−board SWJ−DP (serial−wire and/or JTAG) interface for debugging the Arm® Cortex−M3 processor
- Access to all Ezairo 7160 SL peripherals via standard 0.1” headers
- Onboard 4−bit level translator to translate the DIOs and debug interface at low voltage to a 3.3 V JTAG debugger
- 4 Push Button Switches
- On board 3.3 V Regulator
- 3 LEDs
- Test points and GND hooks for easy probing
- Size 13 ZnAir Battery Holder
- Current measuring header
- Elastomer socket with hybrid (E7160SL−001GEVB only)
- Antenna matching and filtering network

CONFIGURATION

Ezairo E7160SL−001GEVB Socketed Board

The socket used on this version of the Ezairo 7160 SL demonstrator board is designed for easy, tool−free, use. The following are the steps required to ensure proper function of the socket.

Aligning the Clamp

1. Ensure that the rubber plunger sits flush with the top of the grey adapter plate near the end of the range of motion of the clamp.
2. With minimal pressure, the clamp should lock into place.
3. Ensure that the rubber plunger lines up with the cutout in the grey adapter plate.
4. Tighten all nuts fully if adjustment was required.

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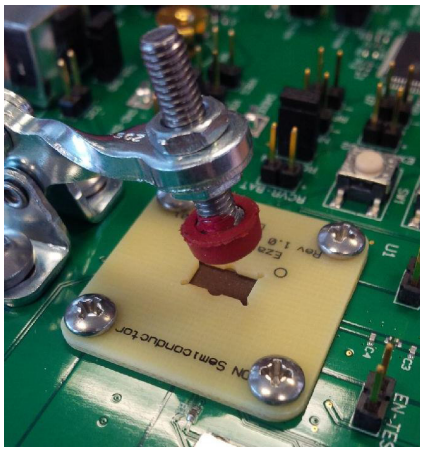

Figure 2. Aligning the Clamp with the Adaptor Plate

Inserting the Hybrid

1. Open the clamp fully.
2. Align the pin 1 marker on Ezairo 7160 SL with the marker on the adapter plate.
3. Insert the hybrid into the socket (ensure the hybrid is fully inserted and level).
4. Fully close the clamp, ensuring it locks into place. *Note: The clamp should not require more than 1 kg of force to fully close.*

Ezairo 7160SL−002GEVB Reflowed Board

The Ezairo 7160 SL reflowed demonstrator board has the Ezairo 7160 SL module soldered to PCB and does not require any additional assembly with respect to the Ezairo 7160 SL module.

***Important note*:**
When VDDO2 is referenced to VDBL (a requirement for FOTA upgrades and when the Authentication Co−processor 3.0 is used), upgrading the firmware on the RSL10 can fail on the Ezairo 7160 SL Hybrid Development Board. This is due to an issue with the board where the RFNRESET pin is pulled up to VBAT via a resistor (R1) instead of VDDO2. To work around this problem you must do one of the following:

- Remove R1.
- Install a stronger pullup resistor between RFNRESET (D5) and VDDO2.

Getting Started

Introduction

This chapter explains how to get started with Ezairo 7160 SL using the Ezairo Sound Designer Software.

Note: IF you are programming the device with your own firmware, refer to the documentation provided with the Ezairo 7100 Evaluation and Development Kit (EDK).

Hardware Requirements

- A programming box to connect the hybrid demonstrator board to a computer. Supported programmers are:
  - Promira Serial Interface from Total Phase, Inc., driver version 1.3.6
  - Communication Accelerator Adaptor (CAA), driver version 1.3
  - HI−PRO, driver version 2.0.0.4
  - DSP Programmer Version 3
  - NOAHlink
  - BlueGiga (Pre Suite only)

Software Requirements

Ezairo Sound Designer Software* (For access, contact medical.content@onsemi.com)
*NDA Required

1. Connect the product to your programmer and to your computer, as follows:
   - Connect your input source to the negative and center pins of the 3−pin AI1H header.
   - Connect your recording or listening equipment to the output, which is labelled OUT0. You might require an external amplifier to drive headphones from the output.
   - You can use SW1 and SW2 (found on the demonstrator board) to adjust the volume. The maximum input signal range is approximately 2 Vpp (volts peak−to−peak).
   - Unused audio inputs (AI0H, AI1H, AI2H and AI3H) can be left floating.
2. Power on the board using the ON−OFF switch.
3. Next, start Sound Designer software by double−clicking on the SD/sounddesigner.exe shortcut, which you will find wherever you installed the Sound Designer software files.
4. Select a workspace, or create a new one.
5. If you do not have a workspace directory available, click Browse and the software allows you to create one. If you click Browse and select a pre−existing directory for your workspace, make sure it is empty. For this example, check Import Sample Workspace, and select E7160SL from the drop−down list. Click OK.
6. Open the console window by clicking the Show console icon. The console window displays error and status messages accumulated in this session. We recommend having the console viewable at all times while using Sound Designer software, to get immediate status information.
7. Click on Control Panel and then, for this example, double−click the Ezairo7160SL.param sample parameter file to open the demo product library.
8. To connect to the device, go to the SETTINGS window. Select the correct Programmer, and Port if applicable. If you also select Verify NVM Writes, the software burns the settings to the device's Non−Volatile Memory and then immediately reads

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back the settings to confirm that the values burned to the device match what is being read out of the device. This option requires additional programming time. Next, click on Detect. A successful detection will populate the device information in the Device Info box.

9. Use the back button−the arrow in the top left corner−to return to the Control Panel.
10. To configure the device for the selected product, click Programmer > Connect. If the connection succeeds, the Connection status symbol appears to the right of the File Name. You can hover over this symbol to view the programmer name and the firmware ID of the device. The connected device must now be configured before you can read, burn or write parameters in Control Panel. Click Programmer > Configure to do this.
11. Now you are ready to begin. See Chapter 3, “Modeler” on page 15 of the Ezairo Sound Designer Software User Manual for your next steps in the process of developing a product with Sound Designer software.

Power Supply

The Ezairo 7160 SL demonstrator board is split into two distinct subsystems, the Ezairo 7160 module and an Atmel microcontroller which acts as an on−board J−Link debugger, to interface and control the RSL10 portion of the Ezairo 7160 SL hybrid without using an external J−Link device. Therefore, there are also 2 subsystems in the power supply. One subsystem supplies power to the Ezairo 7160 SL and the other supplies power to the Atmel microcontroller, with variations and configurations options available for each.

Ezairo 7160 SL Demonstrator Board Power Supply

Ezairo 7160 SL can be powered from several sources, including the onboard battery connector, an external power supply connected via header pins, or from the 6−pin DIN CAA connector. Shorting two pins together on the PSU_SEL header chooses which supply source to use, see Table 1. It is also possible to separately turn off the Ezairo 7160 SL using the on−off switch. This will only turn off power to that module, not the onboard Atmel microcontroller. This can, for example, be used to save battery power if using a battery as the power supply source. For Ezairo 7160 SL to be powered, the VBAT−I header must also be shorted. The VBAT−I header optionally provides a location to measure current consumption of Ezairo 7160 SL.

Table 1. Ezairo 7160 SL POWER SUPPLY OPTIONS

PSU_SEL	Power Supply Source
Short pin 1 to 2	6−Pin DIN (CAA Connector)
Short pin 3 to 4	External Bench Supply (EXT_PSU header)
Short pin 5 to 6	Battery (On board battery holder)

Table 2. VBAT SUPPLY

Pin Name	Min	Nom	Max
VBAT	1.13 V	1.25 V	2.0 V

Atmel Microcontroller Power Supply

The Atmel microcontroller core is powered by a 3.3 V LDO regulator. The regulator is powered by a 5 V rail, which is supplied either by a USB or JTAG connection. The source for this 5 V rail is selected using the 5 V_SEL header. See Table 3. This 3.3 V power source is provided to the microcontroller’s internal regulator, which outputs 1.8 V that is used to power the microcontroller. The rest of the voltage supplies on the microcontroller, for Digital Input/Outputs and Analog references, etc. are supplied from the VDD_AT_SEL header. See Table 4 for configuration options. Table 5 lists the range of voltage outputs possible for the VDBL output. Do note that the UTMI on the microcontroller expects 3.0 V – 3.6 V. Selecting VDBL as a source will put the UTMI out of its operating range. See the Ezairo 7100 Hardware Reference Manual on details for VDBL configuration.

Table 3. ATMEL MICROCONTROLLER POWER SUPPLY SELECTION

PSU_SEL	Power Supply Source
Short pin 1 to 2	USB power
Short pin 2 to 3	JTAG power

Table 4. ATMEL MICROCONTROLLER DIO, AREF, UTMI POWER SUPPLY SELECTION

PSU_SEL	Power Supply Source
Short pin 1 to 2	3.3 V Onboard regulator
Short pin 2 to 3	Configurable voltage output from E7160 (VDBL)

Table 5. VDBL VOLTAGE CONFIGURABLE OUTPUT RANGE

Pin Name	Min	Nom	Max
VBAT	1.8 V	2.0 V	2.1 V

Communication

There are a few ways of achieving communication with the Ezairo 7160 SL demonstrator board:

The micro USB connection (J2) is a J−Link onboard adaptor that provides a SWJ−DP/UART interface for debugging of the RSL10.

It is also possible to connect and debug RSL10 via standard JTAG. The JTAG (J−Link header) connector is compatible with the J−Link debugging device from Segger.

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The TC2050−IDC connector (J3 header) is used to program the Arm Cortex−M3 processor inside the Atmel microcontroller, with J−Link firmware.

Communication and debugging of Ezairo 7100 can be achieved through the Promira Serial Platform from TotalPhase through an I2C interface. The Communication Accelerator Adapter (CAA) is also supported. The serial interface can be connected to the CAA or Promira through the 6−pin DIN connector.

For troubleshooting purposes the I2C signals can be probed on a standard 0.1" header available, labelled I2C, that allows connection to the SDA (pin 2) and SCL (pin 1).

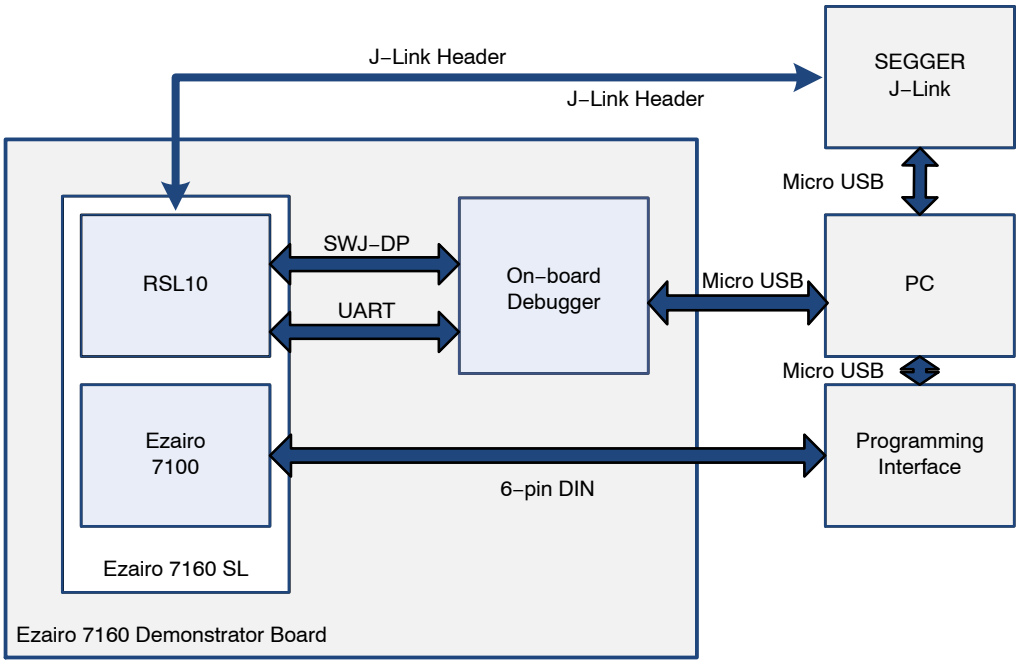

Figure 3. Communication Connections

Table 6. DIN CONNECTOR PIN−OUT

Pin Number	Serial Interface Pin Description
1	Supply Voltage from the Serial Interface
2	System Ground
3	SCL (I2C Clock)
4	SDA (I2C data)
5	VBAT (Sense Voltage)
6	No Connect

Table 7. COMMUNICATION CONFIGURATION

Header	Configuration Description
VSENSE	Connects VBAT to the SENSE pin on the 6−pin DIN connector, if shorted.
CAA−GND	Connects the ground from the Promira/CAA to the HDB ground, if shorted.
NRESET	Can be used to measure the NRESET line on the Ezairo 7100, or to reset it if shorted.
EXTCLK	Pin to connect an external clock source to drive the Ezairo 7160 SL module, specifically, the Ezairo 7100 audio DSP.

RSL10

The RSL10 is a Bluetooth Low Energy radio which is used within Ezairo 7160 SL relaying information from the Ezairo 7100 DSP to an external device, via Bluetooth Low Energy. There is an on−board coaxial 50 Ω SMA connector (J1) that can be used for attaching a 2.4 GHz Bluetooth antenna. The demonstrator board also includes an RF filtering circuit on the antenna input/output.

Level Shifters

The Ezairo 7160 SL demonstrator board includes two on−board level shifters. The DEBUG header is used to enable debugging of the RSL10 via the Atmel microprocessor.

Table 8. DEBUG HEADER CONFIGURATION

Pin Configuration	Configuration
Short pin 7 to 8 and short pin 5 to 6	SWJ−DP Debugging enabled
Short pin 3 to 4 and short pin 1 to 2	Enable serial communication between RSL10 and Atmel microcontroller
Short pin 2 to 4	Enable serial loop back on Atmel microcontroller

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The board also includes a second level shifter accessible via the LEVEL_SHIFTER header. This is made available to connect external peripherals to Ezairo 7160 SL via the RFIO/DIO headers that operate at higher voltages. Pins 1, 3, 5, 7 use the VDDO2 reference supply voltage selected via the VDDO2_SEL header. This is the supply that the E7160 and more specifically, the RSL10 DIOs and Ezairo 7100 DIO bank 2 use. An external power supply voltage can be connected via the EXT_VDDO2 header. This voltage then can be used to supply VDDO2, using the VDDO2_SEL header, negating the need for the level shifter, if the voltage connected is safe for the Ezairo 7160 SL hybrid. Otherwise, if VDDO2 and EXT_VDDO2 differ, EXT_VDDO2 will be used as the reference for pins 2, 4, 6, 8 of the level shifter.

Table 9. VDDO2 HEADER CONFIGURATION

Pins	VDDO2 Source
Short pin 1 to 2	VDBL
Short pin 3 to 4	VBAT
Short pin 5 to 6	VEXT (EXT-VDDO2)

Input Stage

The Ezairo 7160 SL demonstrator board provides access to four analog audio inputs (AI0H, AI1H, AI2H, and AI3H). The ground reference for the inputs can be adjusted using the MIC-GND header as follows:

Table 10. INPUT GROUND REFERENCE SELECTION

MIC-GND	Input Ground Reference
Short pin 1 to 2	GND_MIC*
Short pin 2 to 3	AGND

*Use GND_MIC reference when input is from a microphone. For other electrical test equipment use AGND.

There is also an optional AI3−CAP header that can be used to place a capacitance in between the AI3H input and the AI3 ADC pin.

Output Stage

There are two digital outputs (RCVR0, RCVR1) available on the board through standard 0.1” header. The direct digital outputs are available on headers FILTEN0, FILTEN1, respectively. Separate RC filter networks are provided to attenuate out−of band noise from the direct digital outputs when connected to high impedance audio measurement equipment (OUT0, OUT1). The on−board RC filters are enabled by the FILTEN0/FILTEN1 headers as described in Table 12. To enable output, configure the RCVR−EN and RCVR−BAT headers as described in Table 11.

Table 11. OUTPUT STAGE ENABLE CONFIGURATION

Header	Configuration Description
RCVR−EN	Enable the output drivers of the Ezairo 7160 SL using VBAT as a source, if shorted.
RCVR−BAT	Enable the output drivers of the Ezairo 7160 SL using the voltage connected to this header as the source, if shorted. RCVR−EN must be disconnected.

Table 12. ON−BOARD RC FILTER CONFIGURATION

Function	FILTEN0/FILTEN1
Disabled	open pins 1 to 2 open pins 3 to 4
Enabled	short pins 1 to 2 short pins 3 to 4

Note: To connect receivers or loud speakers (without the RC filter) use headers FILTEN0/FILTEN1 pins 2 and 4.

Digital Input/Output (DIO)

The Ezairo 7160 SL Hybrid Demonstrator Board contains 19 digital I/O (DIO) signals available on three separate 2x4 headers that provide access to a wide variety of interfaces (GPIO, SPI, PCM, I^2C, UART, LSAD, clocks). See the table below for pin out and reference domains. Pin 1 of each header has the corresponding reference domain. Pin 8 on each header is ground. Pin 6 of the RFIO header is ground.

Table 13. DIO/RFIO REFERENCE DOMAINS

DIOs	DIO Header Pin	Header	Reference Domain
20	3	DIO3	VBAT
21	5	DIO3	VBAT
22	7	DIO3	VBAT
23	2	DIO3	VBAT
24	4	DIO3	VBAT
29	6	DIO3	VBAT
4	3	DIO1	VDBL
5	5	DIO1	VDBL
6	7	DIO1	VDBL
7	2	DIO1	VDBL
8	4	DIO1	VDBL
9	6	DIO1	VDBL
RFIO0	3	RFIO1	VDDO2
RFIO1	5	RFIO1	VDDO2
RFIO2	7	RFIO1	VDDO2
RFIO3	2	RFIO1	VDDO2
RFIO12	4	RFIO1	VDDO2

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The Ezairo 7160 SL demonstrator board also has three momentary switches that can be used as momentary hard pull−downs on DIO24 (SW1), DIO29 (SW2) and RFIO1 (SW3).

SW4 can be used to reset the RSL10 radio.

Test Point Headers

Below is a table (Table 14) containing of a list of 0.1” headers on the board that are provided as measurement test points. There are also several ground hooks available on the board as an easy way to provide a reference. They provide easy access to RFGND, DGND, GND−BAT and GNDOD.

Table 14. OUTPUT STAGE ENABLE CONFIGURATION

Header	Measurement
VREG	Output of the voltage regulator in the Ezairo 7160 SL
VBAT	Output voltage of the connected battery / chosen voltage source.
AOUT	Analog output test point. Can be configured to output from a wide range of internal signals. See RSL10 Hardware Reference.
VBDL	Charge−pump output. Double VREG.
VDDO2	Current VDDO2 voltage level supplied to the E7160.

Indicator LEDs

There are three indicator LEDs on board. Two are connected to the Atmel microcontroller. A green LED is connected to PA29 and a red LED is connected to PA28. These can be turned on by pulling these pins low on the Atmel microcontroller. These 2 LEDs are identified with the label D4. The third LED, D1 is a green led that can be turned on by pulling RFIO0 from the RSL10, low.

Board Design

The following sections detail the various sub−circuits of the Ezairo 7160 SL demonstrator board.

The block diagrams in Figure 6 and Figure 7 show the locations of the various circuit sections.

Figure 4 and Figure 5 provide 3−dimensional illustrations of the Ezairo 7160 SL demonstrator board.

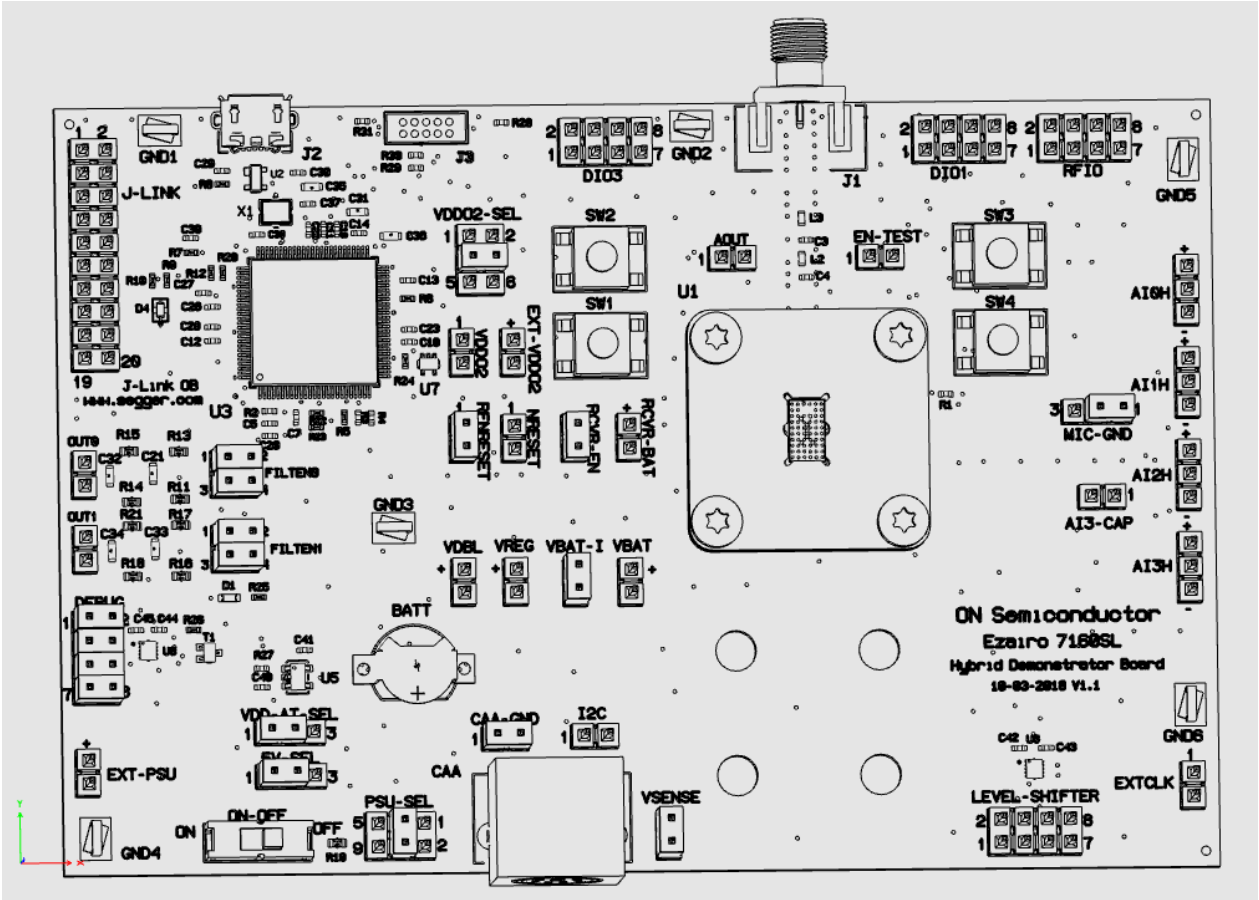

Figure 4. Three−Dimensional Line Drawing of the Board (Top View)

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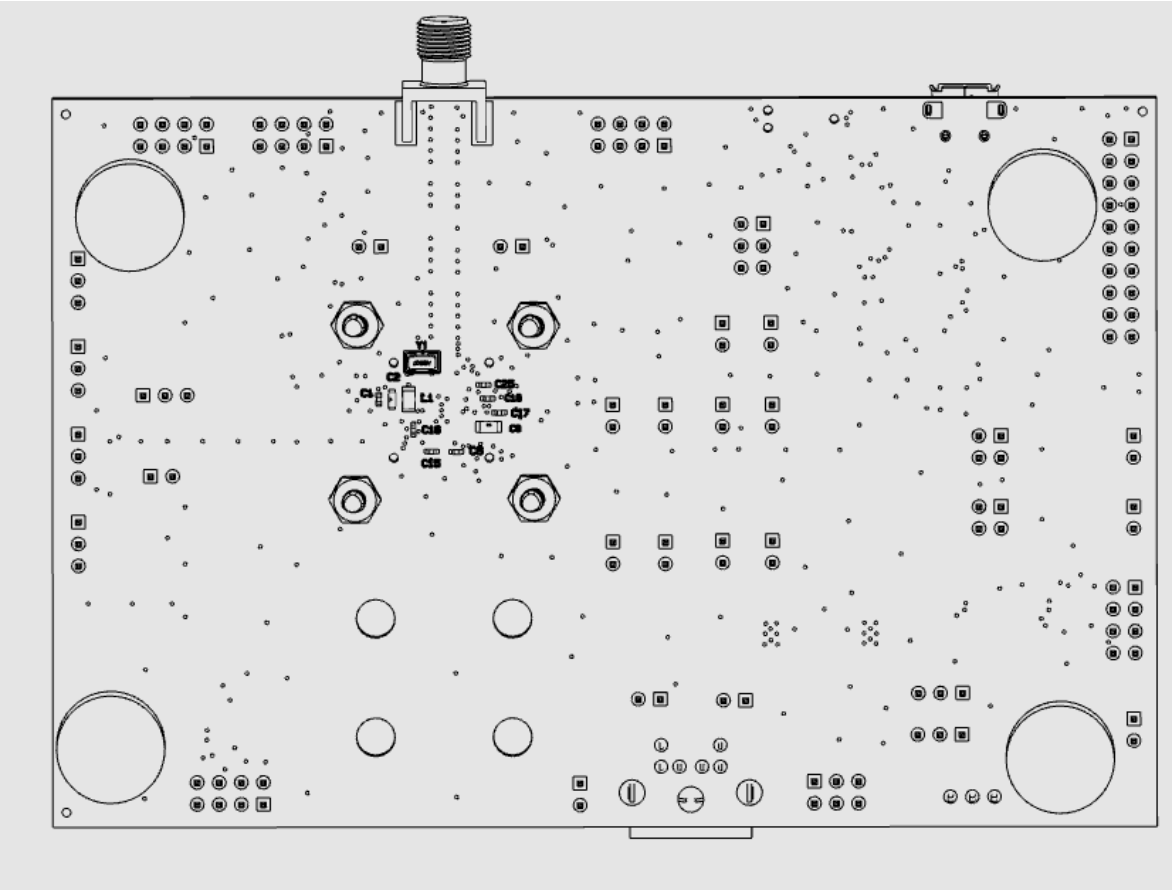

Figure 5. Three−Dimensional Line Drawing of the Board (Bottom View)

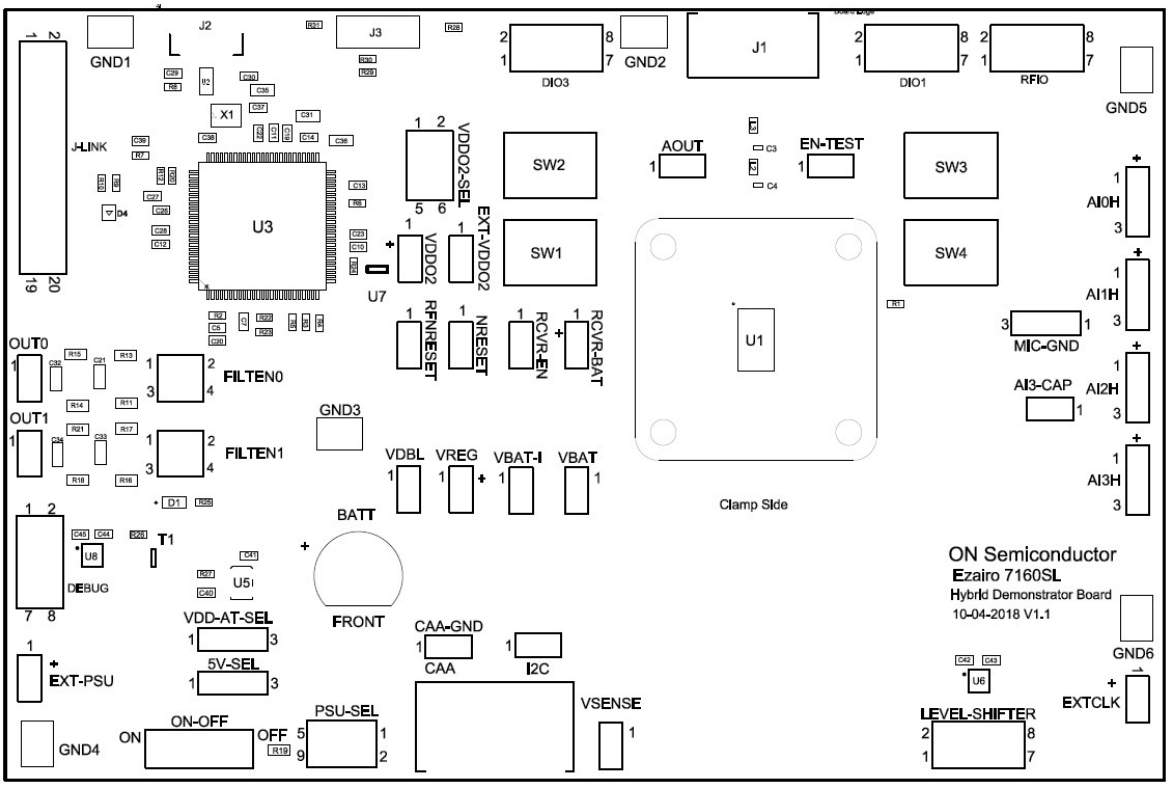

Figure 6. Circuit Location Block Diagram (Top View)

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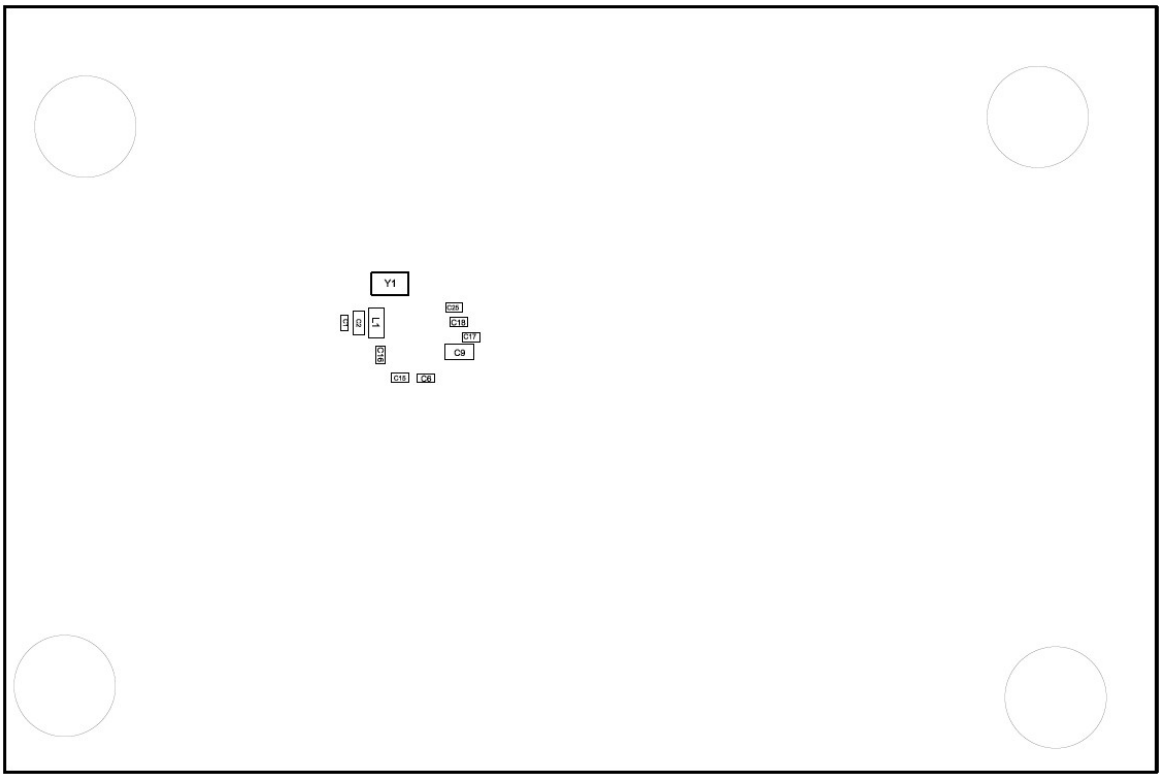

Figure 7. Circuit Location Block Diagram (Bottom View)

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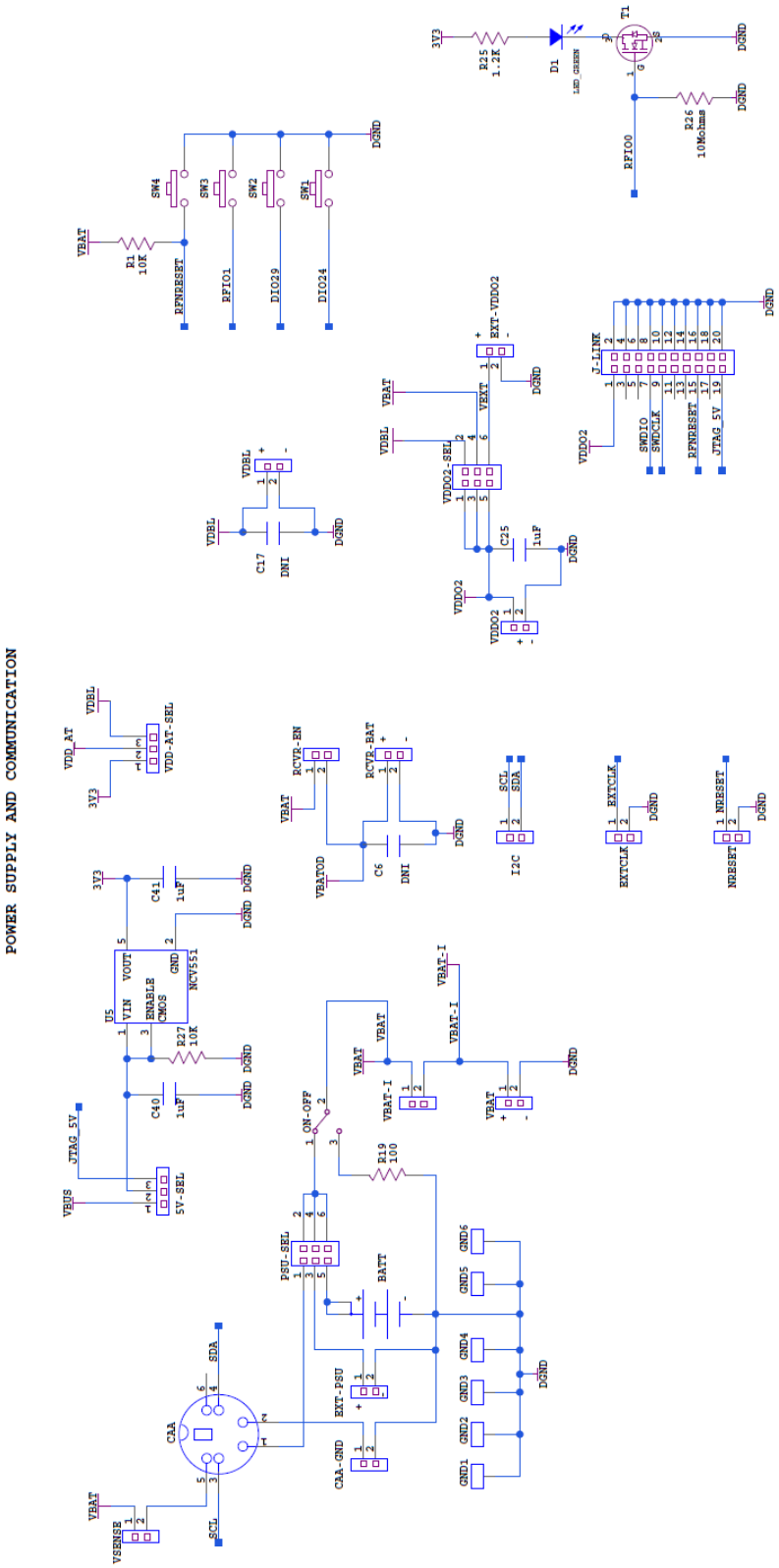
APPENDIX A

Schematic



* R1 and L1 are not required in a hearing aid design and are present for engineering and evaluation purposes.

Figure 8. Power Supply and Communication

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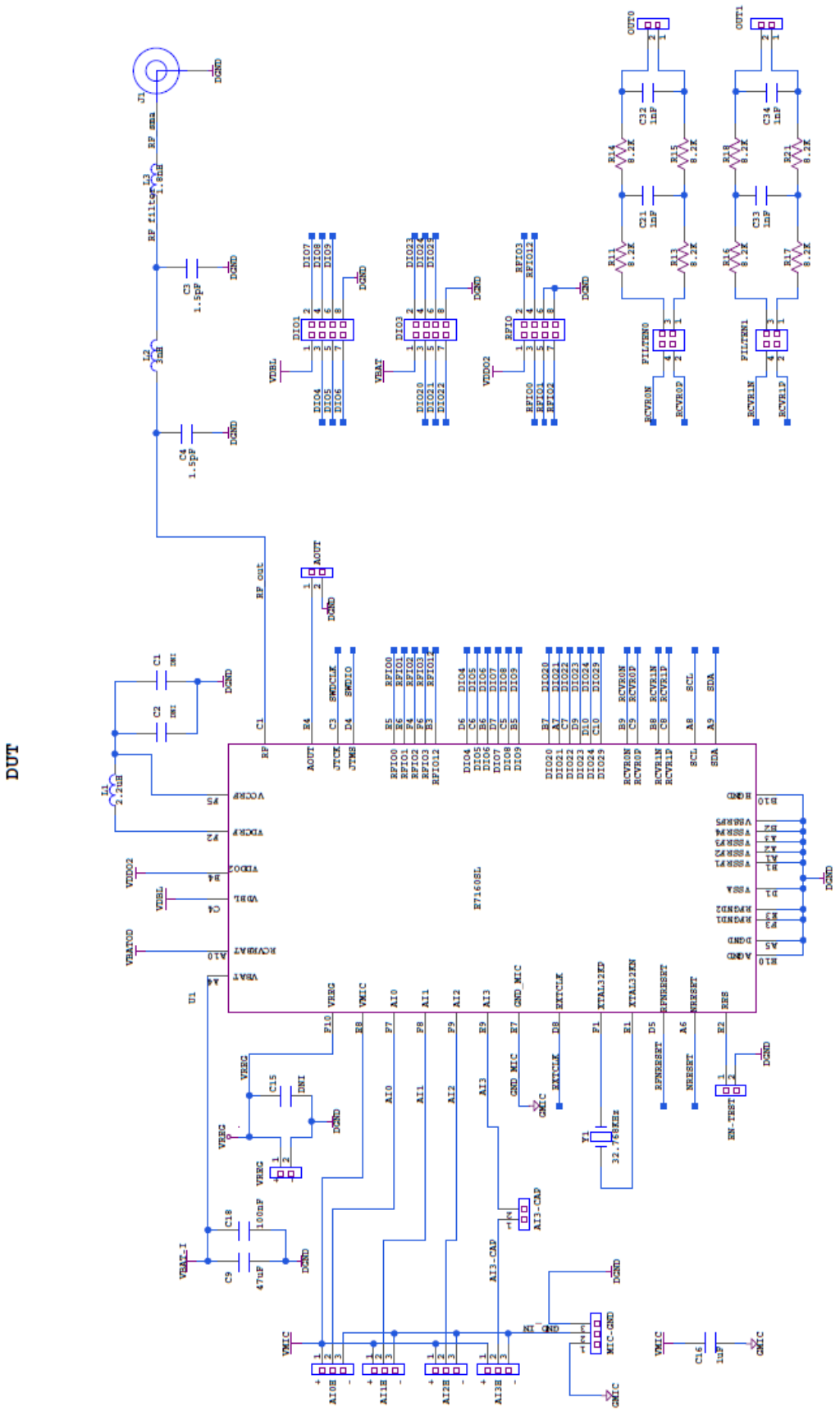

* R1and L1 are not required in a hearing aid design and are present for engineering and evaluation purposes.

Figure 9. DUT

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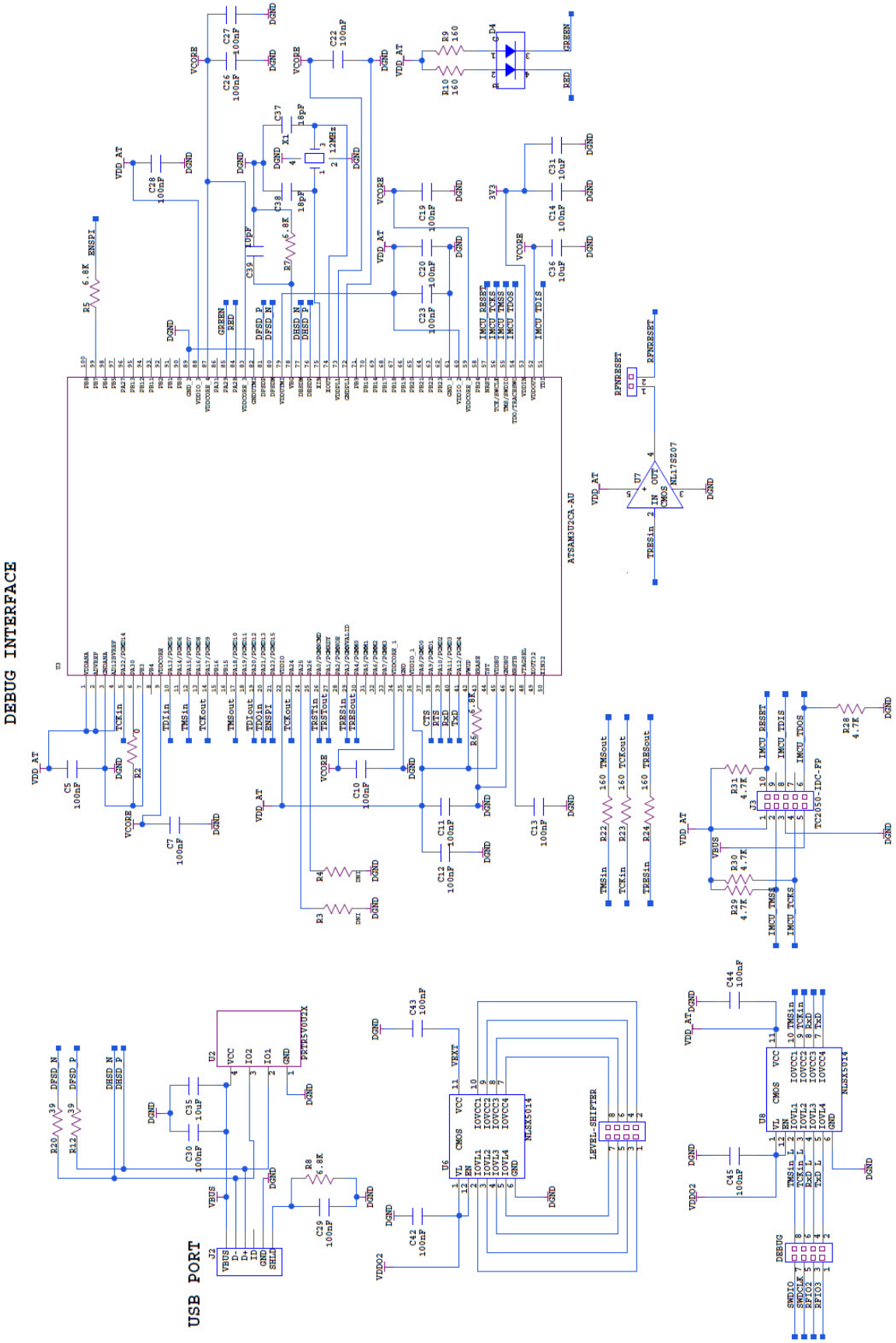

Figure 10. Debug Interface

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